

28-Bit to 56-Bit Registered Buffer With Address Parity Test One Pair to Four Pair Differential Clock PLL Driver

Check for Samples: [SN74SSQEA32882](#)

FEATURES

- JEDEC SSTE32882 Compliant
- 1-to-2 Register Outputs and 1-to-4 Clock Pair Outputs Support Stacked DDR3 RDIMMs
- CKE Powerdown Mode for Optimized System Power Consumption
- 1.5V/1.35V Phase Lock Loop Clock Driver for Buffering One Differential Clock Pair (CK and $\overline{\text{CK}}$) and Distributing to Four Differential Outputs

- 1.5V/1.35V CMOS Inputs
- Checks Parity on Command and Address (CS-Gated) Data Inputs
- Configurable Driver Strength
- Uses Internal Feedback Loop

APPLICATIONS

- DDR3 Registered DIMMs up to DDR3-1600
- DDR3L Registered DIMMs up to DDR3L-1333
- Single-, Dual- and Quad-Rank RDIMM

DESCRIPTION

This JEDEC SSTE32882-compliant, 28-bit 1:2 or 26-bit 1:2 and 4-bit 1:1 registering clock driver with parity is designed for operation on DDR3 registered DIMMs with V_{DD} of 1.5 V and on DDR3L registered DIMMs with V_{DD} of 1.35 V.

All inputs are 1.5 V and 1.35 V CMOS compatible. All outputs are CMOS drivers optimized to drive DRAM signals on terminated traces in DDR3 RDIMM applications. The clock outputs Y_n and $\overline{Y_n}$ and control net outputs $D_x\text{CKEn}$, $\overline{D_x\text{CSn}}$ and $D_x\text{ODTn}$ can be driven with a different strength and skew to optimize signal integrity, compensate for different loading and equalize signal travel speed.

The SN74SSQEA32882 has two basic modes of operation associated with the Quad Chip Select Enable ($\overline{\text{QCSSEN}}$) input. When the $\overline{\text{QCSSEN}}$ input pin is open (or pulled high), the component has two chip select inputs, $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$, and two copies of each chip select output, $\overline{\text{QACS0}}$, $\overline{\text{QACS1}}$, $\overline{\text{QBCS0}}$ and $\overline{\text{QBCS1}}$. This is the "QuadCS disabled" mode. When the $\overline{\text{QCSSEN}}$ input pin is pulled low, the component has four chip select inputs $\overline{\text{DCS}}[3:0]$, and four chip select outputs, $\overline{\text{QCS}}[3:0]$. This is the "QuadCS enabled" mode. Through the remainder of this specification, $\overline{\text{DCS}}[n:0]$ will indicate all of the chip select inputs, where $n=1$ for QuadCS disabled, and $n=3$ for QuadCS enabled. $\overline{\text{QxCS}}[n:0]$ will indicate all of the chip select outputs.

The device also supports a mode where a single device can be mounted on the back side of a DIMM. If $\overline{\text{MIRROR}}=\text{HIGH}$, Input Bus Termination (IBT) has to stay enabled for all input signals in this case.

The SN74SSQEA32882 operates from a differential clock (CK and $\overline{\text{CK}}$). Data are registered at the crossing of CK going HIGH, and $\overline{\text{CK}}$ going LOW. This data could be either re-driven to the outputs or it could be used to access device internal control registers.

The input bus data integrity is protected by a parity function. All address and command input signals are added up and the last bit of the sum is compared to the parity signal delivered by the system at the input $\overline{\text{PAR_IN}}$ one clock cycle later. If they do not match the device pulls the open drain output $\overline{\text{ERROUT}}$ LOW. The control signals ($\overline{\text{DCKE0}}$, $\overline{\text{DCKE1}}$, $\overline{\text{DODT0}}$, $\overline{\text{DODT1}}$, $\overline{\text{DCS}}[n:0]$) are not part of this computation.

The SN74SSQEA32882 implements different power saving mechanisms to reduce thermal power dissipation and to support system power down states. By disabling unused outputs the power consumption is further reduced.

The package is optimized to support high density DIMMs. By aligning input and output positions towards DIMM finger signal ordering and SDRAM ballout the device de-scrambles the DIMM traces allowing low cross talk design with low interconnect latency.

Edge controlled outputs reduce ringing and improve signal eye opening at the SDRAM inputs.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Table 1. ORDERING INFORMATION

T_{CASE(max)}	PACKAGE⁽¹⁾		ORDERABLE ⁽²⁾ PART NUMBER	TOP-SIDE MARKING
See Table 4	176ZAL	Tape and Reel	SN74SSQEA32882ZALR	EA32882B

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
- (2) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

APPLICATION INFORMATION

Vendor Specific SPD Content

SPD EEPROM on DDR3 RDIMMs has 3 vendor specific bytes for vendor and revision ID. This information can be sued by the system BIOS. The following table showsthe correct values for SN74SSQEA32882.

Table 2. Vendor specific SPD content for SN74SSQEA32882

Byte	Value	Description
65	0x80	Vendor ID, part 1
66	0x97	Vendor ID, part 2
67	0x28	Revision ID

Application Reports

For additional Information on SN74SSQEA32882 DDR3 Register please review the following application reports:

- [DDR3 Register CMR programming](#)
- [DDR3 RDIMM SPD settings](#)
- [Yn phase shift on SN74SSQEA32882](#)
- [DDR3 Register IBT Measurement](#)

ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute Maximum Ratings Over Operating Free-Air Temperature Range⁽¹⁾

PARAMETER		VALUE	UNIT
V _{DD}	Supply voltage	–0.4 to +1.975	V
V _I	Receiver input voltage	See ⁽²⁾ and ⁽³⁾	V
V _{REF}	Reference voltage	–0.4 to V _{DD} + 0.5	V
V _O	Driver output voltage	See ⁽²⁾ and ⁽³⁾	V
I _{IK}	Input clamp current	V _I < 0 or V _I > V _{DD}	mA
I _{OK}	Output clamp current	V _O < 0 or V _O > V _{DD}	mA
I _O	Continuous output current	0 < V _O < V _{DD}	mA
I _{CCC}	Continuous current through each V _{DD} or GND pin	±100	mA
T _{stg}	Storage temperature	–65 to +150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) This value is limited to 1.975 V maximum.

Table 4. Case Temperature vs Speed Node

PARAMETER		DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	UNIT
T _{case(max)}	Maximum case temperature ⁽¹⁾	+109	+108	+106	+103	°C

- (1) The temperature values fit to JEDEC RAW cards A, B, and C. The user must keep T_{case} below the specified values in order to keep the junction temperature below +125°C. Other combinations of features and termination resistors can require lower case temperature and extra cooling. These combinations depend on the specific application.

PACKAGE INFORMATION

Pinout Configuration

The package is a 8mm × 13.5mm 176-pin BGA with 0.65mm ball pitch in a 11 × 20 grid. The device pinout supports outputs on the outer two left and right columns to support easy DIMM signal routing. Corresponding inputs are placed in a way that two devices can be placed back to back for 4 Rank modules while the data inputs share the same vias. Each input and output is located close to an associated no ball position or on the outer two rows to allow low cost via technology combined with the small 0.65mm ball pitch.

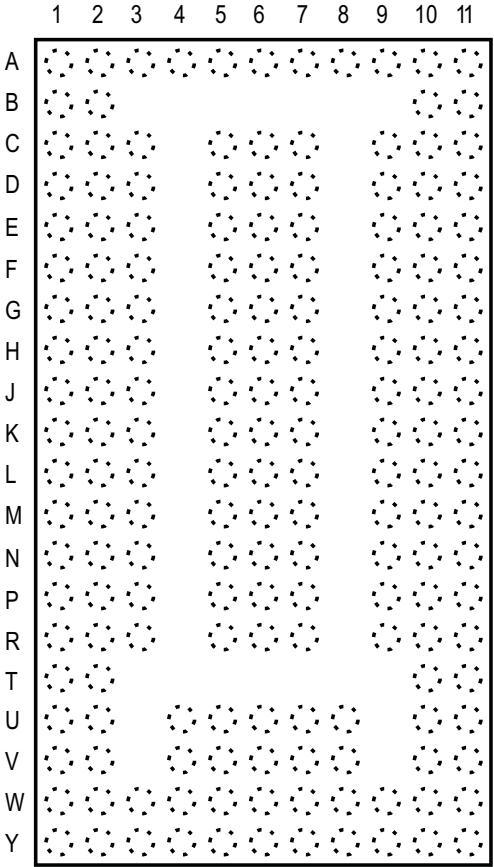


Figure 1. Pinout Configuration

Top View for 176-ball TFBGA (front configuration)
Table 5. Ball Assignment; MIRROR=LOW, QCSEN=HIGH or Floating

	1	2	3	4	5	6	7	8	9	10	11
A	QAA13	QAA8	$\overline{\text{QCSEN}}$	VSS	$\overline{\text{RESET}}$	MIRROR	$\overline{\text{ERROUT}}$	VSS	RSVD	QBA8	QBA13
B	QAA14	QAA7								QBA7	QBA14
C	QAA9	QAA6	VDD		VDD	VDD	VDD		VDD	QBA6	QBA9
D	QAA11	QAA5	VSS		VSS	VSS	VSS		VSS	QBA5	QBA11
E	QAA2	QAA4	VDD		VDD	VDD	VDD		VDD	QBA4	QBA2
F	QAA1	QAA3	VSS		VSS	VSS	VSS		VSS	QBA3	QBA1
G	QAA0	QABA1	VDD		VDD	VDD	VDD		VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS		VSS	VSS	VSS		VSS	QBBA0	QBA12
J	QABA2	$\overline{\text{QACS1}}$	VDD		VDD	VDD	VDD		VDD	$\overline{\text{QBCS1}}$	QBBA2
K	QAA15	QACKE0	VSS		VSS	VSS	VSS		VSS	QBCKE0	QBA15
L	$\overline{\text{QAWE}}$	$\overline{\text{QACS0}}$	VDD		VDD	VDD	VDD		VDD	$\overline{\text{QBCS0}}$	$\overline{\text{QBWE}}$
M	QAA10	QACKE1	VSS		VSS	VSS	VSS		VSS	QBCKE1	QBA10
N	$\overline{\text{QACAS}}$	QAODT0	VDD		VDD	VDD	VDD		VDD	QBODT0	$\overline{\text{QBCAS}}$
P	$\overline{\text{QARAS}}$	QAODT1	DA3		VSS	VSS	VSS		DA4	QBODT1	$\overline{\text{QBRAS}}$
R	DCKE1	DA14	DA15		DA5	RSVD	DA2		DA1	DA10	DOT1
T	DCKE0	$\overline{\text{DCS0}}$								$\overline{\text{DCS1}}$	DOT0
U	DA12	DBA2		$\overline{\text{Y1}}$	PVSS	VDD	PVDD	$\overline{\text{Y0}}$		DA13	$\overline{\text{DCAS}}$
V	DA9	DA11		Y1	PVSS	VSS	PVDD	Y0		$\overline{\text{DRAS}}$	$\overline{\text{DWE}}$
W	DA8	DA6	$\overline{\text{FBIN}}$	$\overline{\text{Y3}}$	AVSS	$\overline{\text{CK}}$	RSVD	$\overline{\text{Y2}}$	$\overline{\text{FBOUT}}$	DA0	DBA0
Y	DA7	RSVD	FBIN	Y3	AVDD	CK	VREFCA	Y2	FBOUT	PAR_IN	DBA1

Pins A9, R6, W7 and Y2 are reserved for future functions must not be connected on system, the system must provide a solder pad for these pins. The device design tolerates floating on these pins. A3 may be left floating since it has an internal pull-up resistor.

Blank space indicate no ball is populated at that gridpoint – vias on the module may be located in these areas

Top View for 176-ball TFBGA (back configuration)

MIRROR=HIGH and QCSEN=HIGH or floating specifies the pinout for SN74SSQEA32882 in back configuration. The device has symmetric pinout with inputs at the south side and outputs to east and west sides. This allows back to back mounting on both sides of the PCB if more than one device is needed.

Table 6. Ball Assignment; MIRROR=HIGH, QCSEN=HIGH or Floating

	1	2	3	4	5	6	7	8	9	10	11
A	QAA13	QAA8	$\overline{\text{QCSEN}}$	VSS	$\overline{\text{RESET}}$	MIRROR	$\overline{\text{ERROUT}}$	VSS	RSVD	QBA8	QBA13
B	QAA14	QAA7								QBA7	QBA14
C	QAA9	QAA6	VDD		VDD	VDD	VDD		VDD	QBA6	QBA9
D	QAA11	QAA5	VSS		VSS	VSS	VSS		VSS	QBA5	QBA11
E	QAA2	QAA4	VDD		VDD	VDD	VDD		VDD	QBA4	QBA2
F	QAA1	QAA3	VSS		VSS	VSS	VSS		VSS	QBA3	QBA1
G	QAA0	QABA1	VDD		VDD	VDD	VDD		VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS		VSS	VSS	VSS		VSS	QBBA0	QBA12
J	QABA2	$\overline{\text{QACS1}}$	VDD		VDD	VDD	VDD		VDD	$\overline{\text{QBCS1}}$	QBBA2
K	QAA15	QACKE0	VSS		VSS	VSS	VSS		VSS	QBCKE0	QBA15
L	$\overline{\text{QAW}}$	$\overline{\text{QACS0}}$	VDD		VDD	VDD	VDD		VDD	$\overline{\text{QBCS0}}$	$\overline{\text{QBWE}}$
M	QAA10	QACKE1	VSS		VSS	VSS	VSS		VSS	QBCKE1	QBA10
N	$\overline{\text{QACAS}}$	QAODT0	VDD		VDD	VDD	VDD		VDD	QBODT0	$\overline{\text{QBCAS}}$
P	$\overline{\text{QARAS}}$	QAODT1	DA4		VSS	VSS	VSS		DA3	QBODT1	$\overline{\text{QBRAS}}$
R	DODT1	DA10	DA1		DA2	RSVD	DA5		DA15	DA14	DCKE1
T	DODT0	$\overline{\text{DCS1}}$								$\overline{\text{DCS0}}$	DCKE0
U	$\overline{\text{DCAS}}$	DA13		$\overline{\text{Y1}}$	PVSS	VDD	PVDD	$\overline{\text{Y0}}$		DBA2	DA12
V	$\overline{\text{DWE}}$	$\overline{\text{DRAS}}$		Y1	PVSS	VSS	PVDD	Y0		DA11	DA9
W	DBA0	DA0	$\overline{\text{FBIN}}$	$\overline{\text{Y3}}$	AVSS	$\overline{\text{CK}}$	RSVD	$\overline{\text{Y2}}$	$\overline{\text{FBOUT}}$	DA6	DA8
Y	DBA1	PAR_IN	FBIN	Y3	AVDD	CK	VREFCA	Y2	FBOUT	RSVD	DA7

Pins A9, R6, W7 and Y10 are reserved for future functions must not be connected on system, the system must provide a solder pad for these pins. The device design needs to tolerate floating on these pins. A3 may be left floating since it has an internal pull-up resistor. Blank space indicate no ball is populated at that gridpoint – vias on the module may be located in these areas

Top View for 176-ball TFBGA (front configuration) in Quad Rank Mode
Table 7. Ball Assignment; MIRROR=LOW, QCSEN=LOW

	1	2	3	4	5	6	7	8	9	10	11
A	QAA13	QAA8	$\overline{\text{QCSEN}}$	VSS	$\overline{\text{RESET}}$	MIRROR	$\overline{\text{ERROUT}}$	VSS	RSVD	QBA8	QBA13
B	QAA14	QAA7								QBA7	QBA14
C	QAA9	QAA6	VDD		VDD	VDD	VDD		VDD	QBA6	QBA9
D	QAA11	QAA5	VSS		VSS	VSS	VSS		VSS	QBA5	QBA11
E	QAA2	QAA4	VDD		VDD	VDD	VDD		VDD	QBA4	QBA2
F	QAA1	QAA3	VSS		VSS	VSS	VSS		VSS	QBA3	QBA1
G	QAA0	QABA1	VDD		VDD	VDD	VDD		VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS		VSS	VSS	VSS		VSS	QBBA0	QBA12
J	QABA2	$\overline{\text{QCS1}}$	VDD		VDD	VDD	VDD		VDD	$\overline{\text{QCS3}}$	QBBA2
K	QAA15	QACKE0	VSS		VSS	VSS	VSS		VSS	QBCKE0	QBA15
L	$\overline{\text{QAWF}}$	$\overline{\text{QCS0}}$	VDD		VDD	VDD	VDD		VDD	$\overline{\text{QCS2}}$	$\overline{\text{QBWF}}$
M	QAA10	QACKE1	VSS		VSS	VSS	VSS		VSS	QBCKE1	QBA10
N	$\overline{\text{QACAS}}$	QAODT0	VDD		VDD	VDD	VDD		VDD	QBODT0	$\overline{\text{QBCAS}}$
P	$\overline{\text{QARAS}}$	QAODT1	DA3		VSS	VSS	VSS		DA4	QBODT1	$\overline{\text{QBRAS}}$
R	DCKE1	DA14	DA15		DA5	$\overline{\text{DCS3}}$	DA2		DA1	DA10	DOTD1
T	DCKE0	$\overline{\text{DCS0}}$								$\overline{\text{DCS1}}$	DOTD0
U	DA12	DBA2		$\overline{\text{Y1}}$	PVSS	VDD	PVDD	$\overline{\text{Y0}}$		DA13	$\overline{\text{DCAS}}$
V	DA9	DA11		Y1	PVSS	VSS	PVDD	Y0		$\overline{\text{DRAS}}$	$\overline{\text{DWE}}$
W	DA8	DA6	$\overline{\text{FBIN}}$	$\overline{\text{Y3}}$	AVSS	$\overline{\text{CK}}$	RSVD	$\overline{\text{Y2}}$	$\overline{\text{FBOUT}}$	DA0	DBA0
Y	DA7	$\overline{\text{DCS2}}$	FBIN	Y3	AVDD	CK	VREFCA	Y2	FBOUT	PAR_IN	DBA1

Pins A9 and W7 are reserved for future functions must not be connected on system, the system must provide a solder pad for these pins. The device design needs to tolerate floating on these pins. A3 must be tied LOW for this configuration.

Blank space indicate no ball is populated at that gridpoint – vias on the module may be located in these areas

Top view for 176-ball TFBGA (back configuration) in Quad Rank Mode
Table 8. Ball Assignment; MIRROR=HIGH, QCSEN=LOW

	1	2	3	4	5	6	7	8	9	10	11
A	QAA13	QAA8	$\overline{\text{QCSEN}}$	VSS	$\overline{\text{RESET}}$	MIRROR	$\overline{\text{ERROUT}}$	VSS	RSVD	QBA8	QBA13
B	QAA14	QAA7								QBA7	QBA14
C	QAA9	QAA6	VDD		VDD	VDD	VDD		VDD	QBA6	QBA9
D	QAA11	QAA5	VSS		VSS	VSS	VSS		VSS	QBA5	QBA11
E	QAA2	QAA4	VDD		VDD	VDD	VDD		VDD	QBA4	QBA2
F	QAA1	QAA3	VSS		VSS	VSS	VSS		VSS	QBA3	QBA1
G	QAA0	QABA1	VDD		VDD	VDD	VDD		VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS		VSS	VSS	VSS		VSS	QBBA0	QBA12
J	QABA2	$\overline{\text{QCS1}}$	VDD		VDD	VDD	VDD		VDD	$\overline{\text{QCS3}}$	QBBA2
K	QAA15	QACKE0	VSS		VSS	VSS	VSS		VSS	QBCKE0	QBA15
L	$\overline{\text{QAWE}}$	QCS0#	VDD		VDD	VDD	VDD		VDD	$\overline{\text{QCS2}}$	$\overline{\text{QBWE}}$
M	QAA10	QACKE1	VSS		VSS	VSS	VSS		VSS	QBCKE1	QBA10
N	$\overline{\text{QACAS}}$	QAODT0	VDD		VDD	VDD	VDD		VDD	QBODT0	$\overline{\text{QBCAS}}$
P	$\overline{\text{QARAS}}$	QAODT1	DA4		VSS	VSS	VSS		DA3	QBODT1	$\overline{\text{QBRAS}}$
R	DODT1	DA10	DA1		DA2	$\overline{\text{DCS3}}$	DA5		DA15	DA14	DCKE1
T	DODT0	$\overline{\text{DCS1}}$								$\overline{\text{DCS0}}$	DCKE0
U	$\overline{\text{DCAS}}$	DA13		$\overline{\text{Y1}}$	PVSS	VDD	PVDD	$\overline{\text{Y0}}$		DBA2	DA12
V	$\overline{\text{DWE}}$	$\overline{\text{DRAS}}$		Y1	PVSS	VSS	PVDD	Y0		DA11	DA9
W	DBA0	DA0	$\overline{\text{FBIN}}$	$\overline{\text{Y3}}$	AVSS	$\overline{\text{CK}}$	RSVD	$\overline{\text{Y2}}$	$\overline{\text{FBOUT}}$	DA6	DA8
Y	DBA1	PAR_IN	FBIN	Y3	AVDD	CK	VREFCA	Y2	FBOUT	$\overline{\text{DCS2}}$	DA7

Pins A9 and W7 are reserved for future functions must not be connected on system, the system must provide a solder pad for these pins. The device design needs to tolerate floating on these pins. A3 must be tied LOW for this configuration.

Blank space indicate no ball is populated at that gridpoint – vias on the module may be located in these areas

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74SSQEA32882ZALR	ACTIVE	NFBGA	ZAL	176	2000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 85	EA32882B	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74SSQEA32882ZALR	NFBGA	ZAL	176	2000	330.0	24.4	8.3	13.8	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

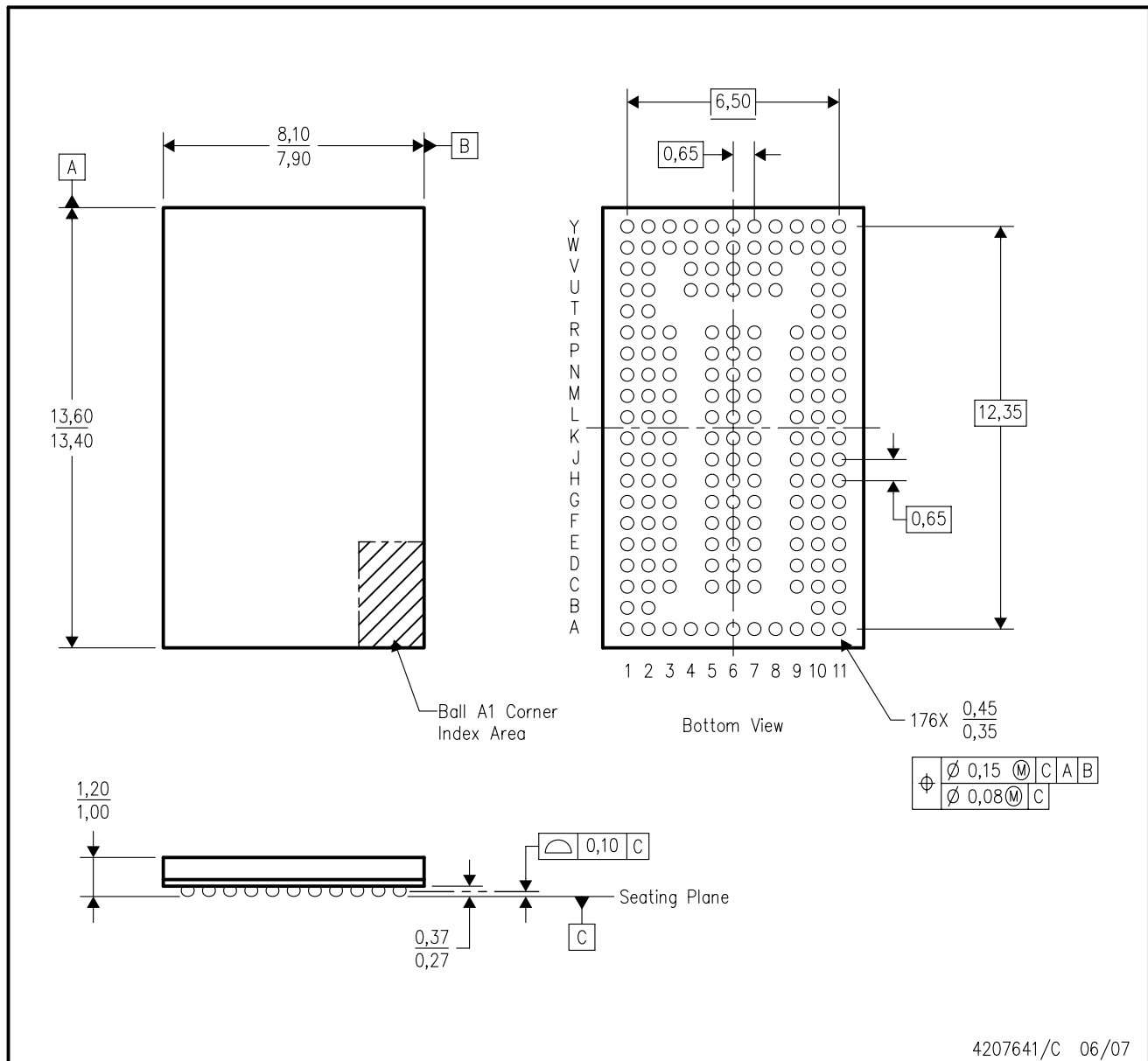


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74SSQEA32882ZALR	NFBGA	ZAL	176	2000	367.0	367.0	38.0

ZAL (R-PBGA-N176)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. This package is lead-free.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Texas Instruments:](#)

[SN74SSQEA32882ZALR](#)