

SN54390, SN54LS390, SN54393, SN54LS393 SN74390, SN74LS390, SN74393, SN74LS393 DUAL 4-BIT DECADE AND BINARY COUNTERS

SDLS107 - OCTOBER 1976 - REVISED MARCH 1988

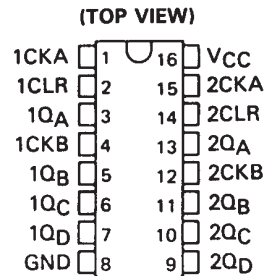
- Dual Versions of the Popular '90A, 'LS90 and '93A, 'LS93
- '390, 'LS390 . . . Individual Clocks for A and B Flip-Flops Provide Dual $\div 2$ and $\div 5$ Counters
- '393, 'LS393 . . . Dual 4-Bit Binary Counter with Individual Clocks
- All Have Direct Clear for Each 4-Bit Counter
- Dual 4-Bit Versions Can Significantly Improve System Densities by Reducing Counter Package Count by 50%
- Typical Maximum Count Frequency . . . 35 MHz
- Buffered Outputs Reduce Possibility of Collector Commutation

description

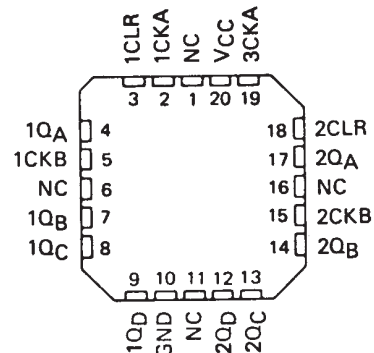
Each of these monolithic circuits contains eight master-slave flip-flops and additional gating to implement two individual four-bit counters in a single package. The '390 and 'LS390 incorporate dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiples of 2 and/or 5 up to divide-by-100. When connected as a bi-quinary counter, the separate divide-by-two circuit can be used to provide symmetry (a square wave) at the final output stage. The '393 and 'LS393 each comprise two independent four-bit binary counters each having a clear and a clock input. N-bit binary counters can be implemented with each package providing the capability of divide-by-256. The '390, 'LS390, '393, and 'LS393 have parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system-timing signals.

Series 54 and Series 54LS circuits are characterized for operation over the full military temperature range of -55°C to 125°C ; Series 74 and Series 74LS circuits are characterized for operation from 0°C to 70°C .

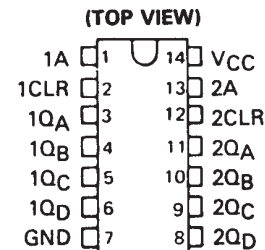
SN54390, SN54LS390 . . . J OR W PACKAGE
SN74390 . . . N PACKAGE
SN74LS390 . . . D OR N PACKAGE



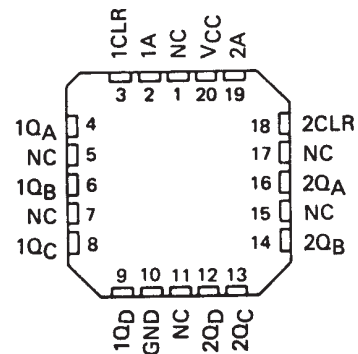
SN54LS390 . . . FK PACKAGE
(TOP VIEW)



SN54393, SN54LS393 . . . J OR W PACKAGE
SN74393 . . . N PACKAGE
SN74LS393 . . . D OR N PACKAGE



SN54LS393 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1988, Texas Instruments Incorporated

SN54390, SN54LS390, SN54393, SN54LS393 SN74390, SN74LS390, SN74393, SN74LS393 DUAL 4-BIT DECADE AND BINARY COUNTERS

SDLS107 - OCTOBER 1976 - REVISED MARCH 1988

**'390, 'LS390
BCD COUNT SEQUENCE
(EACH COUNTER)
(See Note A)**

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

**FUNCTION TABLES
'390, 'LS390
BI-QUINARY (5-2)
(EACH COUNTER)
(See Note B)**

COUNT	OUTPUT			
	Q _A	Q _D	Q _C	Q _B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

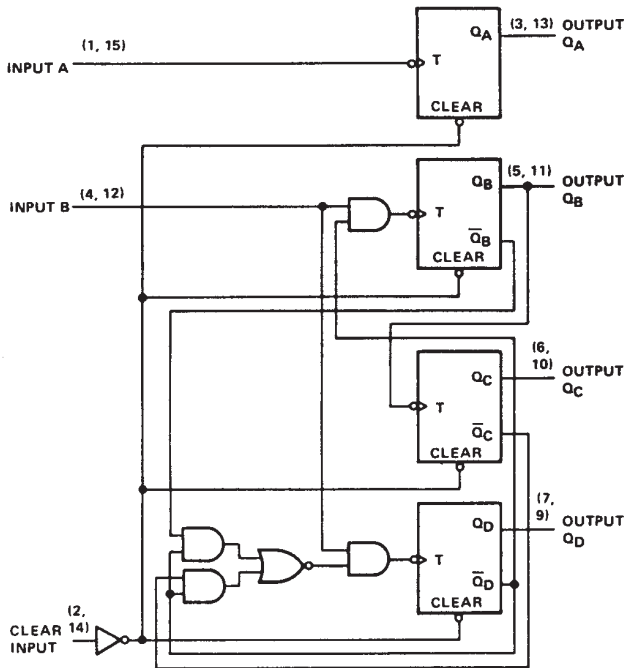
**'393, 'LS393
COUNT SEQUENCE
(EACH COUNTER)**

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTES: A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. H = high level, L = low level.

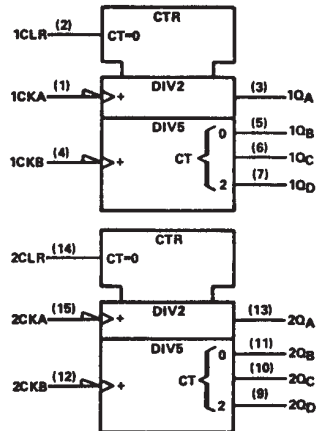
logic diagrams (positive logic)

'390, 'LS390

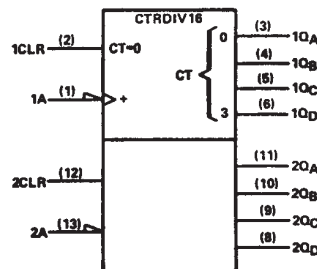


logic symbols †

'390, 'LS390



'393, 'LS393



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

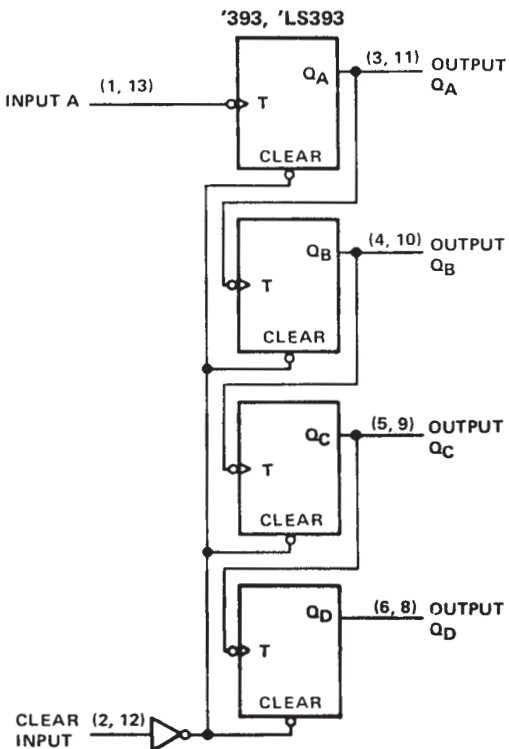


POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54390, SN54LS390, SN54393, SN54LS393
 SN74390, SN74LS390, SN74393, SN74LS393
 DUAL 4-BIT DECADE AND BINARY COUNTERS

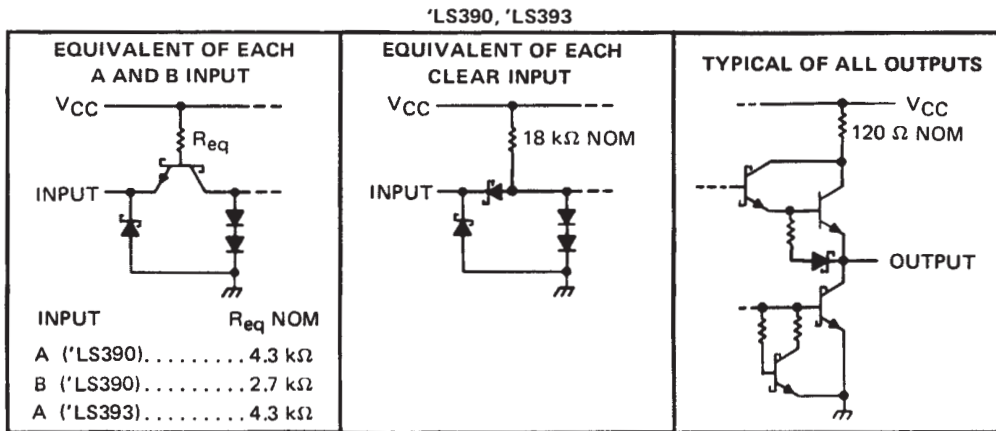
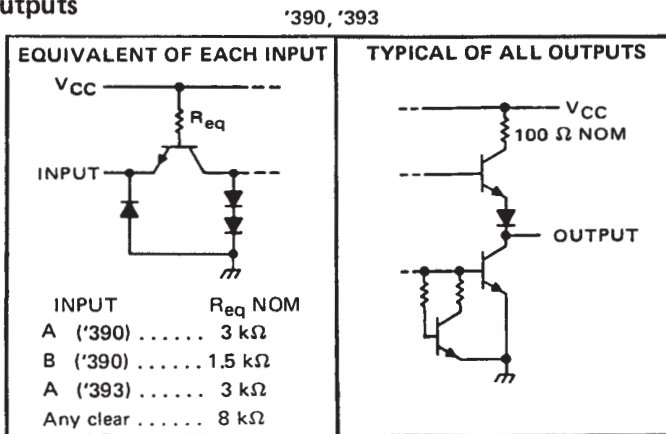
SDLS107 - OCTOBER 1976 - REVISED MARCH 1988

logic diagrams (continued)



Pin numbers shown are for D, J, N and W packages.

schematics of inputs and outputs



SN54390, SN54LS390, SN54393, SN54LS393
SN74390, SN74LS390, SN74393, SN74LS393
DUAL 4-BIT DECADE AND BINARY COUNTERS

SDLS107 – OCTOBER 1976 – REVISED MARCH 1988

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54390, SN54393	-55°C to 125°C
SN74390, SN74393	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54390 SN54393			SN74390 SN74393			UNIT	
	MIN	NOM	MAX	MIN	NOM	MAX		
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V	
High-level output current, I_{OH}			-800			-800	μ A	
Low-level output current, I_{OL}			16			16	mA	
Count frequency, f_{count}	A input		0	25	0		25	MHz
	B input		0	20	0		20	
Pulse width, t_w	A input high or low		20		20		ns	
	B input high or low		25		25			
	Clear high		20		20			
Clear inactive-state setup time, t_{SU}	25↓		25↓				ns	
Operating free-air temperature, T_A	-55		125		0		70	°C

↓ The arrow indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	'390			'393			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage		0.8			0.8			V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$	-1.5			-1.5			V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA} \uparrow$		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$	1			1			mA
I_{IH} High-level input current	Clear	40			40			μ A
	Input A	80			80			
	Input B	120						
I_{IL} Low-level input current	Clear	-1			-1			mA
	Input A	-3.2			-3.2			
	Input B	-4.8						
I_{OS} Short-circuit output current §	$V_{CC} = \text{MAX}$	SN54'	-20	-57	-20	-57	mA	
		SN74'	-18	-57	-18	-57		
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$	42	69		38	64	mA	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

¶ The Q_A outputs of the '390 are tested at $I_{OL} = 16 \text{ mA}$ plus the limit value for I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

NOTE 2: I_{CC} is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.



SN54390, SN54LS390, SN54393, SN54LS393
 SN74390, SN74LS390, SN74393, SN74LS393
 DUAL 4-BIT DECADE AND BINARY COUNTERS

SDLS107 – OCTOBER 1976 – REVISED MARCH 1988

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

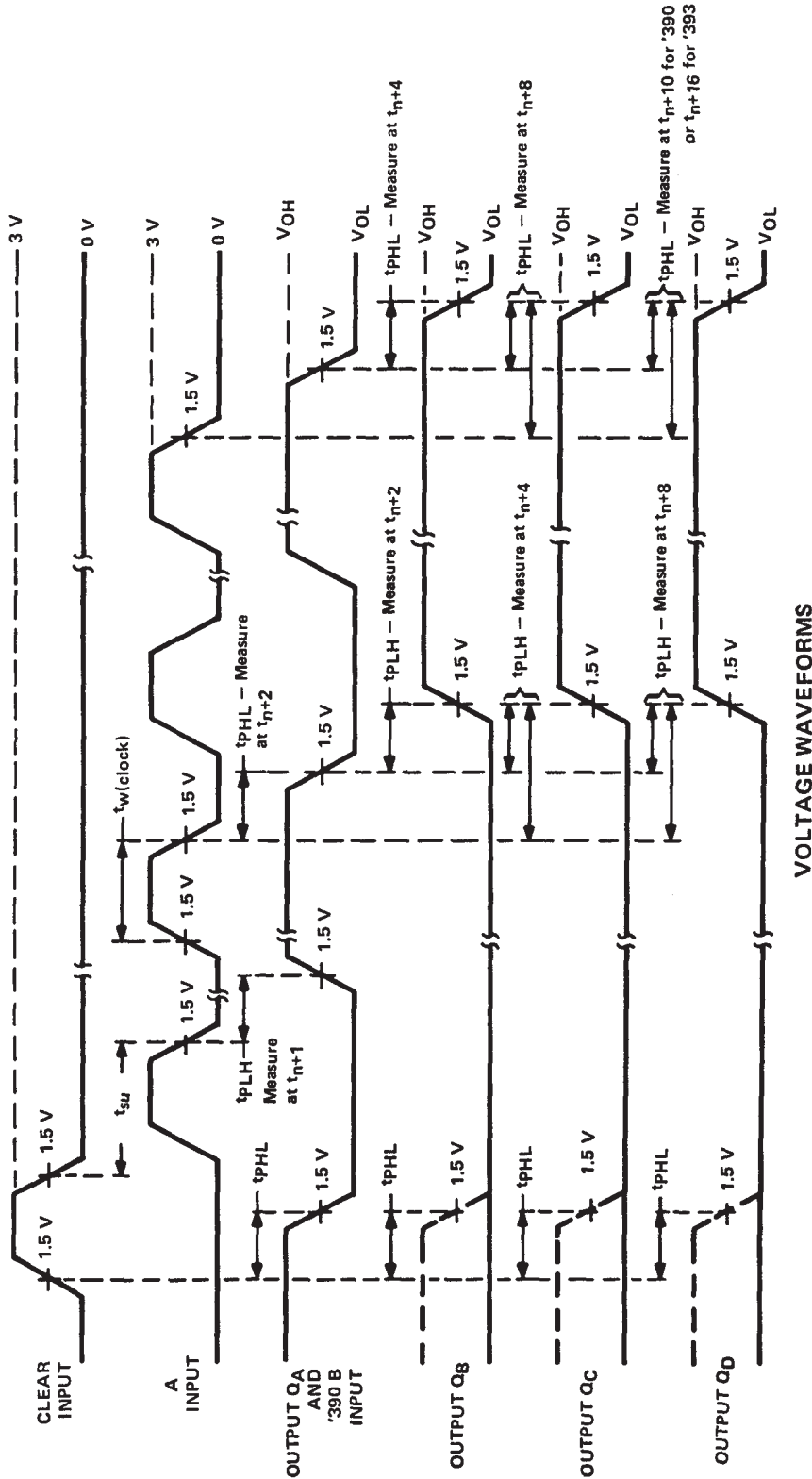
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'390			'393			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{\max}	A	Q_A	$C_L = 15\text{ pF}$, $R_L = 400\ \Omega$, See Note 3 and Figure 1	25	35		25	35	MHz	
	B	Q_B		20	30					
t_{PLH}	A	Q_A		12	20		12	20	ns	
t_{PHL}				13	20		13	20		
t_{PLH}	A	Q_C of '390 Q_D of '393		37	60		40	60	ns	
t_{PHL}				39	60		40	60		
t_{PLH}	B	Q_B		13	21				ns	
t_{PHL}				14	21					
t_{PLH}	B	Q_C		24	39				ns	
t_{PHL}				26	39					
t_{PLH}	B	Q_D		13	21				ns	
t_{PHL}				14	21					
t_{PHL}	Clear	Any		24	39		24	39	ns	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

SN54390, SN54LS390, SN54393, SN54LS393
 SN74390, SN74LS390, SN74393, SN74LS393
 DUAL 4-BIT DECADE AND BINARY COUNTERS

SDLS107 - OCTOBER 1976 - REVISED MARCH 1988

PARAMETER MEASUREMENT INFORMATION



NOTE A: Input pulses are supplied by a generator having the following characteristics $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms.

FIGURE 1



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54390, SN54LS390, SN54393, SN54LS393 SN74390, SN74LS390, SN74393, SN74LS393 DUAL 4-BIT DECADE AND BINARY COUNTERS

SDLS107 – OCTOBER 1976 – REVISED MARCH 1988

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Clear input voltage	7 V
Any A or B clock input voltage	5.5 V
Operating free-air temperature range: SN54LS390, SN54LS393	-55°C to 125°C
SN74LS390, SN74LS393	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS390 SN54LS393			SN74LS390 SN74LS393			UNIT	
	MIN	NOM	MAX	MIN	NOM	MAX		
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V	
High-level output current, I_{OH}	-400			-400			μ A	
Low-level output current, I_{OL}	4			8			mA	
Count frequency, f_{count}	A input		0	25	0		25	MHz
	B input		0	12.5	0		12.5	
Pulse width, t_w	A input high or low		20		20		ns	
	B input high or low		40		40			
	Clear high		20		20			
Clear inactive-state setup time, t_{SU}	25 \downarrow			25 \downarrow			ns	
Operating free-air temperature, T_A	-55		125	0		70	°C	

\downarrow The arrow indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54LS'			SN74LS'			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage		0.7			0.8			V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$	-1.5			-1.5			V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V},$	$I_{OL} = 4 \text{ mA}$ [¶]		0.25	0.4	0.25	0.4	V
		$I_{OL} = 8 \text{ mA}$ [¶]				0.35	0.5	
I_I Input current at maximum input voltage	Clear	$V_I = 7 \text{ V}$		0.1		0.1		mA
	Input A	$V_{CC} = \text{MAX}$		0.2		0.2		
	Input B	$V_I = 5.5 \text{ V}$		0.4		0.4		
I_{IH} High-level input current	Clear			0.02		0.02		mA
	Input A	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		0.1		0.1		
	Input B			0.2		0.2		
I_{IL} Low-level input current	Clear			-0.4		-0.4		mA
	Input A	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-1.6		-1.6		
	Input B			-2.4		-2.4		
I_{OS} Short-circuit output current [§]	$V_{CC} = \text{MAX}$	-20	-100	-20	-100			mA
I_{CC} Supply current	$V_{CC} = \text{MAX},$ See Note 2	'LS390		15	26	15	26	mA
		'LS393		15	26	15	26	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

[§] Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

[¶] The Q_A outputs of the 'LS390 are tested at $I_{OL} = \text{MAX}$ plus the limit value for I_{IL} for the clock B input. This permits driving the clock B input while maintaining full fan-out capability.

NOTE 2: I_{CC} is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.



**SN54390, SN54LS390, SN54393, SN54LS393
 SN74390, SN74LS390, SN74393, SN74LS393
 DUAL 4-BIT DECADE AND BINARY COUNTERS**

SDLS107 – OCTOBER 1976 – REVISED MARCH 1988

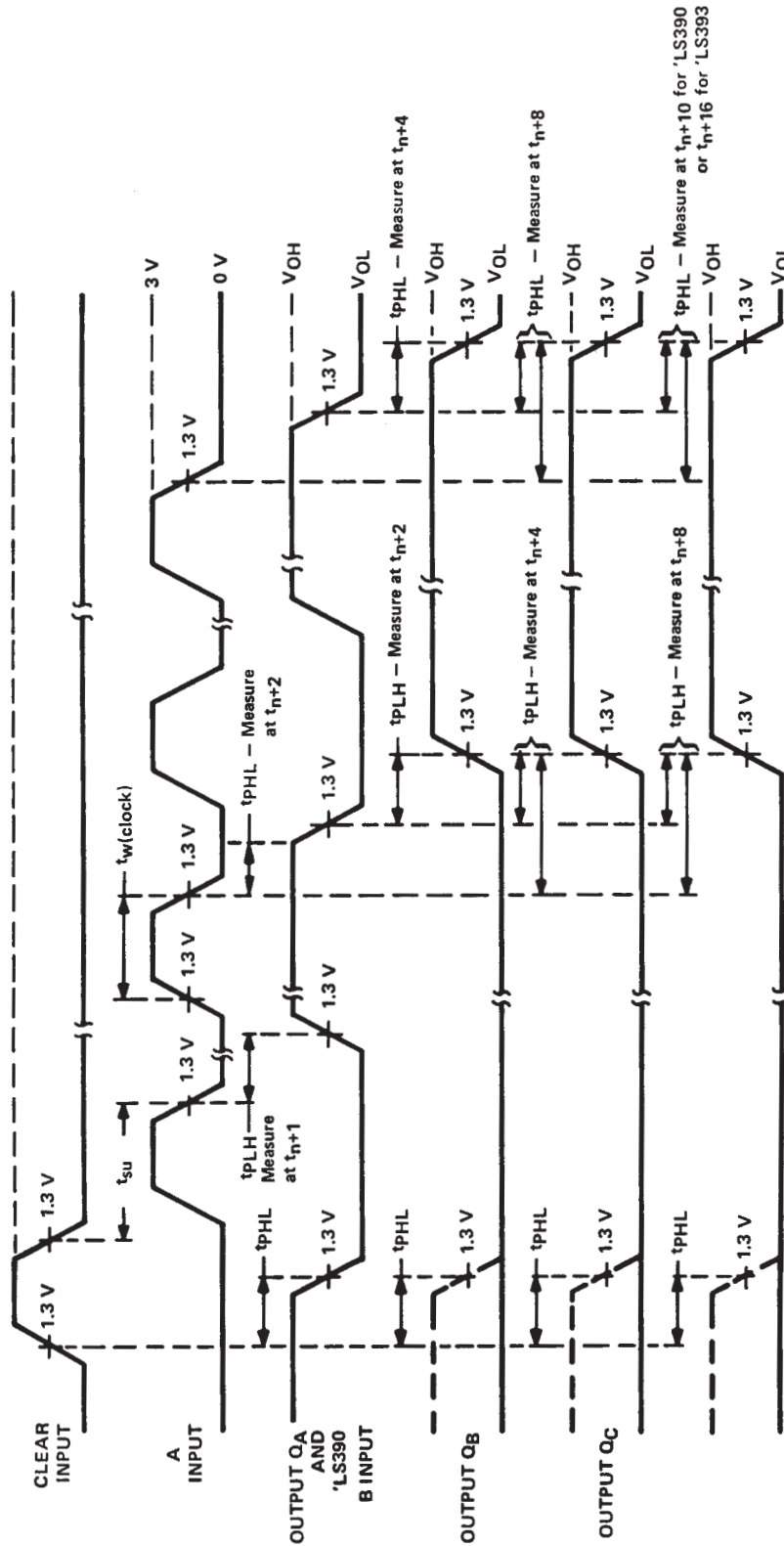
switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS390			'LS393			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	A	Q_A	$C_L = 15\text{ pF}$, $R_L = 2\text{ k}\Omega$, See Note 4 and Figure 2	25	35		25	35	MHz	
	B	Q_B		12.5	20					
t_{PLH}	A	Q_A		12	20		12	20	ns	
t_{PHL}				13	20		13	20		
t_{PLH}	A	Q_C of 'LS390 Q_D of 'LS393		37	60		40	60	ns	
t_{PHL}				39	60		40	60		
t_{PLH}	B	Q_B		13	21				ns	
t_{PHL}				14	21					
t_{PLH}	B	Q_C		24	39				ns	
t_{PHL}				26	39					
t_{PLH}	B	Q_D		13	21				ns	
t_{PHL}				14	21					
t_{PHL}	Clear	Any		24	39		24	39	ns	

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.



PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTE A: Input pulses are supplied by a generator having the following characteristics $t_r \leq 15$ ns, $t_f \leq 6$ ns, PRR = 1 MHz, duty cycle = 50 %, $Z_{out} \approx 50$ ohms.

FIGURE 2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
7802601EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7802601EA SNJ54LS390J	Samples
7802601FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7802601FA SNJ54LS390W	Samples
7802601FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7802601FA SNJ54LS390W	Samples
JM38510/32701B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32701B2A	Samples
JM38510/32701B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32701B2A	Samples
JM38510/32701BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32701BEA	Samples
JM38510/32701BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32701BEA	Samples
JM38510/32702B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32702B2A	Samples
JM38510/32702B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32702B2A	Samples
JM38510/32702BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32702BCA	Samples
JM38510/32702BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32702BCA	Samples
JM38510/32702BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32702BDA	Samples
JM38510/32702BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32702BDA	Samples
JM38510/32702SDA	ACTIVE	CFP	W	14	25	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32702SDA SNV54LS393W	Samples
JM38510/32702SDA	ACTIVE	CFP	W	14	25	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32702SDA SNV54LS393W	Samples
M38510/32701B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32701B2A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
M38510/32701B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32701B2A	Samples
M38510/32701BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32701BEA	Samples
M38510/32701BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32701BEA	Samples
M38510/32702B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32702B2A	Samples
M38510/32702B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 32702B2A	Samples
M38510/32702BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32702BCA	Samples
M38510/32702BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32702BCA	Samples
M38510/32702BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32702BDA	Samples
M38510/32702BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32702BDA	Samples
M38510/32702SDA	ACTIVE	CFP	W	14	25	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32702SDA SNV54LS393W	Samples
M38510/32702SDA	ACTIVE	CFP	W	14	25	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 32702SDA SNV54LS393W	Samples
SN54LS390J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS390J	Samples
SN54LS390J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS390J	Samples
SN54LS393J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS393J	Samples
SN54LS393J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS393J	Samples
SN74LS390D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS390	Samples
SN74LS390D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS390	Samples
SN74LS390N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS390N	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS390N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS390N	Samples
SN74LS390NE4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS390N	Samples
SN74LS390NE4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS390N	Samples
SN74LS390NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS390	Samples
SN74LS390NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS390	Samples
SN74LS393D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS393	Samples
SN74LS393D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS393	Samples
SN74LS393DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS393	Samples
SN74LS393DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS393	Samples
SN74LS393N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS393N	Samples
SN74LS393N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS393N	Samples
SN74LS393NE4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS393N	Samples
SN74LS393NE4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS393N	Samples
SN74LS393NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS393	Samples
SN74LS393NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS393	Samples
SNJ54LS390FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54LS390FK	Samples
SNJ54LS390FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54LS390FK	Samples
SNJ54LS390J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7802601EA SNJ54LS390J	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54LS390J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7802601EA SNJ54LS390J	Samples
SNJ54LS390W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7802601FA SNJ54LS390W	Samples
SNJ54LS390W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7802601FA SNJ54LS390W	Samples
SNJ54LS393FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54LS 393FK	Samples
SNJ54LS393FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54LS 393FK	Samples
SNJ54LS393J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS393J	Samples
SNJ54LS393J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS393J	Samples
SNJ54LS393W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS393W	Samples
SNJ54LS393W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54LS393W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LS390, SN54LS393, SN54LS393-SP, SN74LS390, SN74LS393 :

- Catalog: [SN74LS390](#), [SN74LS393](#), [SN54LS393](#)
- Military: [SN54LS390](#), [SN54LS393](#)
- Space: [SN54LS393-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS390NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LS393DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS393NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

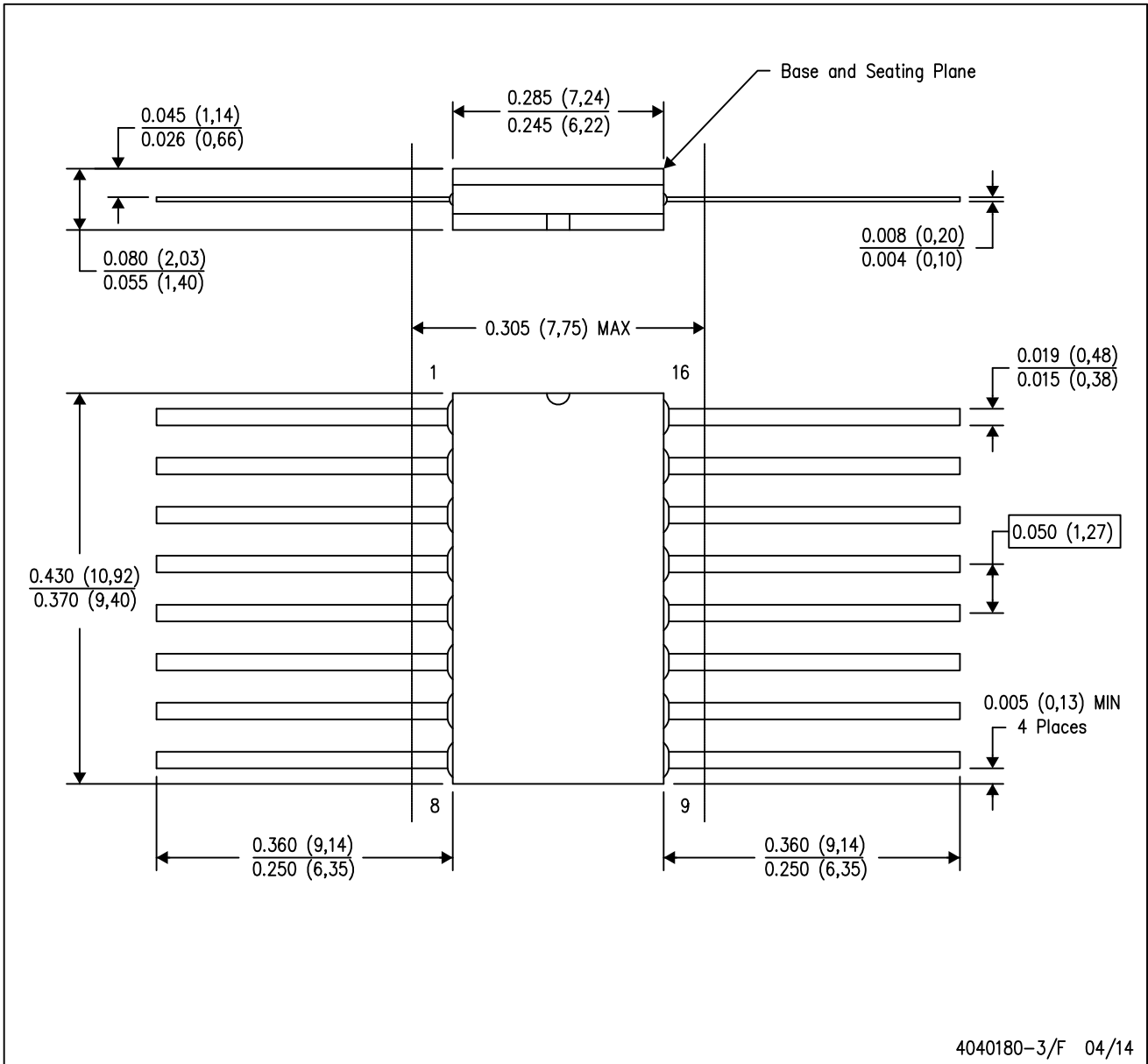
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS390NSR	SO	NS	16	2000	367.0	367.0	38.0
SN74LS393DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74LS393NSR	SO	NS	14	2000	367.0	367.0	38.0

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP2-F16

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



4040180-2/F 04/14

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Texas Instruments:

[SN74LS390N](#) [SN74LS390D](#) [SN74LS390DR](#) [SN74LS390DRE4](#) [SN74LS390NE4](#) [SN74LS390NSR](#)
[SN74LS390DG4](#) [SN74LS390DRG4](#)