



SN74AHC1G14 Single Schmitt-Trigger Inverter Gate

1 Features

- Operating Range 2 V to 5.5 V
- Maximum t_{pd} of 10 ns at 5 V
- Low Power Consumption, 10- μ A Max I_{CC}
- ± 8 -mA Output Drive at 5 V
- Latch-Up Performance Exceeds 250 mA Per JEDEC 17

2 Applications

- Barcode Scanners
- Cable Solutions
- E-Books
- Embedded PCs
- Field Transmitter: Temperature or Pressure Sensors
- Fingerprint Biometrics
- HVAC: Heating, Ventilating, and Air Conditioning
- Network-Attached Storage (NAS)
- Server Motherboard and PSU
- Software Defined Radios (SDR)
- TV: High Definition (HDTV), LCD, and Digital
- Video Communications Systems
- Wireless Data Access Cards, Headsets, Keyboards, Mice, and LAN Cards

3 Description

The SN74AHC1G14 device is a single inverter gate. The device performs the Boolean function $Y = \bar{A}$.

The device functions as an independent inverter gate, but because of the Schmitt action, gates may have different input threshold levels for positive- (V_{T+}) and negative-going (V_{T-}) signals.

Device Information

ORDER NUMBER	PACKAGE (PIN)	BODY SIZE (NOM)
SN74AHC1G14DBV	SOT-23 (5)	2.90 mm \times 1.60 mm
SN74AHC1G14DCK	SC70 (5)	2.00 mm \times 1.25 mm
SN74AHC1G14DRL	SOT (5)	1.60 mm \times 1.20 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Side)



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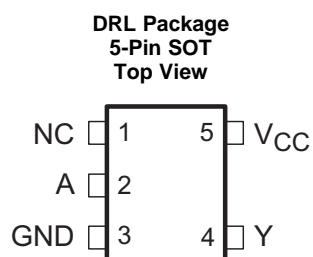
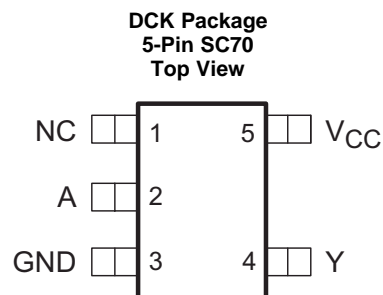
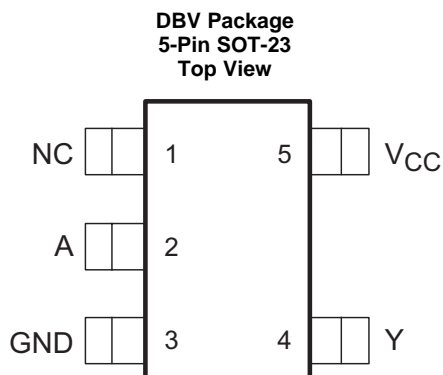
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision P (August 2013) to Revision Q	Page
<ul style="list-style-type: none"> Added <i>Applications</i> section, <i>Device Information</i> table, <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Typical Characteristics</i> section, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section 	1
Changes from Revision O (May 2013) to Revision P	Page
<ul style="list-style-type: none"> Updated document to new TI data sheet format - no specification changes 	1
Changes from Revision N (June 2005) to Revision O	Page
<ul style="list-style-type: none"> Changed document format from Quicksilver to DocZone. 	1

5 Pin Configuration and Functions



Pin Functions⁽¹⁾

PIN		I/O	DESCRIPTION
NO.	NAME		
1	NC	—	No connect
2	A	I	Data Input
3	GND	—	Ground
4	Y	O	Data Output
5	VCC	—	Power

(1) NC – No internal connection.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage		−0.5	7	V
V_I	Input voltage ⁽²⁾		−0.5	7	V
V_O	Output voltage ⁽²⁾		−0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$		−20	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_j	Maximum junction temperature			150	°C
T_{stg}	Storage temperature		−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2$ V		−50	μA
		$V_{CC} = 3.3$ V ± 0.3 V		−4	mA
		$V_{CC} = 5$ V ± 0.5 V		−8	
I_{OL}	Low-level output current	$V_{CC} = 2$ V		50	μA
		$V_{CC} = 3.3$ V ± 0.3 V		4	mA
		$V_{CC} = 5$ V ± 0.5 V		8	
T_A	Operating free-air temperature		−40	125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74AHC1G14			UNIT
		DBV (SOT-23)	DCK (SC70)	DRL (SOT)	
		5 PINS	5 PINS	5 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	225.7	252	271.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	160.3	—	116.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	59.4	—	89.9	°C/W
ψ _{JT}	Junction-to-top characterization parameter	41.0	—	17.3	°C/W
ψ _{JB}	Junction-to-board characterization parameter	58.7	—	89.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = –40°C to 85°C			RECOMMENDED T _A = –40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V _{T+} Positive-going input threshold voltage		3 V	1.2		2.2	1.2		2.2	1.2		2.2	V
		4.5 V	1.75		3.15	1.75		3.15	1.75		3.15	
		5.5 V	2.15		3.85	2.15		2.85	2.15		3.85	
V _{T–} Negative-going input threshold voltage		3 V	0.9		1.9	0.9		1.9	0.9		1.9	V
		4.5 V	1.35		2.75	1.35		2.75	1.35		2.75	
		5.5 V	1.65		3.35	1.65		3.35	1.65		3.35	
ΔV _T Hysteresis (V _{T+} – V _{T–})		3 V	0.3		1.2	0.3		1.2	0.25		1.2	V
		4.5 V	0.4		1.4	0.4		1.4	0.35		1.4	
		5.5 V	0.5		1.6	0.5		1.6	0.45		1.6	
V _{OH}	I _{OH} = –50 μA	2 V	1.9	2		1.9			1.9			V
		3 V	2.9	3		2.9			2.9			
		4.5 V	4.4	4.5		4.4			4.4			
	I _{OH} = –4 mA	3 V	2.58			2.48			2.4			
	I _{OL} = –8 mA	4.5 V	3.94			3.8			3.7			
V _{OL}	I _{OH} = 50 μA	2 V			0.1			0.1			0.1	V
		3 V			0.1			0.1			0.1	
		4.5 V			0.1			0.1			0.1	
	I _{OH} = 4 mA	3 V			0.36			0.44			0.55	
	I _{OL} = 8 mA	4.5 V			0.36			0.44			0.55	
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1			±1			±1	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			1			10			10	μA
C _i	V _I = V _{CC} or GND	5 V		2	10			10			10	pF

SN74AHC1G14

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6.6 Switching Characteristics, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	$T_A = 25^\circ\text{C}$		$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		RECOMMENDED $T_A = -40^\circ\text{C to } 125^\circ\text{C}$		UNIT
				TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	$C_L = 15 \text{ pF}$	8.3	12.8	1	15	1	16	ns
t_{PHL}				8.3	12.8	1	15	1	16	ns
t_{PLH}	A	Y	$C_L = 50 \text{ pF}$	10.8	16.3	1	18.5	1	19.5	ns
t_{PHL}				10.8	16.3	1	18.5	1	19.5	ns

6.7 Switching Characteristics, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

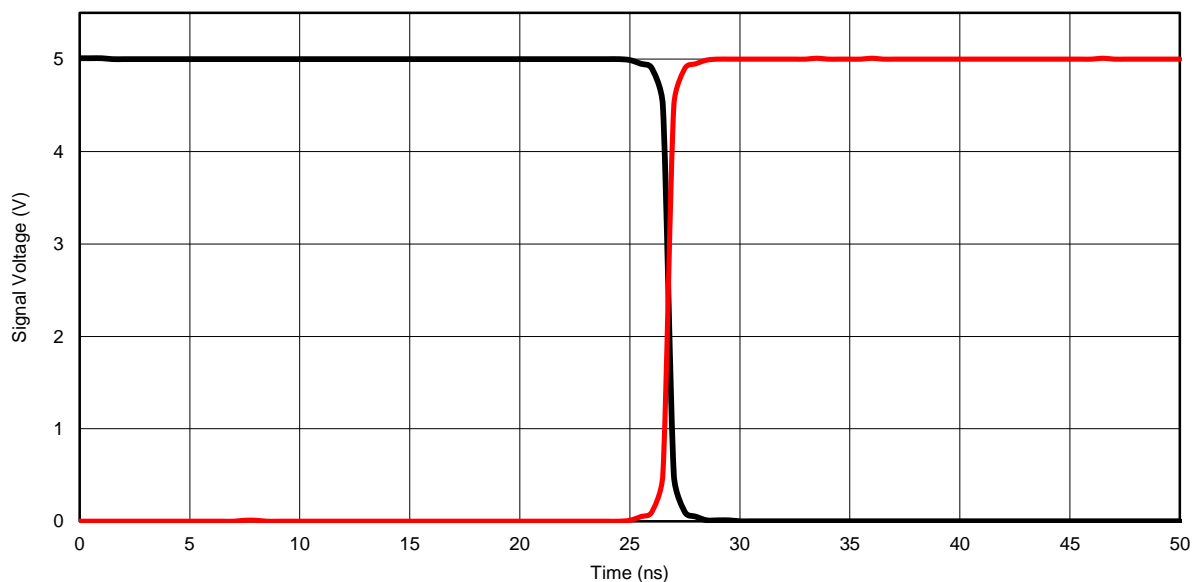
PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	$T_A = 25^\circ\text{C}$		$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		RECOMMENDED $T_A = -40^\circ\text{C to } 125^\circ\text{C}$		UNIT
				TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	$C_L = 15 \text{ pF}$	5.5	8.6	1	10	1	11	ns
t_{PHL}				5.5	8.6	1	10	1	11	ns
t_{PLH}	A or B	Y	$C_L = 50 \text{ pF}$	7	10.6	1	12	1	11	ns
t_{PHL}				7	10.6	1	12	1	11	ns

6.8 Operating Characteristics

$V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	$f = 1 \text{ MHz}$	9	pF

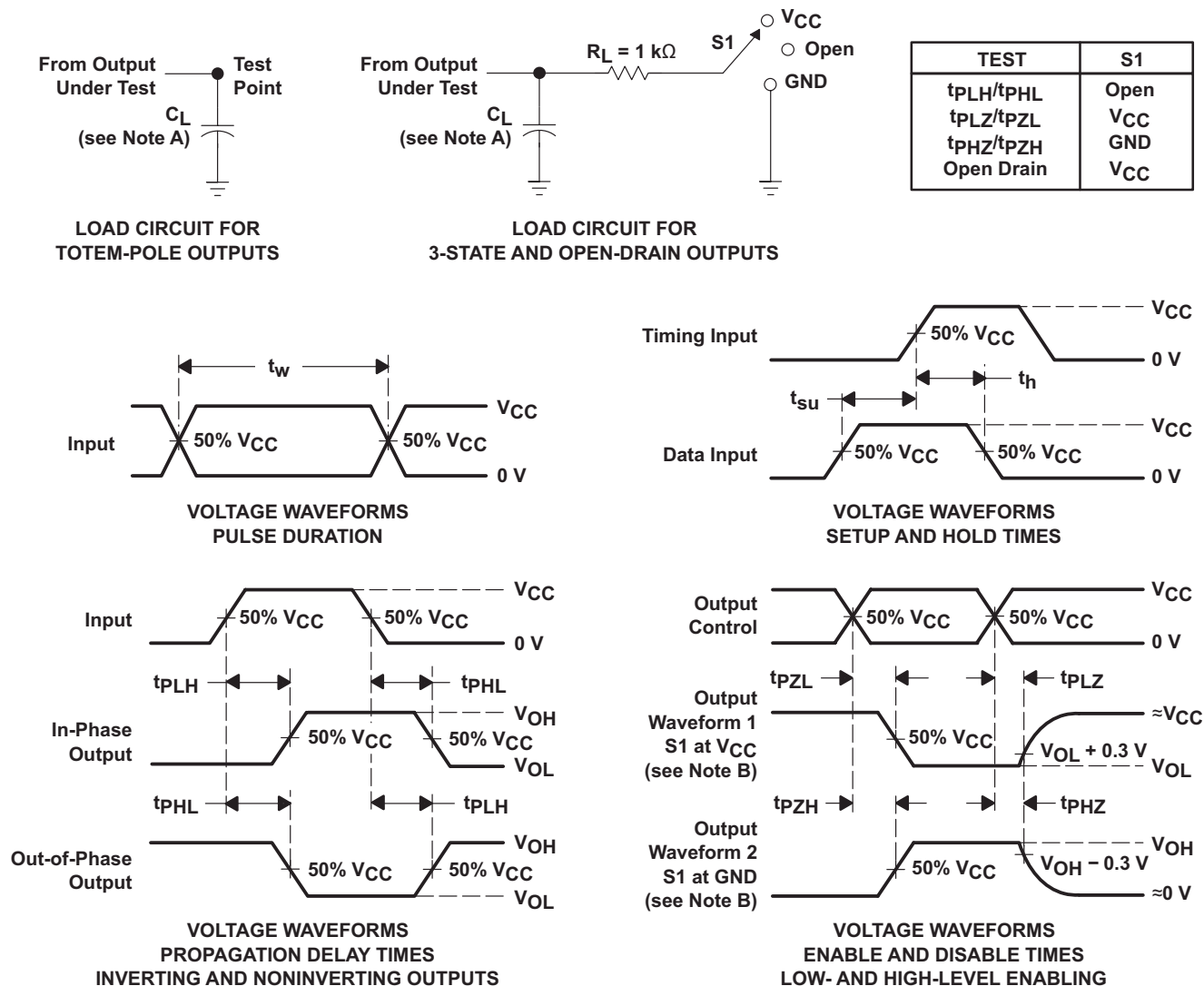
6.9 Typical Characteristics



$T_A = 25^\circ\text{C}$, $V_A = 5 \text{ V}$

Figure 1. Response Time vs Output Voltage

7 Parameter Measurement Information



- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
- The outputs are measured one at a time with one input transition per measurement.
- All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74AHC1G14 device is a single inverter gate. The device performs the Boolean function $Y = \bar{A}$.

The device functions as an independent inverter gate, but because of the Schmitt action, gates may have different input threshold levels for positive- (V_{T+}) and negative-going (V_{T-}) signals.

8.2 Functional Block Diagram

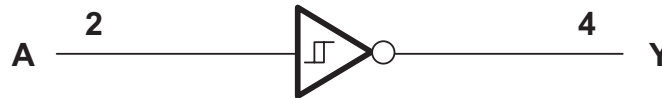


Figure 3. Logic Diagram (Positive Side)

8.3 Feature Description

The SN74AHC1G14 device has a wide operating V_{CC} range of 2 V to 5.5 V, which allows it to be used in a broad range of systems. The low propagation delay allows fast switching and higher speeds of operation. In addition, the low-power consumption makes this device a good choice for portable and battery power-sensitive applications.

8.4 Device Functional Modes

[Table 1](#) lists the functional modes for SN74AHC1G14.

Table 1. Function Table

INPUT A	OUTPUT Y
H	L
L	H

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Physically interactive interface elements like push buttons or rotary knobs offer simple and easy ways to interact with an electronic system. Many of these physical interface elements often have issues with bouncing, or where the physical conductive contact can connect and disconnect multiple times during a button push or release. This bouncing can cause one or more faulty transient signals to be passed during this transitional period. These faulty signals can be observed in many common applications, for example, a television remote with bouncing error can adjust the TV channel multiple times despite the button being pushed only once. To mitigate these faulty signals, we can use a Schmitt-trigger, or a device with hysteresis, to remove these faulty signals. Hysteresis allows a device to *remember* its history, and in this case, the SN74AHC1G14 uses this memory to debounce the signal of the physical element, or filter the faulty transient signals and pass only the valid signal each time the element is used. In this example, we show a push-button signal passed through an SN74AHC1G14 that is debounced and inverted to the microprocessor for push detection.

9.2 Typical Application

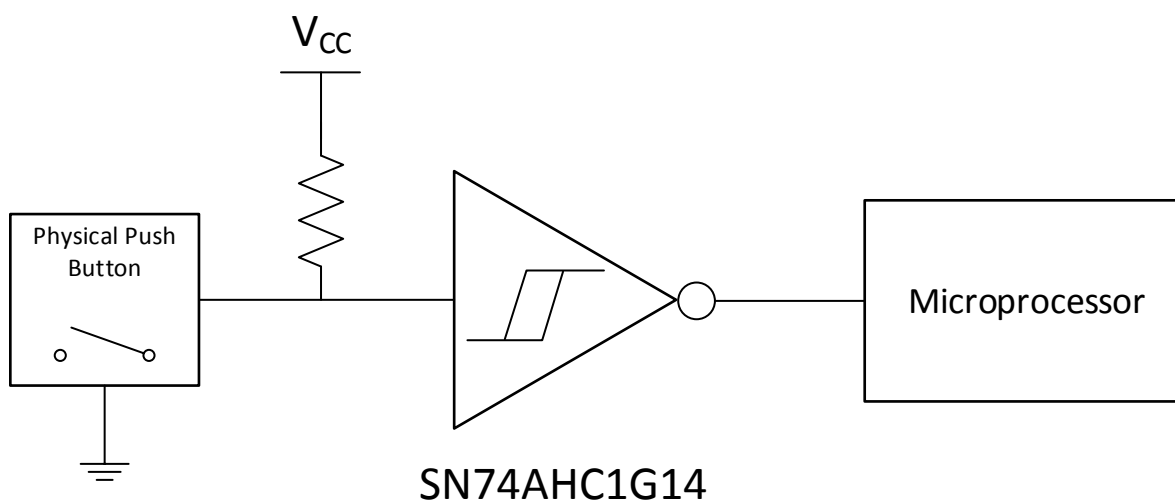


Figure 4. Switch Debouncer

9.2.1 Design Requirements

The SN74AHC1G14 device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The SN74AHC1G14 allows for performing logical Boolean functions with hysteresis using digital signals. All input signals must remain as close as possible to either 0 V or VCC for optimal operation.

Typical Application (continued)

9.2.2 Detailed Design Procedure

1. Recommended input conditions:
 - For rise time and fall time specifications, see $\Delta t/\Delta v$ in the [Recommended Operating Conditions](#) table.
 - For specified high and low levels, see V_{IH} and V_{IL} in the [Recommended Operating Conditions](#) table.
 - Inputs and outputs are overvoltage tolerant and can therefore go as high as 5.5 V at any valid V_{CC} .
2. Recommended output conditions:
 - Load currents must not exceed ± 50 mA.
3. Frequency selection criterion:
 - The effects of frequency upon the power consumption of the device can be studied in *CMOS Power Consumption and CPD Calculation*, [SCAA035](#).
 - Added trace resistance and capacitance can reduce maximum frequency capability; follow the layout practices listed in the [Layout Guidelines](#) section.

9.2.3 Application Curves

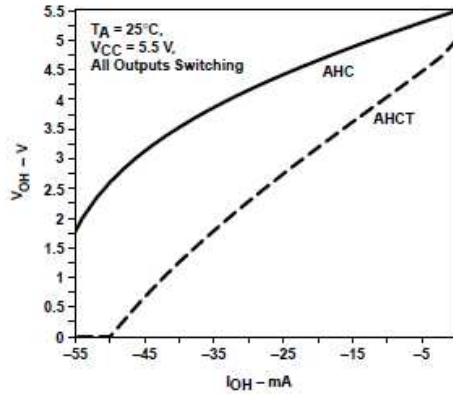

 $V_{CC} = 5.5$ V

Figure 5. AHC Family V_{OH} vs I_{OH}

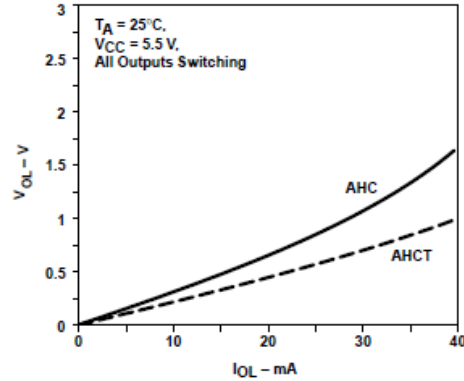

 $V_{CC} = 5.5$ V

Figure 6. AHC Family V_{OL} vs I_{OL}

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the [Recommended Operating Conditions](#) table.

Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- μ F bypass capacitor is recommended. If multiple pins are labeled V_{CC} , then a 0.01- μ F or 0.022- μ F capacitor is recommended for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD} , a 0.1- μ F bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 μ F and 1 μ F are commonly used in parallel. The bypass capacitor must be installed as close as possible to the power terminal for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace, which results in the reflection. Not all PCB traces can be straight; therefore some traces must turn corners. [Figure 7](#) shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

11.2 Layout Example

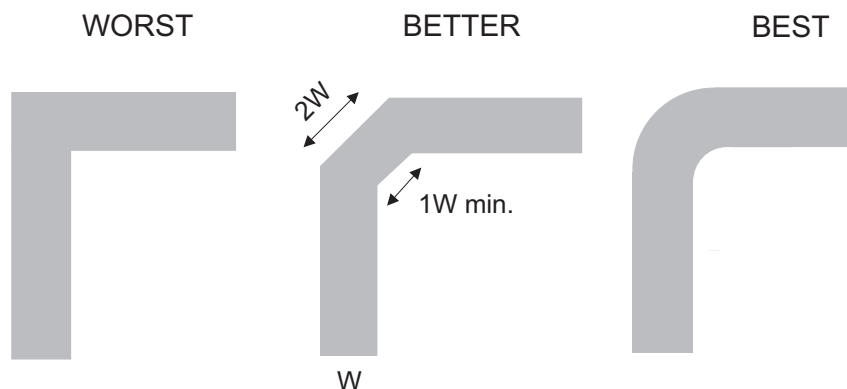


Figure 7. Trace Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#)
- *CMOS Power Consumption and CPD Calculation*, [SCAA035](#)
- *Selecting the Right Texas Instruments Signal Switch*, [SZZA030](#)

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC1G14DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(A143, A14G, A14J, A14L, A14S)	Samples
SN74AHC1G14DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	A14G	Samples
SN74AHC1G14DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	A14G	Samples
SN74AHC1G14DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(A143, A14G, A14L, A14S)	Samples
SN74AHC1G14DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 125	(AF3, AFG, AFJ, AF L, AFS)	Samples
SN74AHC1G14DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(AF3, AFG, AFJ, AF L, AFS)	Samples
SN74AHC1G14DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AF3	Samples
SN74AHC1G14DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 125	(AF3, AFG, AFJ, AF L, AFS)	Samples
SN74AHC1G14DCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(AF3, AFG, AFJ, AF L, AFS)	Samples
SN74AHC1G14DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AF3	Samples
SN74AHC1G14DRLR	ACTIVE	SOT-5X3	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AFS	Samples
SN74AHC1G14DRLRG4	ACTIVE	SOT-5X3	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AFS	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

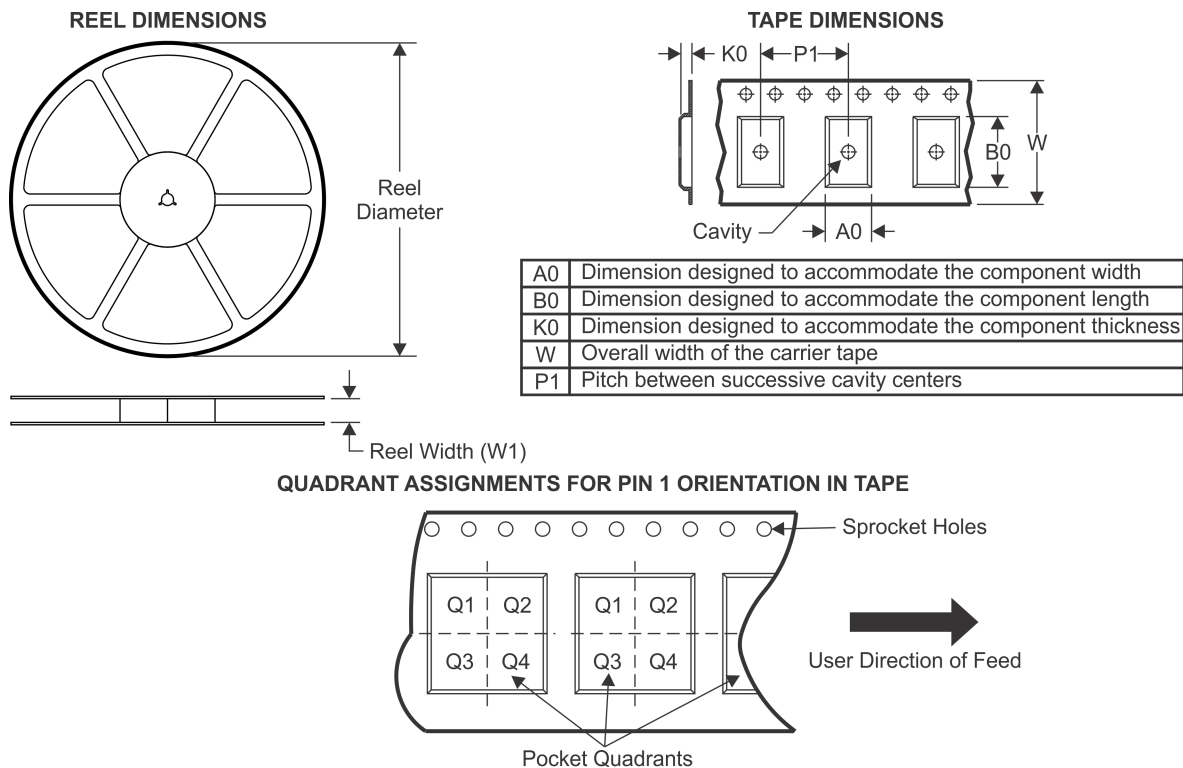
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC1G14DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHC1G14DBVR	SOT-23	DBV	5	3000	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74AHC1G14DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHC1G14DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHC1G14DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHC1G14DBVT	SOT-23	DBV	5	250	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74AHC1G14DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHC1G14DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AHC1G14DCKRG4	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHC1G14DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AHC1G14DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHC1G14DCKT	SC70	DCK	5	250	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74AHC1G14DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

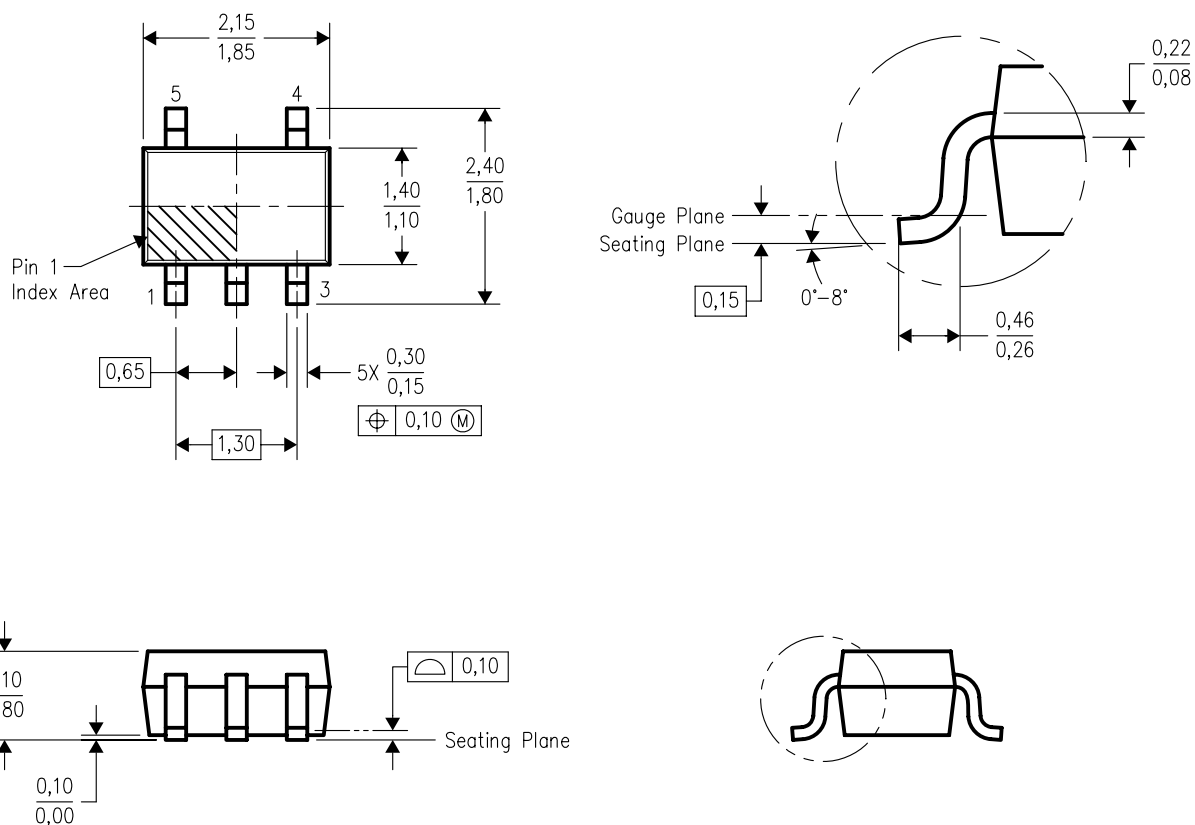


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC1G14DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AHC1G14DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AHC1G14DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AHC1G14DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AHC1G14DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74AHC1G14DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74AHC1G14DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AHC1G14DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AHC1G14DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AHC1G14DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AHC1G14DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AHC1G14DCKT	SC70	DCK	5	250	205.0	200.0	33.0
SN74AHC1G14DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE

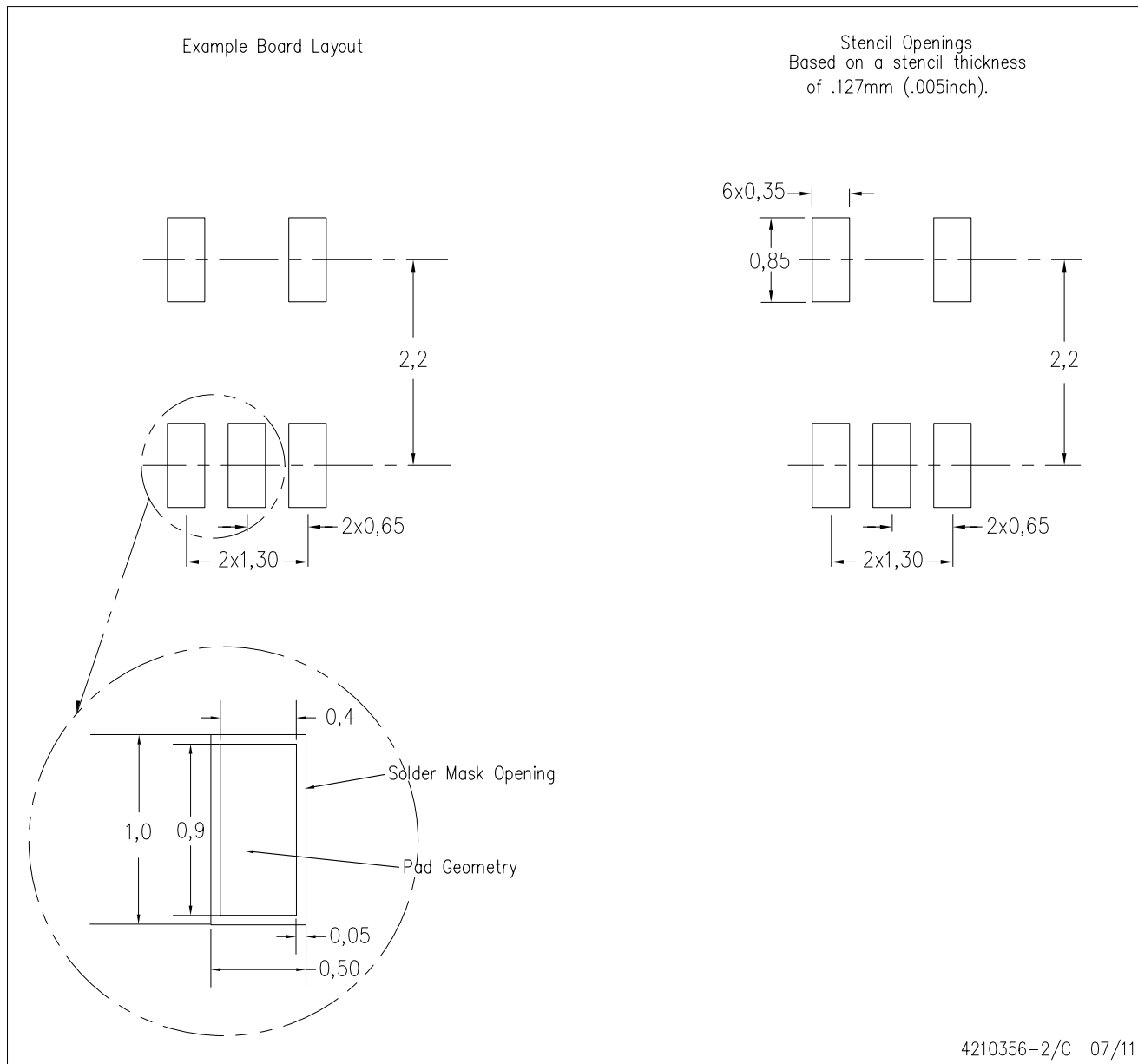


4093553-3/G 01/2007

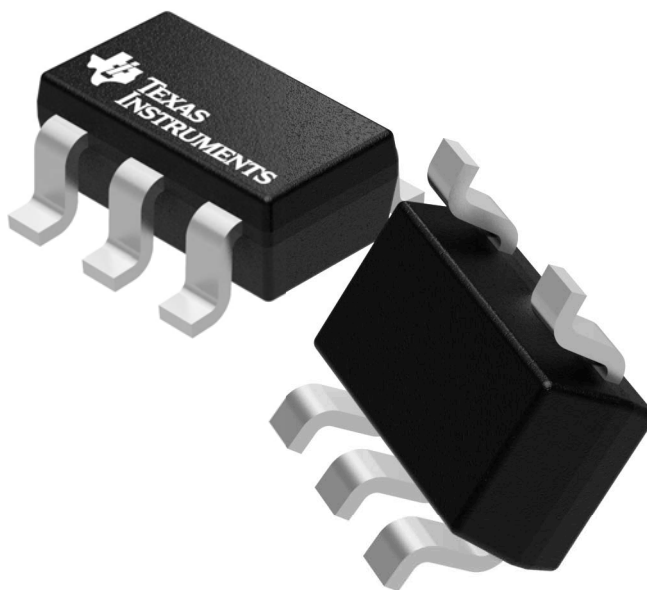
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

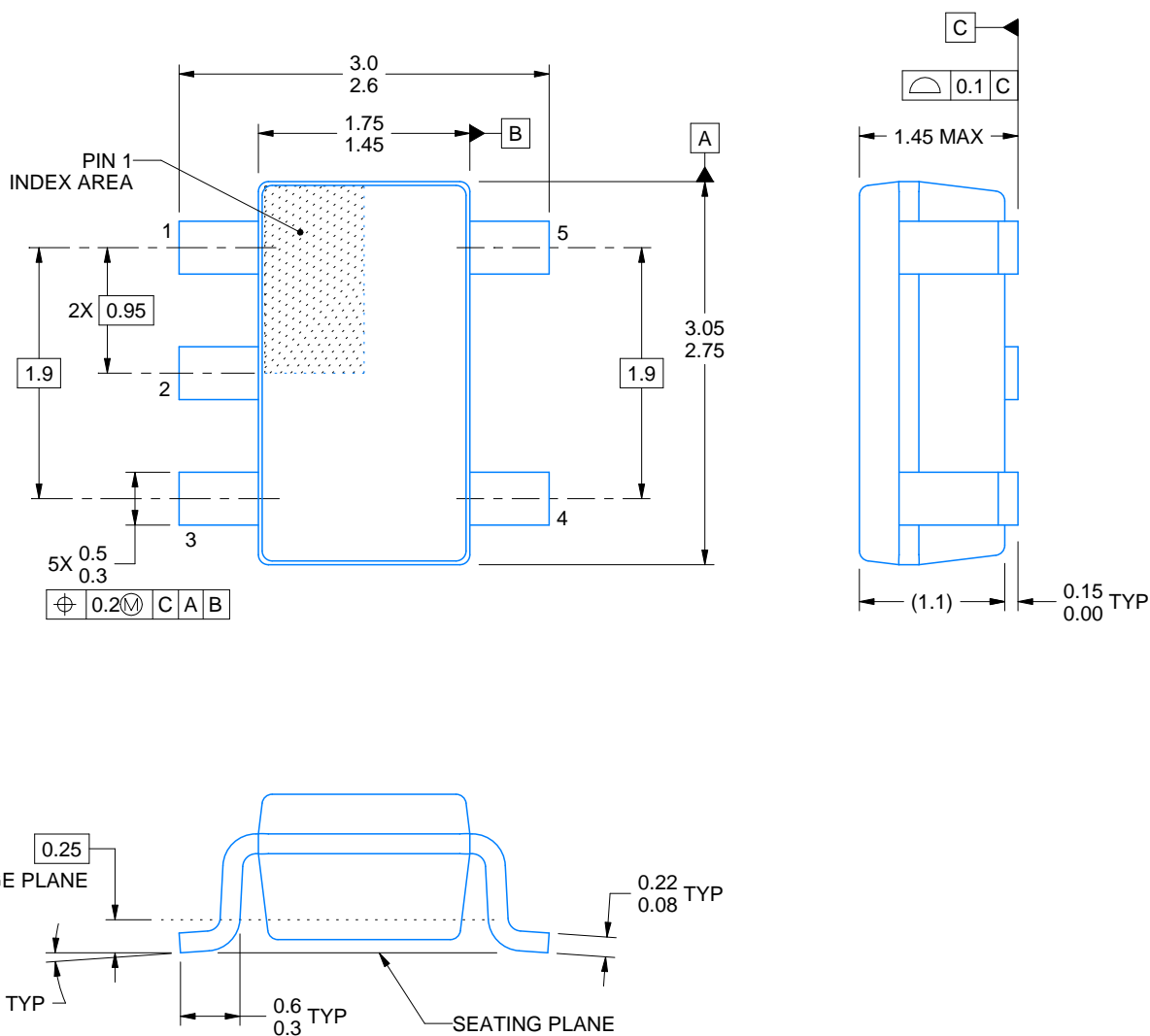


DBV0005A

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/C 04/2017

NOTES:

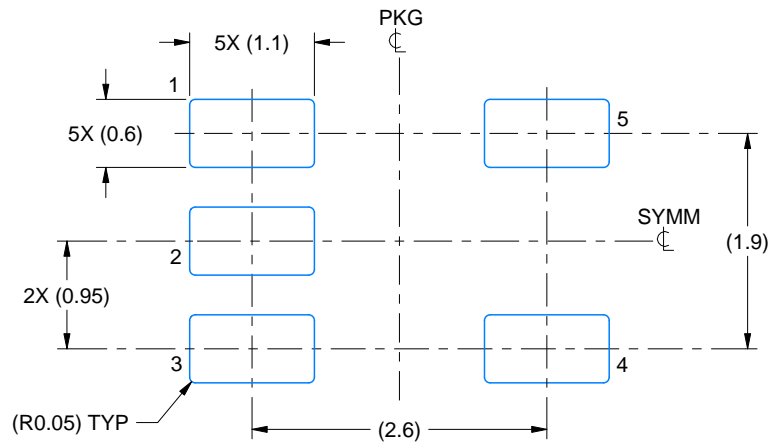
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

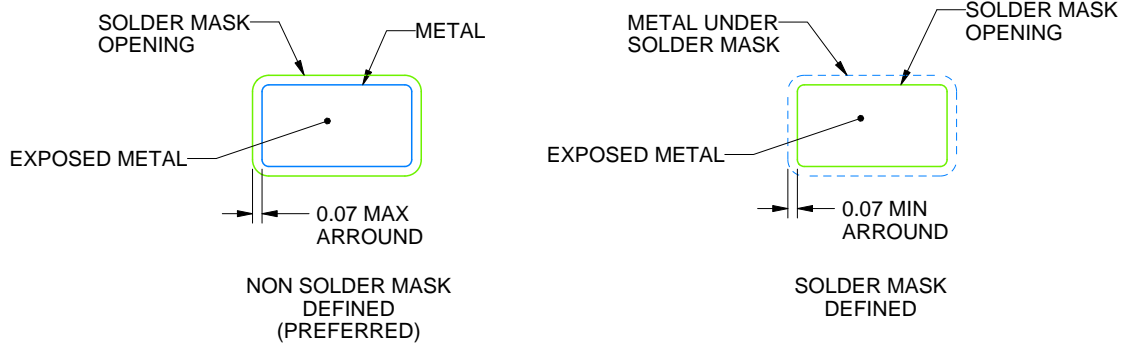
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

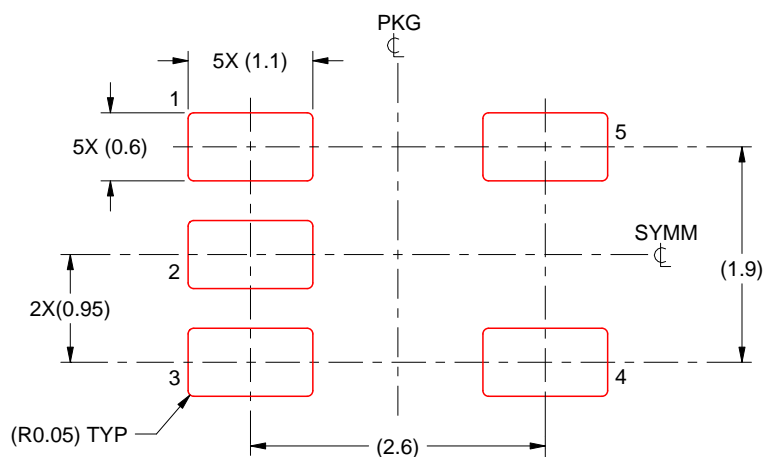
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

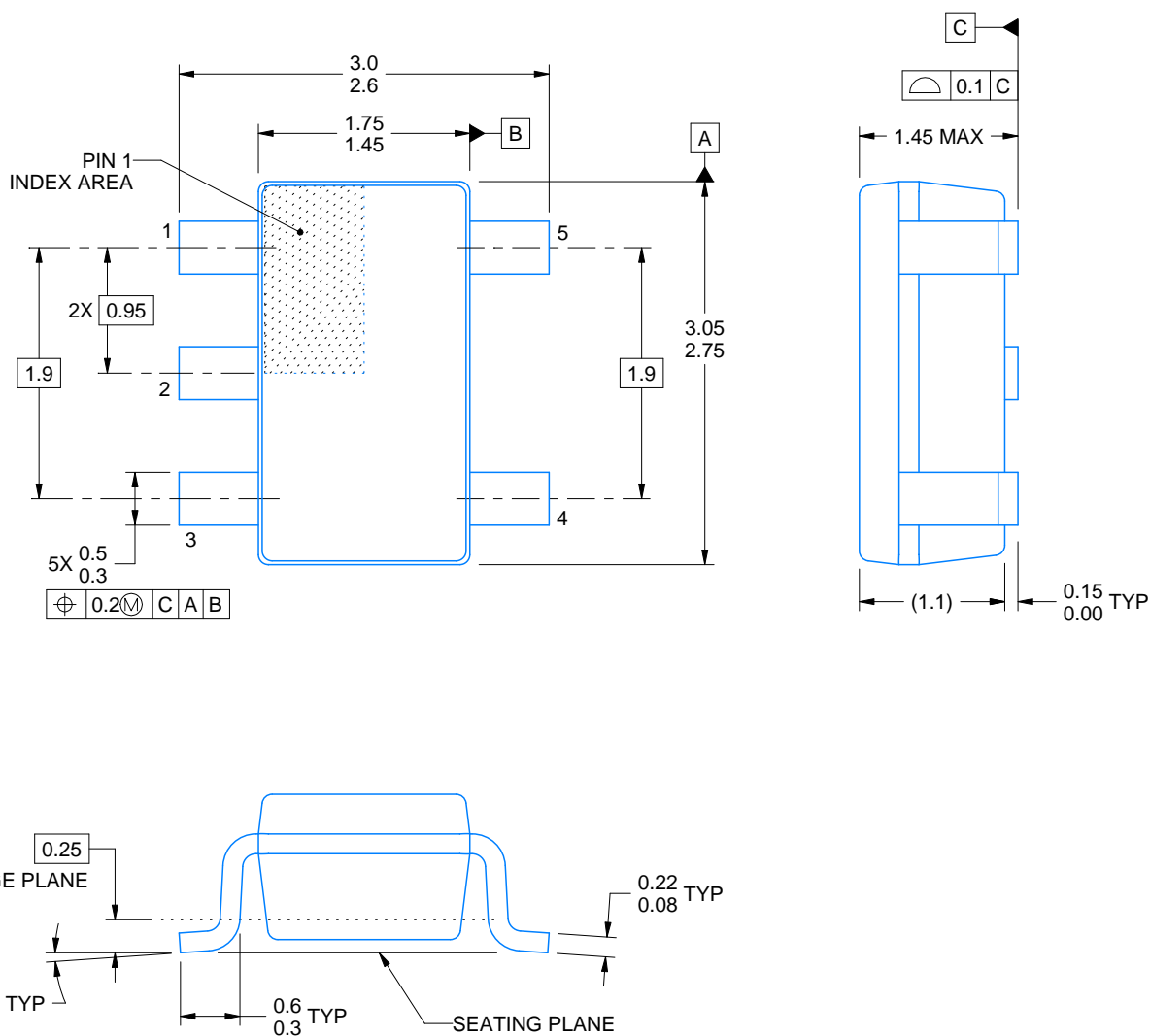


DBV0005A

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/C 04/2017

NOTES:

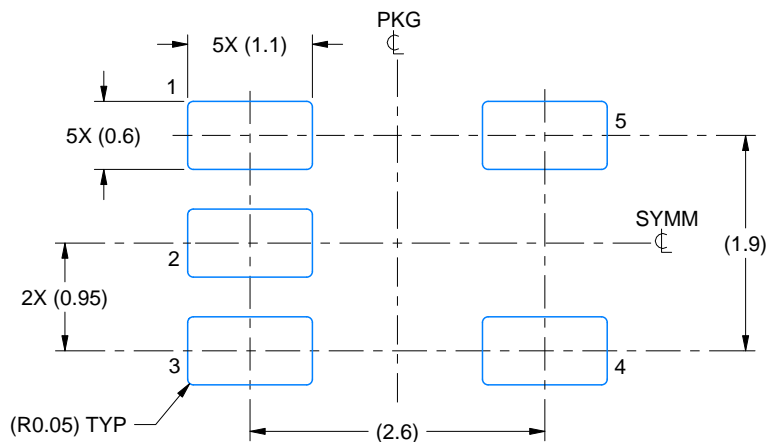
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

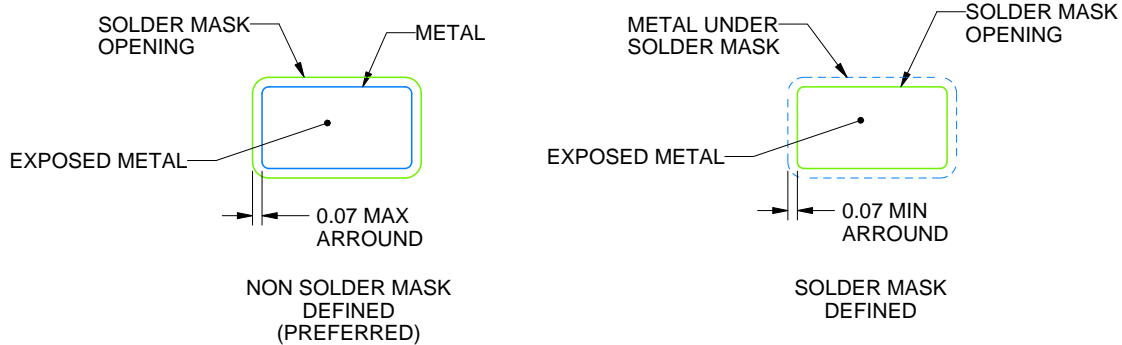
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

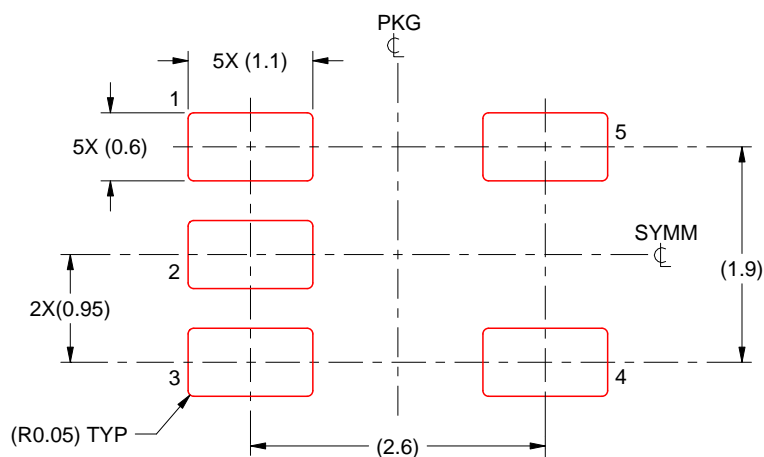
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

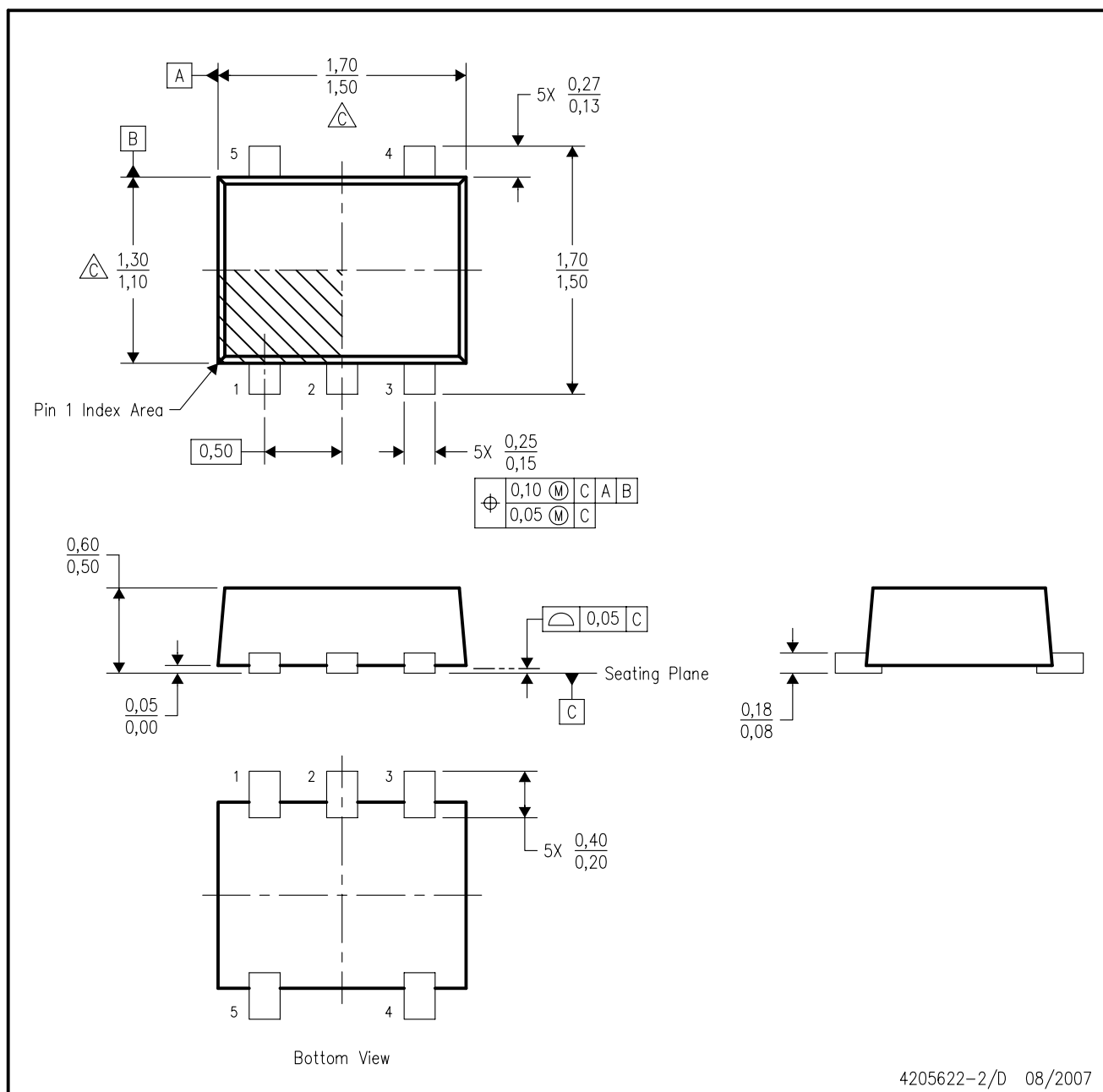


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.



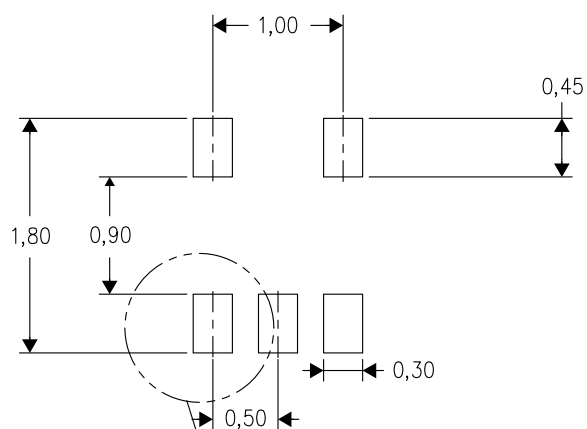
4205622-2/D 08/2007

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
 - D. JEDEC package registration is pending.

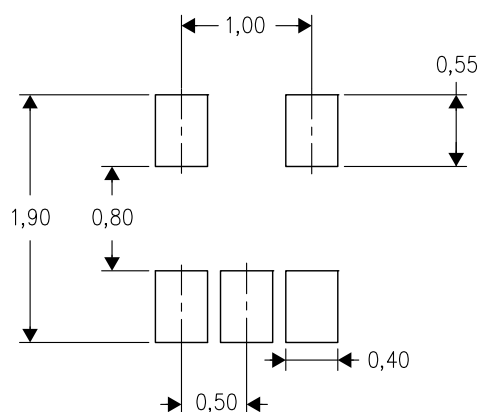
DRL (R-PDSO-N5)

PLASTIC SMALL OUTLINE

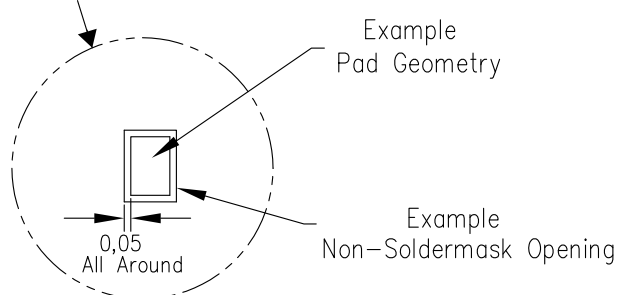
Example Board Layout



Example Stencil Design
(Note E)



Example
Non-Soldermask Defined Pad



4208207-2/E 06/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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