1 Introduction

The TI TSW14J56 evaluation module (EVM) is a next generation pattern generator and data capture card used to evaluate performances of the new TI JESD204B device family of high-speed analog-to-digital converters (ADC) and digital-to-analog converters (DAC). For an ADC, by capturing the sampled data over a JESD204B interface when using a high-quality, low-jitter clock, and a high-quality input frequency, the TSW14J56 can be used to demonstrate datasheet performance specifications. Using Altera JESD204B IP cores, the TSW14J56 can be dynamically configurable to support lane speeds from 600 Mbps to 10.3125 Gbps, from 1 to 8 lanes, 1 to 16 converters, and 1 to 4 octets per frame with one firmware build. Together with the accompanying High-Speed Data Converter Pro Graphic User Interface (GUI), it is a complete system that captures and evaluates data samples from ADC EVMs and generates and sends desired test patterns to DAC EVMs.

2 Functionality

The TSW14J56EVM has a single industry standard FMC connector that interfaces directly with TI JESD204B ADC and DAC EVM's. When used with an ADC EVM, high-speed serial data is captured, de-serialized and formatted by an Altera Arria V GZ FPGA. The data is then stored into an external DDR3 memory bank, enabling the TSW14J56 to store up to 512M 16-bit data samples. To acquire data on a host PC, the FPGA reads the data from memory and transmits it on a serial peripheral interface (SPI). An onboard high-speed USB-to-SPI converter bridges the FPGA SPI interface to the host PC and GUI.

In pattern generator mode, the TSW14J56 generates desired test patterns for DAC EVMs under test. These patterns are sent from the host PC over the USB interface to the TSW14J56. The FPGA stores the data received into the board DDR3 memory module. The data from memory is then read by the FPGA and transmitted to a DAC EVM across the JESD204B interface connector. The board contains a 100-MHz oscillator used to generate the DDR3 reference clock and a 10-MHz oscillator for general purpose use. Figure 1 shows the TI ADS42JB49EVM plugged into the TSW14J56EVM.
Figure 1. TSW14J56EVM Interfacing with an ADS42JB49EVM

The major features of the TSW14J56 are:

- Subclasses: 0 (backward compatible), 1
- Support for deterministic latency
- Serial lanes speeds up to 10.3125 Gbps
- 10 routed transceiver channels
- 8 Gb DDR3 SDRAM (split into two independent 32× 4 Gb SDRAMs, total of 256M samples each). Quarter rate DDR3 controllers supporting up to 800-MHz operation
- 256K 16-bit samples of internal FPGA memory
- Supports 2.5 and 3-V adjustable CMOS IO standard
- Two onboard VCXOs (100 MHz and 10 MHz)
- Onboard UCD90120A for power sequencing and monitoring
- Onboard FT4232HL USB device for JTAG and SPI emulation
• Reference clocking for transceivers available through FMC port or SMAs
• Supported by TI HSDC PRO software
• FPGA firmware developed with Quartus II 13.0 and QSYS
  – JESD RX IP core with support for:
    • SPI and JTAG reconfigurable JESD core parameters: L, M, K, F, HD, S, and more
    • ILA configuration data accessible through SPI and JTAG
    • Lane alignment and character replacement enabled or disabled through SPI and JTAG
  – JESD TX IP core with support for:
    • SPI and JTAG reconfigurable JESD core parameters: L, M, K, F, HD, S, and more
    • ILA data configured through SPI and JTAG
    • Character replacement enabled or disabled through SPI and JTAG
  – Dynamically reconfigurable transceiver data rate. Operating range from 0.600 to 10.3125 Gbps

Figure 2 shows a block diagram of the TSW14J56 EVM.
2.1 ADC EVM Data Capture

New TI high-speed ADCs and DACs now have high-speed serial data that meets the JESD204B standard. These devices are generally available on an EVM that connects directly to the TSW14J56EVM. The common connector between the EVMs and the TSW14J56EVM is a Samtec high-speed, high-density FMC connector (SEAF-40-05.0-S-10-2-A-K) suitable for high-speed differential pairs up to 21 Gbps. A common pinout for the connector across a family of EVMs has been established. At present, the interface between the EVMs and the TSW14J56EVM has defined connections for 10 lanes of serial differential data, two device clock pairs, two SYSREF pairs, two SYNC pairs, four over-range single-ended indicators, and 94 spare general purpose signals that can be used as CMOS I/O pins or differential LVDS signals. There are also two differential clock inputs pairs.

The data format for JESD204B ADCs and DACs is a serialized format, where individual bits of the data are presented on the serial pairs commonly referred to as lanes. Devices designed around the JESD204B spec can have up to 8 lanes for transmitting or receiving data. The firmware in the FPGA on the TSW14J56 is designed to accommodate any of TI's ADC or DAC operating with any number of lanes from 1 to 8.

The GUI loads the FPGA with the appropriate firmware and a specific JESD204B configuration, based on the ADC device selected in the device drop down window. Each ADC device that appears in this window has an initialization file (.ini) associated to it. This .ini file contains JESD information, such as number of lanes, number of converters, octets per frame, and other parameters. This information is loaded into the FPGA registers after the user clicks on the capture button. After the parameters are loaded, synchronization is established between the data converter and FPGA and valid data is then captured into the on-board memory. See the High-Speed Data Capture Pro GUI Software User's Guide SLWU087 and section 2.3 in the guide for more information. Several .ini files are available to allow the user to load predetermined ADC JESD204B interfaces. For example, if the user selects the ADC called "ADS42JB69_LMF_421", the FPGA will be configured to capture data from the ADS42JB69EVM with the ADC JESD interface configured for 4 lanes, 2 converters, and 1 octet per frame.

The TSW14J56 device can capture up to 512M 16-bit samples at a maximum line rate of 10.3125 Gbps that are stored inside the on-board DDR3 memory. To acquire data on a host PC, the FPGA reads the data from memory and transmits it on a serial protocol interface (SPI). An on-board high-speed USB-to-SPI converter bridges the FPGA SPI interface to the host PC and GUI.

2.2 DAC EVM Pattern Generator

In pattern generator mode, the TSW14J56EVM generates desired test patterns for DAC EVMs under test. These patterns are sent from the host PC over the USB interface to the TSW14J56. The FPGA stores the data received into the on-board DDR3 memory. The data from the memory is then read by the FPGA, converted to JESD204B serial format, then transmitted to a DAC EVM. The TSW14J56 can generate patterns up to 512M 16-bit samples at a line rate up to 10.3125 Gbps.

The GUI comes with several existing test patterns that can be download immediately. The GUI also has a pattern generation tool that allows the user to generate a custom pattern, then download it to the on-board memory. See the High-Speed Data Capture Pro Software User's Guide SLWU087 for more information. Like the ADC capture mode, the DAC pattern generator mode uses .ini files to load predetermined JESD204B interface information to the FPGA.

3 Hardware Configuration

This section describes the various portions of the TSW14J56EVM hardware.

3.1 Power Connections

The TSW14J56EVM hardware is designed to operate from a single supply voltage of +5 V DC. The power input is controlled by the on and off switch, SW6. Make sure this switch is in the off position before inserting the provided power plug. Connect the +5 V DC output of the provided AC-to-DC power supply to J11 of the EVM. Connect the other power supply cable to 100 to 240, 50 to 60-Hz VAC source. The board can also be powered up by providing +5 V DC to the red test point, TP34, and the return to any black GND test point. The TSW14J56 draws approximately 0.6 A at power-up and 1.6 A when capturing 4 lanes of data from an ADS42JB69EVM at a line rate of 2.5 Gbps.
3.2 Switches, Jumpers, and LEDs

3.2.1 Switches and Pushbuttons

The TSW14J56 contains several switches and pushbuttons that enable certain functions on the board. The description of the switches can be found in Table 1.

Table 1. Switch Description of the TSW14J56 Device

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SW6</td>
<td>Board main power switch</td>
</tr>
<tr>
<td>SW1 and SW4</td>
<td>Spare dip switches that are connected to spare FPGA inputs</td>
</tr>
<tr>
<td>SW2, SW3, and SW5</td>
<td>Spare pushbutton that are connected to spare FPGA inputs</td>
</tr>
<tr>
<td>SW7 (CPU RESET)</td>
<td>FPGA hardware reset</td>
</tr>
<tr>
<td>SW8 (MSEL)</td>
<td>Sets programming mode of FPGA. Default is all on</td>
</tr>
<tr>
<td>SW9 (UCD Reset)</td>
<td>Power monitor U13 reset</td>
</tr>
</tbody>
</table>

3.2.2 Jumpers

The TSW14J56 contains several jumpers (JP) and solder jumpers (SJP) that enable certain functions on the board. The description of the jumpers can be found in Table 2.

Table 2. Jumper Description of the TSW14J56 Device

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>JP1 (Y1 PWR)</td>
<td>Power enable to general purpose 10-MHz oscillator Y1</td>
<td>1 to 2</td>
</tr>
<tr>
<td>SJP1 (Y1 EN)</td>
<td>Enable to 10-MHz oscillator Y1</td>
<td>1 to 2</td>
</tr>
<tr>
<td>JP3 (Y2 PWR)</td>
<td>Power enable to DDR3 reference 100-MHz oscillator Y2</td>
<td>1 to 2</td>
</tr>
<tr>
<td>JP4, JP5, JP6, and JP7</td>
<td>USB or JTAG control of FPGA programming. Default is USB control</td>
<td>1 to 2</td>
</tr>
<tr>
<td>JP8</td>
<td>USB or internal 5-V power for USB interface. Default is internal power</td>
<td>1 to 2</td>
</tr>
<tr>
<td>JP9</td>
<td>USB internal 5-V power enable. Default is power enabled</td>
<td>2 to 3</td>
</tr>
<tr>
<td>SJP9</td>
<td>Direction control for buffer U7. Default is B to A</td>
<td>1 to 2</td>
</tr>
<tr>
<td>SJP10</td>
<td>Direction control for buffer U10. Default is B to A</td>
<td>1 to 2</td>
</tr>
<tr>
<td>SJP11</td>
<td>Direction control for buffer U11. Default is B to A</td>
<td>1 to 2</td>
</tr>
<tr>
<td>SJP5-SJP8</td>
<td>USB or JTAG control of UCD90120A programming. Default is JTAG</td>
<td>2 to 3</td>
</tr>
<tr>
<td>SJP12</td>
<td>Selects either 3.0 or 2.5 V for V_ADJ power net. Default is 3.0 V</td>
<td>1 to 2</td>
</tr>
</tbody>
</table>

3.3 LEDs

3.3.1 Power and Configuration LEDs

Several LEDs are on the TSW14J56 EVM to indicate the presence of power and the state of the FPGA. The description of these LEDs can be found in Table 3.
Table 3. Power and Configuration LED Description of the TSW14J56 Device

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D17</td>
<td>On if DDR3 VREF power is good</td>
</tr>
<tr>
<td>D32</td>
<td>On if power monitor device indicates that a power net is out of tolerance</td>
</tr>
<tr>
<td>D11</td>
<td>On if +1.0 V is within specification</td>
</tr>
<tr>
<td>D13</td>
<td>On if VCC_1.5 V is within specification</td>
</tr>
<tr>
<td>D16</td>
<td>On if VCC_3.0 V is within specification</td>
</tr>
<tr>
<td>D19</td>
<td>On if VCC_2.5 V is within specification</td>
</tr>
<tr>
<td>D21</td>
<td>On if VCC_2.5 V is within specification</td>
</tr>
<tr>
<td>D23</td>
<td>On if VCCA_GXB_3.0 V is within specification</td>
</tr>
<tr>
<td>D25</td>
<td>On if VCC_PLL_2.5 V is within specification</td>
</tr>
<tr>
<td>D26</td>
<td>On if VCC_0.85V is within specification</td>
</tr>
<tr>
<td>D27</td>
<td>On if VCCDDR_1.5 V is within specification</td>
</tr>
<tr>
<td>D30</td>
<td>On if VTTDDR_0.75 V is within specification</td>
</tr>
<tr>
<td>D33</td>
<td>On if 3.3 V_UCD is within specification</td>
</tr>
<tr>
<td>D28</td>
<td>On after FPGA completes configuration</td>
</tr>
</tbody>
</table>

3.3.2 Status LEDs

Eight status LEDs on the TSW14J56EVM indicate the status of the FPGA, DDR3, and JESD204B interface:

- **D1** – Indicates DAC EVM established SYNC with the TSW14J56 device when off
- **D2** – Indicates presence of device clock from DAC EVM when blinking
- **D3** – Indicates ADC EVM established SYNC with the TSW14J56 device when off
- **D4** – Indicates presence of device clock from ADC EVM when blinking
- **D5** – Not used
- **D6** – DDR3 initialization and calibration complete when off
- **D7** – DDR3 ready when off
- **D8** – DDR3 pass calibration and initialization if on

3.4 Connectors

3.4.1 FPGA Mezzanine Card (FMC) Connector

The TSW14J56 EVM has one connector to allow for the direct plug in of TI JESD204B serial interface ADC and DAC EVMs. The specifications for this connector are mostly derived from the ANSI/VITA 57.1 FPGA Mezzanine Card (FMC) Standard. This standard describes the compliance requirements for a low-overhead protocol bridge between the IO of a mezzanine card and an FPGA processing device on a carrier card. This specification is being used by FPGA vendors on their development platforms.

The FMC connector, J4, provides the interface between the TSW14J56EVM and the ADC or DAC EVM under test. This 400-pin Samtec high-speed, high-density connector (part number SEAF-40-05.0-S-10-2-A-K) is suitable for high-speed differential pairs up to 21 Gbps.

In addition to the JESD204B standard signals, 23 CMOS single-ended signals are sourced from the USB interface through the connector. In the future, these signals may allow the HSDC Pro GUI to control the SPI serial programming of ADC and DAC EVMs that support this feature. The connector pinout description is shown in Table 4.
### Table 4. FMC Connector Description of the TSW14J56

<table>
<thead>
<tr>
<th>FMC Signal Name</th>
<th>FMC Pin</th>
<th>Standard JESD204 Application Mapping</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RX0_P/N</td>
<td>C6 and C7</td>
<td>Lane 0± (M → C)</td>
<td>JESD Serial data transmitted from mezzanine and received by carrier</td>
</tr>
<tr>
<td>RX1_P/N</td>
<td>A2 and A3</td>
<td>Lane 1± (M → C)</td>
<td>JESD Serial data transmitted from mezzanine and received by carrier</td>
</tr>
<tr>
<td>RX2_P/N</td>
<td>A6 and A7</td>
<td>Lane 2± (M → C)</td>
<td>JESD Serial data transmitted from mezzanine and received by carrier</td>
</tr>
<tr>
<td>RX3_P/N</td>
<td>A10 and A11</td>
<td>Lane 3± (M → C)</td>
<td>JESD Serial data transmitted from mezzanine and received by carrier</td>
</tr>
<tr>
<td>RX4_P/N</td>
<td>A14 and A15</td>
<td>Lane 4± (M → C)</td>
<td>JESD Serial data transmitted from mezzanine and received by carrier</td>
</tr>
<tr>
<td>RX5_P/N</td>
<td>A18 and A19</td>
<td>Lane 5± (M → C)</td>
<td>JESD Serial data transmitted from mezzanine and received by carrier</td>
</tr>
<tr>
<td>RX6_P/N</td>
<td>B16 and B17</td>
<td>Lane 6± (M → C)</td>
<td>JESD Serial data transmitted from mezzanine and received by carrier</td>
</tr>
<tr>
<td>RX7_P/N</td>
<td>B12 and B13</td>
<td>Lane 7± (M → C)</td>
<td>JESD Serial data transmitted from mezzanine and received by carrier</td>
</tr>
<tr>
<td>RX8_P/N</td>
<td>B8 and B9</td>
<td>Lane 8± (M → C)</td>
<td>JESD Serial data transmitted from mezzanine and received by carrier</td>
</tr>
<tr>
<td>RX9_P/N</td>
<td>B4 and B5</td>
<td>Lane 9± (M → C)</td>
<td>JESD Serial data transmitted from mezzanine and received by carrier</td>
</tr>
<tr>
<td>TX0_P/N</td>
<td>C2 and C3</td>
<td>Lane 0± (C → M)</td>
<td>JESD Serial data transmitted from carrier and received by mezzanine</td>
</tr>
<tr>
<td>TX1_P/N</td>
<td>A22 and A23</td>
<td>Lane 1± (C → M)</td>
<td>JESD Serial data transmitted from carrier and received by mezzanine</td>
</tr>
<tr>
<td>TX2_P/N</td>
<td>A26 and A27</td>
<td>Lane 2± (C → M)</td>
<td>JESD Serial data transmitted from carrier and received by mezzanine</td>
</tr>
<tr>
<td>TX3_P/N</td>
<td>A30 and A31</td>
<td>Lane 3± (C → M)</td>
<td>JESD Serial data transmitted from carrier and received by mezzanine</td>
</tr>
<tr>
<td>TX4_P/N</td>
<td>A34 and A35</td>
<td>Lane 4± (C → M)</td>
<td>JESD Serial data transmitted from carrier and received by mezzanine</td>
</tr>
<tr>
<td>TX5_P/N</td>
<td>A38 and A39</td>
<td>Lane 5± (C → M)</td>
<td>JESD Serial data transmitted from carrier and received by mezzanine</td>
</tr>
<tr>
<td>TX6_P/N</td>
<td>B36 and B37</td>
<td>Lane 6± (C → M)</td>
<td>JESD Serial data transmitted from carrier and received by mezzanine</td>
</tr>
<tr>
<td>TX7_P/N</td>
<td>B32 and B33</td>
<td>Lane 7± (C → M)</td>
<td>JESD Serial data transmitted from carrier and received by mezzanine</td>
</tr>
<tr>
<td>TX8_P/N</td>
<td>B28 and B29</td>
<td>Lane 8± (C → M)</td>
<td>JESD Serial data transmitted from carrier and received by mezzanine</td>
</tr>
<tr>
<td>TX9_P/N</td>
<td>B24 and B25</td>
<td>Lane 9± (C → M)</td>
<td>JESD Serial data transmitted from carrier and received by mezzanine</td>
</tr>
<tr>
<td>GBTCLK0_M2C_P/N</td>
<td>D4 and D5</td>
<td>DEVCLKA± (M → C)</td>
<td>Primary carrier-bound reference clock required for FPGA giga-bit transceivers. Equivalent to device clock.</td>
</tr>
<tr>
<td>GBTCLK1_M2C_P/N</td>
<td>B20 and B21</td>
<td>Alt. DEVCLKA± (M → C)</td>
<td>Alternate Primary Carrier-bound reference clock required for FPGA giga-bit transceivers. For use when DEVCLKA (M → C) is not available</td>
</tr>
</tbody>
</table>
Table 4. FMC Connector Description of the TSW14J56 (continued)

<table>
<thead>
<tr>
<th>FMC Signal Name</th>
<th>FMC Pin</th>
<th>Standard JESD204 Application Mapping</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK_LA0_P/N</td>
<td>G6 and G7</td>
<td>DEVCLKB± (M → C)</td>
<td>Secondary carrier-bound device clock. Used for special FPGA functions such as sampling SYSREF</td>
</tr>
<tr>
<td>LA01_P/N_CC</td>
<td>D8 and D9</td>
<td>DEVCLK± (C → M)</td>
<td>Mezzanine-bound device clock. Used for low noise conversion clock</td>
</tr>
<tr>
<td>SYSREF_P/N</td>
<td>G9 and G10</td>
<td>SYSREF± (M → C)</td>
<td>Carrier-bound SYSREF signal</td>
</tr>
<tr>
<td>LA05_P/N</td>
<td>D11 and D12</td>
<td>SYSREF± (C → M)</td>
<td>Mezzanine-bound SYSREF signal</td>
</tr>
<tr>
<td>RX_SYNC_P/N</td>
<td>G12 and G13</td>
<td>SYNC± (C → M)</td>
<td>ADC mezzanine-bound SYNC signal for use in class 0/1/2 JESD204 systems</td>
</tr>
<tr>
<td>TX_SYNC_P/N</td>
<td>F10 and F11</td>
<td>DAC SYNC± (M → C)</td>
<td>Carrier-bound SYNC signal for use in class 0/1/2 JESD204 systems</td>
</tr>
<tr>
<td>TX_ALT_SYNC_P/N</td>
<td>F19 and F20</td>
<td>Alt. DAC SYNC± (M → C)</td>
<td>Alternate carrier-bound SYNC signal for use in class 0/1/2 JESD204B systems</td>
</tr>
<tr>
<td>RX_ALT_SYNC_P/N</td>
<td>H31 and H32</td>
<td>Alt. SYNC± (C → M)</td>
<td>Alternate ADC mezzanine-bound SYNC signal. For use when SYNC (C → M) is not available</td>
</tr>
<tr>
<td>SYNC</td>
<td>K22</td>
<td>DAC SYNC (M → C)</td>
<td>Carrier-bound CMOS-level SYNC signal for use in class 0/1/2 JESD204 systems</td>
</tr>
</tbody>
</table>

**Special Purpose I/O**

<table>
<thead>
<tr>
<th></th>
<th></th>
<th>Power good from mezzanine to carrier</th>
</tr>
</thead>
<tbody>
<tr>
<td>PG_M2C_A</td>
<td>F1</td>
<td>Power good from carrier to mezzanine</td>
</tr>
<tr>
<td>PG_C2M_A</td>
<td>D1</td>
<td>GPIO clock</td>
</tr>
<tr>
<td>CLK0_M2C_P/N</td>
<td>H4 and H5</td>
<td>GPIO clock</td>
</tr>
<tr>
<td>CLK1_M2C_P/N</td>
<td>G2 and G3</td>
<td>GPIO clock</td>
</tr>
</tbody>
</table>

All other signals not mentioned in Table 4 can be used as general purpose I/O, either as single-ended signals or differential pairs. The ANSI/VITA 57.1 standard assigns voltages to certain pins. These are labeled as 12V, 3P3V, and VADJ nets on the connector page of the schematic. On the TSW14J56, these pins are connected to test points to allow the user to provide voltages at these pin locations.

### 3.4.2 JTAG Connectors

The TSW14J56EVM includes two industry-standard JTAG connectors, one that connects to the JTAG ports of the FPGA and the other that connects to the programming pins of the power monitor or sequencer device. Jumpers on the TSW14J56EVM allow for the FPGA to be programmed from the JTAG connector or the USB interface. JTAG connector J2 is to be used for troubleshooting only. The board default setup is with the FPGA JTAG pins connected to the USB interface. This allows the FPGA to be programmed by the HSDC Pro software GUI. Every time the TSW14J56EVM is powered-down, the FPGA configuration is removed. The user must program the FPGA through the GUI after every time the board is powered-up.

JTAG connector J10 is used to program the TI UCD90120A power monitor/sequencer device. This device is pre-programmed at the factory and this interface should only be used for troubleshooting.

### 3.4.3 USB I/O Connection

Control of the TSW14J56EVM is through USB connector J9. This provides the interface between HSDC Pro GUI running on a PC Windows™ operating system and the FPGA. For the computer, the drivers needed to access the USB port are included on the HSDC Pro GUI installation software that can be downloaded from the web. The drivers are automatically installed during the installation process. On the TSW14J56EVM, the USB port is used to identify the type and serial number of the EVM under test, load the desired FPGA configuration file, capture data from ADC EVMs, and send test pattern data to the DAC EVMs.
4 Software Start-Up

4.1 Installation Instructions

Download the latest version of the HSDC Pro GUI (slwc107x.zip) to a local location on a host PC. Visit www.ti.com and find the install link on the TSW14J56EVM page.

Unzipping the software package generates a folder called “High Speed Data Converter Pro - Installer vx.xx.exe”, where x.xx is the version number. Run this program to start the installation.

Follow the on-screen instructions during installation.

NOTE: If an older version of the GUI has already been installed, make sure to uninstall it before loading a newer version.

Figure 3. GUI Installation

Make sure to disconnect all USB cables from any TSW14xxx boards before installing the software.

Click “Install”. A new window opens. Click “Next”.

Accept the license agreement. Click “Next” to start the installation. After the installer has finished, click “Next”.

The installation is now complete. The GUI executable and associated files reside in the following directory: C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro.

4.2 USB Interface and Drivers

• Connect a USB cable between J9 of the TSW14J56EVM and a host PC.
• Connect the provided +5 V DC source to the EVM and 100 to 240, 50 to 60-Hz VAC source.
• Set SW6 to on.

Click on the High-Speed Data Converter Pro icon that was created on the desktop panel, or go to C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro and double click on the executable called “High Speed Data Converter Pro.exe” to start the GUI.

The GUI first attempts to connect to the EVM USB interface. If the GUI identifies a valid board serial number, a pop-up opens displaying this value, as shown in Figure 4. The user can connect several TSW14J56 EVMs to one host PC, but the GUI can only connect to one at a time. When multiple boards are connected to the PC, the pop-up displays all of the serial numbers found. The user then selects which board to associate the GUI with.
Click “OK” to connect the GUI to the board. The top level GUI opens and appears as shown in Figure 5.

If the message “No Board Connected” opens, double check the USB cable connections and that power switch SW6 is in the on position. If the cable connections appear fine, try establishing a connection by clicking the “Instrument Option” tab at the top left of the GUI and selecting “Connect to the Board”. If this still does not correct this issue, check the status of the host USB port.

When the software is installed and the USB cable is connected to the TSW14J56EVM and the PC, the TSW14J56 USB serial converter should be located in the Hardware Device Manager under the universal serial bus controllers as shown in Figure 6. This is a quad device, therefore an A, B, C, and D USB serial converter are shown. When the USB cable is removed, these four are no longer visible in the device manager. If the drivers are present in the device manager window and the software still does not connect, cycle power to the board and repeat the prior steps.
5 Downloading Firmware

The TSW14J56EVM has an Altera Arria V GZ device that requires firmware to be downloaded every time power is cycled to operate. The firmware files needed are special .rbf formatted files that are provided with the software package. The files used by the GUI currently reside in the directory called C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro\14J56 Details\Firmware.

To load a firmware, after the GUI has established connection, click the “Select ADC” window in the top left of the GUI and select the device to evaluate, for example, ADS42JB69_LMF_421, as shown in Figure 7.

The GUI prompts the user to update the firmware for the ADC. Click “Yes”. The GUI will display the message “Downloading Firmware, Please Wait”. The software now loads the firmware from the PC to the FPGA, a process that takes about 1 minute. Once completed, the GUI reports an Interface Type in the lower right corner and the FPGA_CONF_DONE LED (D28) illuminates along with several of the status LEDs.

If the message appears as shown in Figure 8, verify that all power status LEDs are illuminated. If any LED is off, there may be a problem with a power supply on the board, which can prevent the firmware from downloading. Cycle the power switch to re-initialize the power-up sequencer to try to correct this problem.

![Download Firmware Error Message](image)

**Figure 8. Download Firmware Error Message**
## Revision History

<table>
<thead>
<tr>
<th>Changes from Original (November 2013) to A Revision</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Added the number of converters and octets</td>
<td>2</td>
</tr>
<tr>
<td>• Added a link to the High-Speed Data Converter Pro GUI</td>
<td>2</td>
</tr>
</tbody>
</table>

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.
Texas Instruments (TI) provides the enclosed Evaluation Board/Kit/Module (EVM) under the following conditions:

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods.

Should this evaluation board/kit not meet the specifications indicated in the User’s Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING LIMITED WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please visit www.ti.com/esh or contact TI.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used. TI currently deals with a variety of customers for products, and therefore our arrangement with the user is not exclusive. TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.

REGULATORY COMPLIANCE INFORMATION

As noted in the EVM User’s Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs not subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user’s sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation. Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.
FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003. Changes or modifications not expressly approved by the party responsible for compliance could void the user’s authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.
【Important Notice for Users of EVMs for RF Products in Japan】

This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry’s Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

Texas Instruments Japan Limited
(address) 24-1, Nishi-Shinjuku 6 chome, Shinjuku-ku, Tokyo, Japan

http://www.tij.co.jp

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】
本開発キットは技術基準適合証明を受けておりません。
本製品のご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。
1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

日本テキサス・インスツルメンツ株式会社
東京都新宿区西新宿6丁目24番1号
西新宿三井ビル

http://www.tij.co.jp
**EVALUATION BOARD/KIT/MODULE (EVM)**

**WARNINGS, RESTRICTIONS AND DISCLAIMERS**

For Feasibility Evaluation Only, in Laboratory/Development Environments. Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. Since the EVM is not a completed product, it may not meet all applicable regulatory and safety compliance standards (such as UL, CSA, VDE, CE, RoHS and WEEE) which may normally be associated with similar items. You assume full responsibility to determine and/or assure compliance with any such standards and related certifications as may be applicable. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM’s electronic components and packing materials.

Certain Instructions. It is important to operate this EVM within TI’s recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User’s Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User’s Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, “Claims”) arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

Safety-Critical or Life-Critical Applications. If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2013, Texas Instruments Incorporated
IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have not been so designated is solely at the Buyer’s risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

| Audio          | www.ti.com/audio
| Amplifiers     | amplifier.ti.com
| Data Converters| dataconverter.ti.com
| DLP® Products  | www.dlp.com
| DSP            | dsp.ti.com
| Clocks and Timers | www.ti.com/clocks
| Interface      | interface.ti.com
| Logic          | logic.ti.com
| Power Mgmt     | power.ti.com
| Microcontrollers| microcontroller.ti.com
| RFID           | www.ti-rfid.com
| OMAP Applications Processors | www.ti.com/omap
| Wireless Connectivity | www.ti.com/wirelessconnectivity
|                      | TI E2E Community e2e.ti.com

Applications

| Automotive and Transportation | www.ti.com/automotive
| Communications and Telecom    | www.ti.com/communications
| Computers and Peripherals     | www.ti.com/computers
| Consumer Electronics          | www.ti.com/consumer-apps
| Energy and Lighting           | www.ti.com/energy
| Industrial                    | www.ti.com/industrial
| Medical                       | www.ti.com/medical
| Space, Avionics and Defense   | www.ti.com/space-avionics-defense
| Video and Imaging             | www.ti.com/video

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2013, Texas Instruments Incorporated
Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Texas Instruments: 
TSW14J56EVM