

DRV883x Low-Voltage H-Bridge Driver

1 Features

- H-Bridge Motor Driver
 - Drives a DC Motor or Other Loads
 - Low MOSFET On-resistance: HS + LS 280 mΩ
- 1.8-A Maximum Drive Current
- Separate Motor and Logic Supply Pins:
 - Motor VM: 0 to 11 V
 - Logic VCC: 1.8 to 7 V
- PWM or PH/EN Interface
 - DRV8837: PWM, IN1/IN2
 - DRV8838: PH/EN
- Low-power Sleep Mode With 120-nA Maximum Sleep Current
 - nSLEEP pin
- Small Package and Footprint
 - 8 WSON (PowerPAD™)
 - 2.0 × 2.0 mm
- Protection Features
 - VCC Undervoltage Lockout (UVLO)
 - Overcurrent Protection (OCP)
 - Thermal Shutdown (TSD)

2 Applications

- Cameras
- DSLR Lenses
- Consumer Products
- Toys
- Robotics
- Medical Devices

3 Description

The DRV883x provides an integrated motor driver solution for cameras, consumer products, toys, and other low-voltage or battery-powered motion control applications. The device can drive one DC motor or other devices like solenoids. The output driver block consists of N-channel power MOSFET's configured as an H-bridge to drive the motor winding. An internal charge pump generates needed gate drive voltages.

The DRV883x can supply up to 1.8 A of output current. It operates on a motor power supply voltage from 0 to 11 V, and a device power supply voltage of 1.8 V to 7.0 V.

The DRV8837 has a PWM (IN/IN) input interface; the DRV8837 has a PH/EN input interface. Both interfaces are compatible with industry-standard devices.

Internal shutdown functions are provided for overcurrent protection, short circuit protection, undervoltage lockout, and overtemperature.

Device Information

| ORDER NUMBER | PACKAGE | BODY SIZE |
|--------------|----------|--------------|
| DRV8837DSGR | WSON (8) | 2.0 × 2.0 mm |
| DRV8838DSGR | WSON (8) | 2.0 × 2.0 mm |

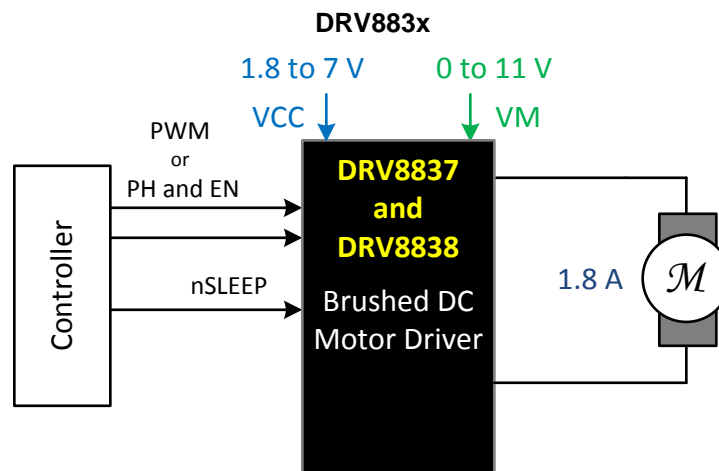


Table of Contents

| | | | |
|---|----------|--|-----------|
| 1 Features | 1 | 7.3 Feature Description | 11 |
| 2 Applications | 1 | 7.4 Device Functional Modes | 12 |
| 3 Description | 1 | 8 Applications and Implementation | 13 |
| 4 Revision History | 2 | 8.1 Application Information | 13 |
| 5 Terminal Configuration and Functions | 3 | 8.2 Typical Applications | 13 |
| 6 Specifications | 4 | 9 Power Supply Recommendations | 15 |
| 6.1 Absolute Maximum Ratings | 4 | 10 Layout | 16 |
| 6.2 Handling Ratings | 4 | 10.1 Layout Guidelines | 16 |
| 6.3 Recommended Operating Conditions | 4 | 10.2 Layout Example | 16 |
| 6.4 Thermal Information | 4 | 11 Device and Documentation Support | 17 |
| 6.5 Electrical Characteristics | 5 | 11.1 Related Links | 17 |
| 6.6 Timing Requirements | 6 | 11.2 Trademarks | 17 |
| 6.7 Typical Characteristics | 8 | 11.3 Electrostatic Discharge Caution | 17 |
| 7 Detailed Description | 9 | 11.4 Glossary | 17 |
| 7.1 Overview | 9 | 12 Mechanical, Packaging, and Orderable Information | 18 |
| 7.2 Functional Block Diagram | 9 | | |

4 Revision History

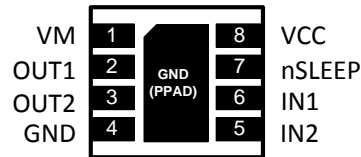
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision B (December 2013) to Revision C | Page |
|--|-------------|
| • Added the DRV8838 device information, specifications, and timing diagrams | 1 |
| • Added Device Information table | 1 |
| • Added a PWM Interface diagram | 1 |
| • Added more information to the Detailed Description and moved information from the Functional Description | 9 |
| • Added functional block diagram for DRV8838 | 10 |
| • Added the Applications and Implementation section | 13 |
| • Added Power Supply Recommendations, Layout, Device and Documentation Support, and Packaging sections | 15 |

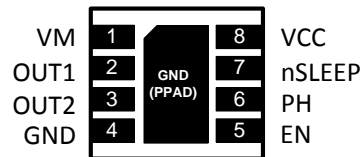
| Changes from Revision A (August 2012) to Revision B | Page |
|--|-------------|
| • Changed Features section | 1 |
| • Changed Recommended Operating Conditions | 4 |
| • Changed Electrical Characteristics section | 5 |
| • Changed Timing Requirements section | 6 |
| • Changed Power Supplies and Input Pins section | 11 |

5 Terminal Configuration and Functions

**DRV8837 DSG – WSON
(Top View)**



**DRV8838 DSG – WSON
(Top View)**



Terminal Descriptions

| TERMINAL | | TYPE | DESCRIPTION |
|-------------------------|--------|------|--|
| NAME | NUMBER | | |
| POWER AND GROUND | | | |
| GND | 4 | PWR | Device ground Must be connected to ground |
| VCC | 8 | PWR | Logic Power supply Bypass to GND with a 0.1- μ F ceramic capacitor rated for VCC |
| VM | 1 | PWR | Motor power supply Bypass to GND with a 0.1- μ F ceramic capacitor rated for VM |
| CONTROL | | | |
| IN1/PH | 6 | I | IN1 or PHASE input See Detailed Description for more information |
| IN2/EN | 5 | I | IN2 or ENABLE input |
| nSLEEP | 7 | I | Sleep mode input Logic low puts the device in low-power sleep mode; logic high for normal operation; internal pulldown resistor |
| OUTPUT | | | |
| OUT1 | 2 | O | Motor output |
| OUT2 | 3 | O | Connect to motor winding |

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾

| | MIN | MAX | UNIT |
|---|--------------------|-----|------|
| Motor power supply voltage range (VM) | -0.3 | 12 | V |
| Logic power supply voltage range (VCC) | -0.3 | 7 | V |
| Control pin voltage range (IN1, IN2, PH, EN, nSLEEP) | -0.5 | 7 | V |
| Peak drive current (OUT1, OUT2) | Internally limited | | A |
| T _J , operating virtual junction temperature range | -40 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

6.2 Handling Ratings

over operating free-air temperature range (unless otherwise noted)

| | MIN | MAX | UNIT |
|--|-----|-----|------|
| T _{stg} Storage temperature range | -60 | 150 | °C |

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | MIN | MAX | UNIT |
|---|-----|-----|------|
| VM Motor power supply voltage range | 0 | 11 | V |
| VCC Logic power supply voltage range | 1.8 | 7 | V |
| I _{OUT} Motor peak current | 0 | 1.8 | A |
| f _{PWM} Externally applied PWM frequency | 0 | 250 | kHz |
| V _{LOGIC} Logic level input voltage | 0 | 5.5 | V |
| T _A Operating ambient temperature | -40 | 85 | °C |

- (1) Power dissipation and thermal limits must be observed.

6.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

| THERMAL METRIC ⁽¹⁾ | DRV8837, DRV8838 | UNIT |
|---|--------------------|------|
| | WSON (8 TERMINALS) | |
| θ _{JA} Junction-to-ambient thermal resistance ⁽²⁾ | 60.9 | °C/W |
| θ _{JC(TOP)} Junction-to-case (top) thermal resistance ⁽³⁾ | 71.4 | |
| θ _{JB} Junction-to-board thermal resistance ⁽⁴⁾ | 32.2 | |
| ψ _{JT} Junction-to-top characterization parameter ⁽⁵⁾ | 1.6 | |
| ψ _{JB} Junction-to-board characterization parameter ⁽⁶⁾ | 32.8 | |
| θ _{JC(BOTTOM)} Junction-to-case (bottom) thermal resistance ⁽⁷⁾ | 9.8 | |

- (1) For more information about traditional and new thermal limits, see the IC Package Thermal Metrics Report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

6.5 Electrical Characteristics

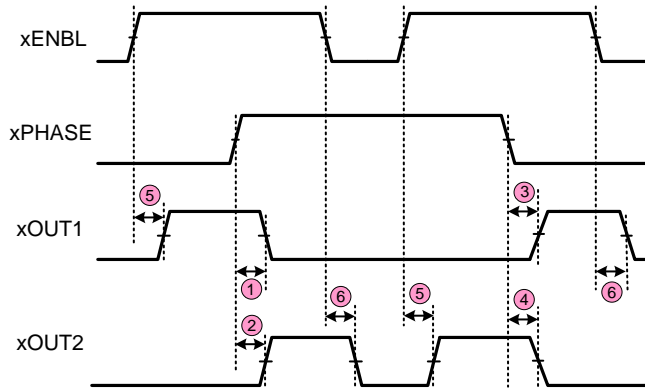
T_A = 25°C, over recommended operating conditions unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-----------------------------------|--|------------|------------|-----------|------|
| POWER SUPPLIES (VM, VCC) | | | | | | |
| VM | VM operating voltage | | 0 | | 11 | V |
| I _{VM} | VM operating supply current | VM = 5 V; VCC = 3 V; No PWM | | 40 | 100 | μA |
| | | VM = 5 V; VCC = 3 V; 50 kHz PWM | | 0.8 | 1.5 | mA |
| I _{VMQ} | VM sleep mode supply current | VM = 5 V; VCC = 3 V; nSLEEP = 0 | | 30 | 95 | nA |
| VCC | VCC operating voltage | | 1.8 | | 7 | V |
| I _{VCC} | VCC operating supply current | VM = 5 V; VCC = 3 V; No PWM | | 300 | 500 | μA |
| | | VM = 5 V; VCC = 3 V; 50 kHz PWM | | 0.7 | 1.5 | mA |
| I _{VCCQ} | VCC sleep mode supply current | VM = 5 V; VCC = 3 V; nSLEEP = 0 | | 5 | 25 | nA |
| CONTROL INPUTS (IN1/PH, IN2/EN, nSLEEP) | | | | | | |
| V _{IL} | Input logic low voltage | | 0.25 × VCC | 0.38 × VCC | | V |
| V _{IH} | Input logic high voltage | | | 0.46 × VCC | 0.5 × VCC | V |
| V _{HYS} | Input logic hysteresis | | | 0.08 × VCC | | mV |
| I _{IL} | Input logic low current | V _{IN} = 0 V | -5 | | 5 | μA |
| I _{IH} | Input logic high current | V _{IN} = 3.3 V | | | 50 | μA |
| | | V _{IN} = 3.3 V, DRV8838 nSLEEP pin | | 60 | | μA |
| R _{PD} | Pulldown resistance | | | 100 | | kΩ |
| | | DRV8838 nSLEEP pin | | 55 | | kΩ |
| MOTOR DRIVER OUTPUTS (OUT1, OUT2) | | | | | | |
| R _{DS(ON)} | HS + LS FET on-resistance | VM = 5 V; VCC = 3 V; I _O = 800 mA; T _J = 25°C | | 280 | 330 | mΩ |
| I _{OFF} | Off-state leakage current | V _{OUT} = 0 V | -200 | | 200 | nA |
| PROTECTION CIRCUITS | | | | | | |
| V _{UVLO} | VCC undervoltage lockout | VCC falling | | | 1.7 | V |
| | | VCC rising | | | 1.8 | |
| I _{OCP} | Overcurrent protection trip level | | 1.9 | | 3.5 | A |
| t _{DEG} | Overcurrent deglitch time | | | 1 | | μs |
| t _{RETRY} | Overcurrent retry time | | | 1 | | ms |
| T _{TSD} | Thermal shutdown temperature | Die temperature T _J | 150 | 160 | 180 | °C |

6.6 Timing Requirements

T_A = 25°C, V_M = 5 V, V_{CC} = 3 V, R_L = 20 Ω

| NUMBER | PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|--------|-------------------|--|-----|-----|------|
| 1 | t ₁ | Delay time, PHASE high to OUT1 low | | 160 | ns |
| 2 | t ₂ | Delay time, PHASE high to OUT2 high | | 200 | ns |
| 3 | t ₃ | Delay time, PHASE low to OUT1 high | | 200 | ns |
| 4 | t ₄ | Delay time, PHASE low to OUT2 low | | 160 | ns |
| 5 | t ₅ | Delay time, ENBL high to OUTx high | | 200 | ns |
| 6 | t ₆ | Delay time, ENBL low to OUTx low | | 160 | ns |
| 7 | t ₇ | Output enable time | | 300 | ns |
| 8 | t ₈ | Output disable time | | 300 | ns |
| 9 | t ₉ | Delay time, INx high to OUTx high | | 160 | ns |
| 10 | t ₁₀ | Delay time, INx low to OUTx low | | 160 | ns |
| 11 | t ₁₁ | Output rise time | 30 | 188 | ns |
| 12 | t ₁₂ | Output fall time | 30 | 188 | ns |
| | t _{wake} | Wake time, nSLEEP rising edge to part active | | 30 | μs |



DRV8838

Figure 1. Input and Output Timing for DRV8838

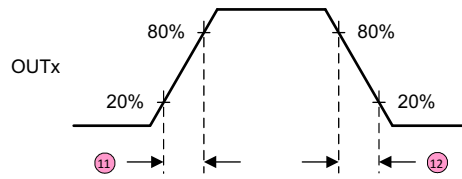
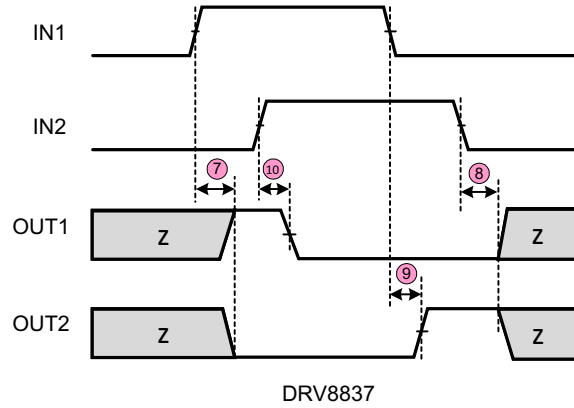
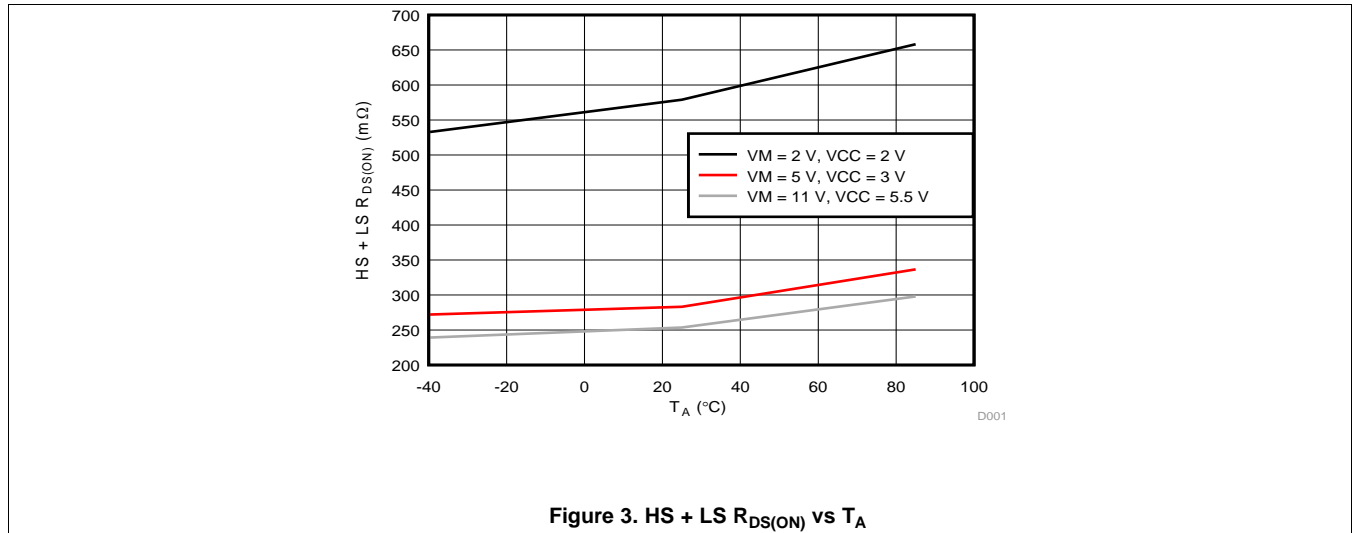


Figure 2. Input and Output Timing for DRV8837

6.7 Typical Characteristics

Plot generated using characterization data



7 Detailed Description

7.1 Overview

The DRV883x is a H-bridge driver that can drive one DC motor or other devices like solenoids. The outputs are controlled using either a PWM interface (IN1/IN2) on the DRV8837 or a PH/EN interface on the DRV8838.

A low-power sleep mode is included, which can be enabled using the nSLEEP pin.

These devices greatly reduce the component count of motor driver systems by integrating the necessary driver FETs and FET control circuitry into a single device. In addition, the DRV883x adds protection features above traditional discrete implementations: undervoltage lockout, overcurrent protection, and thermal shutdown.

7.2 Functional Block Diagram

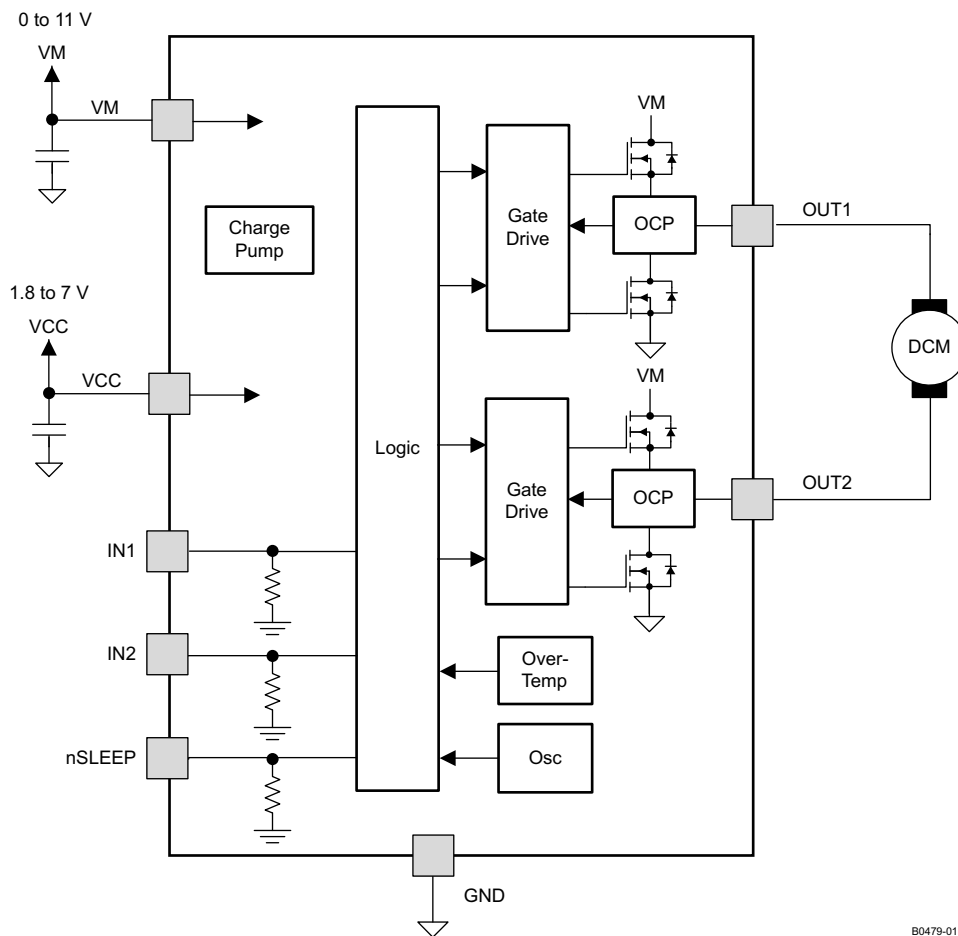


Figure 4. DRV8837 Functional Block Diagram

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Functional Block Diagram (continued)

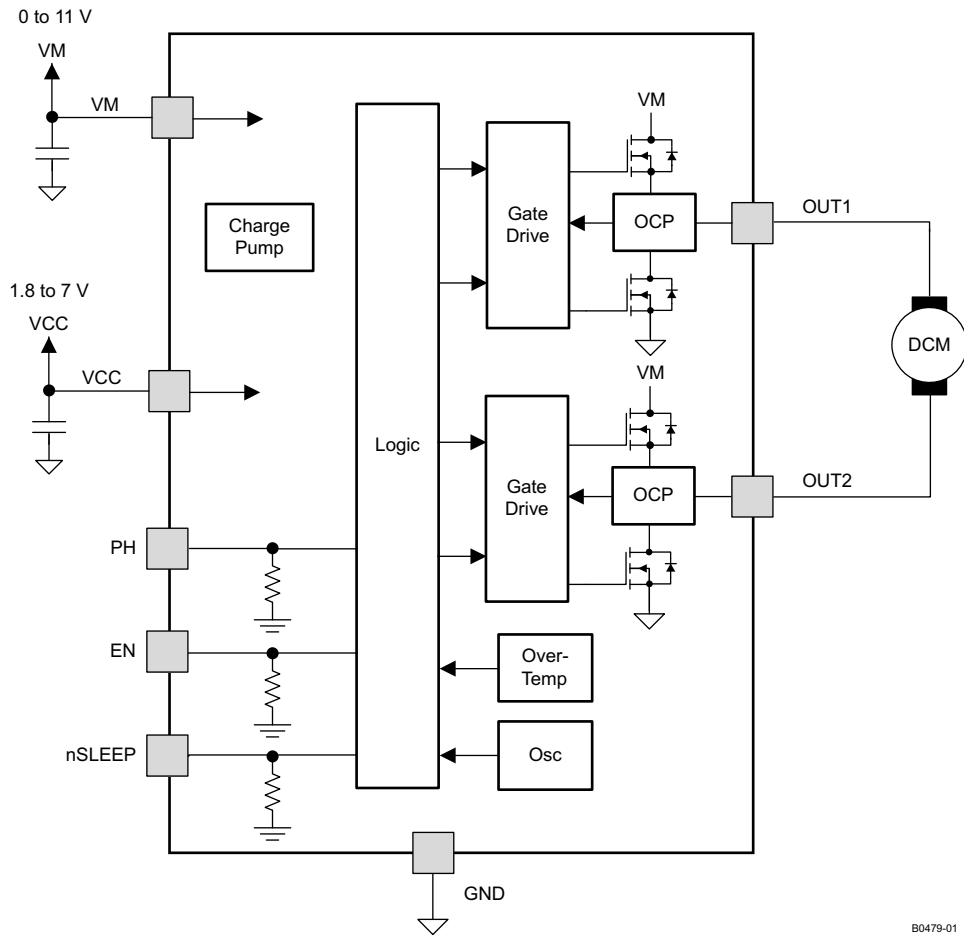


Figure 5. DRV8838 Functional Block Diagram

B0479-01

7.3 Feature Description

7.3.1 Bridge Control

The DRV8837 is controlled using a PWM input interface, also called an IN/IN interface. Each output is controlled by a corresponding input pin.

Table 1 shows the logic for the DRV8837 device:

Table 1. DRV8837 Device Logic

| nSLEEP | IN1 | IN2 | OUT1 | OUT2 | Function (DC Motor) |
|--------|-----|-----|------|------|---------------------|
| 0 | X | X | Z | Z | Coast |
| 1 | 0 | 0 | Z | Z | Coast |
| 1 | 0 | 1 | L | H | Reverse |
| 1 | 1 | 0 | H | L | Forward |
| 1 | 1 | 1 | L | L | Brake |

The DRV8838 is controlled using a PHASE/ENABLE interface. This interface uses one pin to control the H-bridge current direction, and one pin to enable or disable the H-bridge.

Table 2 shows the logic for the DRV8838:

Table 2. DRV8838 Device Logic

| nSLEEP | PH | EN | OUT1 | OUT2 | Function (DC Motor) |
|--------|----|----|------|------|---------------------|
| 0 | X | X | Z | Z | Coast |
| 1 | X | 0 | L | L | Brake |
| 1 | 1 | 1 | L | H | Reverse |
| 1 | 0 | 1 | H | L | Forward |

7.3.2 Sleep Mode

If the nSLEEP pin is brought to a logic-low state, the DRV883x enters a low-power sleep mode. In this state, all unnecessary internal circuitry is powered down.

7.3.3 Power Supplies and Input Terminals

The input pins may be driven within their recommended operating conditions with or without the VCC and/or VM power supplies present. No leakage current path will exist to the supply. There is a weak pulldown resistor (approximately 100 kΩ) to ground on each input pin.

VCC and VM may be applied and removed in any order. When VCC is removed, the device will enter a low power state and draw very little current from VM. VCC and VM may be connected together if the supply voltage is between 1.8 and 7 V.

The VM voltage supply does not have any undervoltage lockout protection (UVLO), so as long as $VCC > 1.8\text{ V}$; the internal device logic will remain active. This means that the VM pin voltage may drop to 0 V, however, the load may not be sufficiently driven at low VM voltages.

7.3.4 Protection Circuits

The DRV883x is fully protected against VCC undervoltage, overcurrent, and overtemperature events.

VCC Undervoltage Lockout: If at any time the voltage on the VCC pin falls below the undervoltage lockout threshold voltage, all FETs in the H-bridge will be disabled. Operation resumes when VCC rises above the UVLO threshold.

Overcurrent Protection (OCP): An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than tDEG, all FETs in the H-bridge will be disabled. Operation resumes automatically after t_{RETRY} has elapsed. Overcurrent conditions will be detected on both the high-side and low-side devices. A short to VM, GND, or from OUT1 to OUT2 results in an overcurrent condition

Thermal Shutdown (TSD): If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled. After the die temperature falls to a safe level, operation automatically resumes.

Table 3. Fault Behavior

| Fault | Condition | H-bridge | Recovery |
|-------------------------|---------------------------------|----------|---------------------------|
| VCC undervoltage (UVLO) | $VCC < 1.7\text{ V}$ | Disabled | $VCC > 1.8\text{ V}$ |
| Overcurrent (OCP) | $I_{OUT} > 1.9\text{ A (MIN)}$ | Disabled | t_{RETRY} elapses |
| Thermal Shutdown (TSD) | $T_J > 150^\circ\text{C (MIN)}$ | Disabled | $T_J < 150^\circ\text{C}$ |

7.4 Device Functional Modes

The DRV883x is active unless the nSLEEP pin is brought logic low. In sleep mode the H-bridge FETs are disabled Hi-Z. The DRV883x is brought out of sleep mode automatically if nSLEEP is brought logic high.

The H-bridge outputs are disabled during undervoltage lockout, overcurrent, and overtemperature fault conditions.

Table 4. Operation Modes

| Mode | Condition | H-bridge |
|-------------------|-------------------------|-----------|
| Operating | nSLEEP pin = 1 | Operating |
| Sleep mode | nSLEEP pin = 0 | Disabled |
| Fault encountered | Any fault condition met | Disabled |

8 Applications and Implementation

8.1 Application Information

The DRV883x device is used to drive one DC motor or other devices like solenoids. The following design procedure can be used to configure the DRV883x.

8.2 Typical Applications

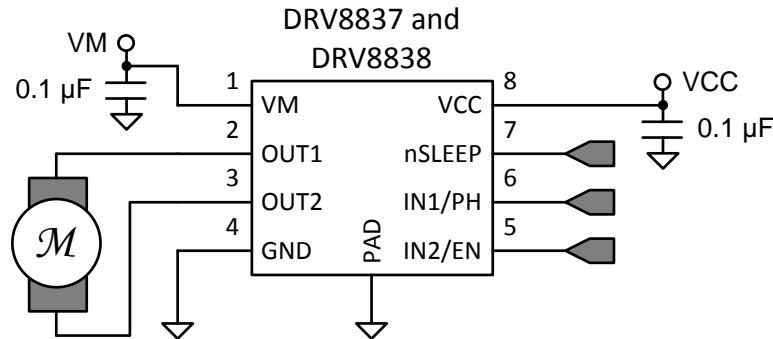


Figure 6. Schematic of DRV883x Application

8.2.1 Design Requirements

Table 5 shows required parameters for a typical usage case.

Table 5. System Design Requirements

| Design Parameter | Reference | Example Value |
|----------------------|------------------|---------------|
| Motor supply voltage | VM | 9 V |
| Logic supply voltage | VCC | 3.3 V |
| Target RMS current | I _{OUT} | 0.8 A |

8.2.2 Detailed Design Procedure

8.2.2.1 Power Dissipation

Power dissipation in the DRV883x is dominated by the power dissipated in the output FET resistance, or R_{DS(ON)}. Average power dissipation when running a stepper motor can be roughly estimated by:

$$P_{TOT} = R_{DS(ON)} \times (I_{OUT(RMS)})^2$$

where

- P_{TOT} is the total power dissipation
 - R_{DS(ON)} is the resistance of the HS plus LS FETs
 - I_{OUT(RMS)} is the RMS or DC output current being supplied to the load
- (1)

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that R_{DS(ON)} increases with temperature, so as the device heats, the power dissipation increases.

The DRV883x has thermal shutdown protection. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

8.2.3 Application Performance Plots

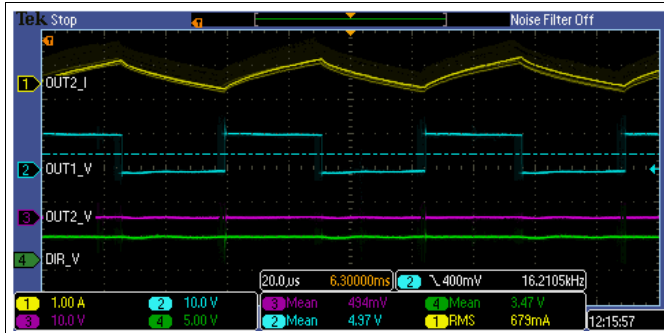


Figure 7. 50% Duty Cycle, Forward Direction



Figure 8. 50% Duty Cycle, Reverse Direction

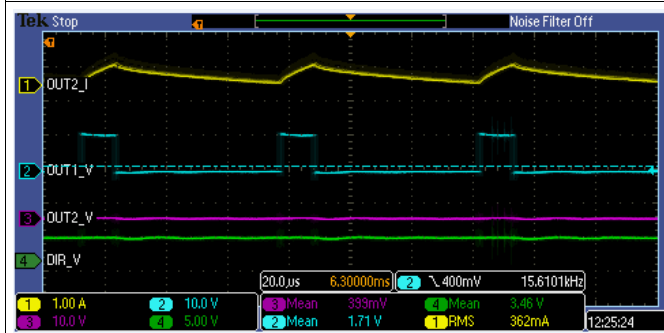


Figure 9. 20% Duty Cycle, Forward Direction



Figure 10. 20% Duty Cycle, Reverse Direction

9 Power Supply Recommendations

VCC and VM may be applied and removed in any order. When VCC is removed, the device enters a low power state and draws very little current from VM. VCC and VM may be connected together if the supply voltage is between 1.8 and 7 V.

Bypass VM and VCC with 0.1- μ F ceramic capacitors rated for VM and VCC. Place these capacitors as close to the device as possible.

The VM voltage supply does not have any undervoltage lockout protection, so as long as $VCC > 1.8$ V; the internal device logic will remain active. This means that the VM pin voltage may drop to 0 V; however, the load may not be sufficiently driven at low VM voltages.

10 Layout

10.1 Layout Guidelines

The VM and VCC terminals should be bypassed to GND using low-ESR ceramic bypass capacitors with a recommended value of 0.1 μF rated for VM and VCC. These capacitors should be placed as close to the VM and VCC pins as possible with a thick trace or ground plane connection to the device GND pin.

10.2 Layout Example

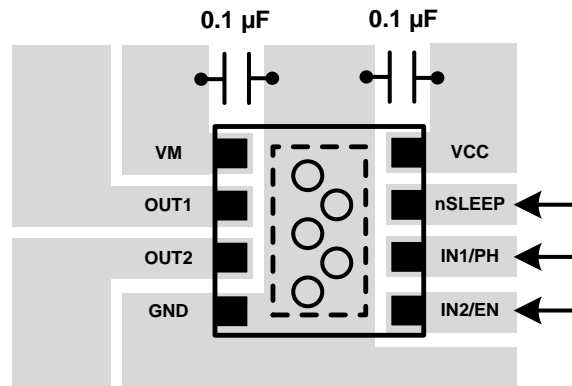


Figure 11. Simplified Layout Example

11 Device and Documentation Support

11.1 Related Links

The following table lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 6. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| DRV8837 | Click here | Click here | Click here | Click here | Click here |
| DRV8838 | Click here | Click here | Click here | Click here | Click here |

11.2 Trademarks

PowerPAD is a trademark of Texas Instruments.

11.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| DRV8837DSGR | ACTIVE | WSO | DSG | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 837 | Samples |
| DRV8837DSGT | ACTIVE | WSO | DSG | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 837 | Samples |
| DRV8838DSGR | ACTIVE | WSO | DSG | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | | Samples |
| DRV8838DSGT | ACTIVE | WSO | DSG | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DRV8837DSGR | WSON | DSG | 8 | 3000 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| DRV8837DSGT | WSON | DSG | 8 | 250 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| DRV8838DSGR | WSON | DSG | 8 | 3000 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| DRV8838DSGT | WSON | DSG | 8 | 250 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal


| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| DRV8837DSGR | WSON | DSG | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| DRV8837DSGT | WSON | DSG | 8 | 250 | 210.0 | 185.0 | 35.0 |
| DRV8838DSGR | WSON | DSG | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| DRV8838DSGT | WSON | DSG | 8 | 250 | 210.0 | 185.0 | 35.0 |

DSG (S-PWSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



4208210/B 10/10

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-Leads (QFN) package configuration.
 -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E. Falls within JEDEC MO-229.

THERMAL PAD MECHANICAL DATA

DSG (S-PWSON-N8)

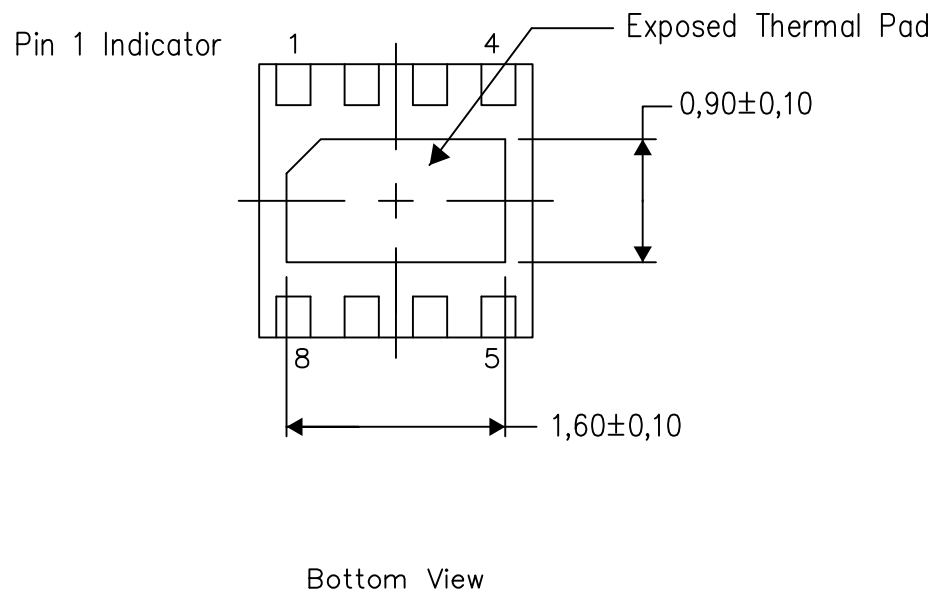
PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



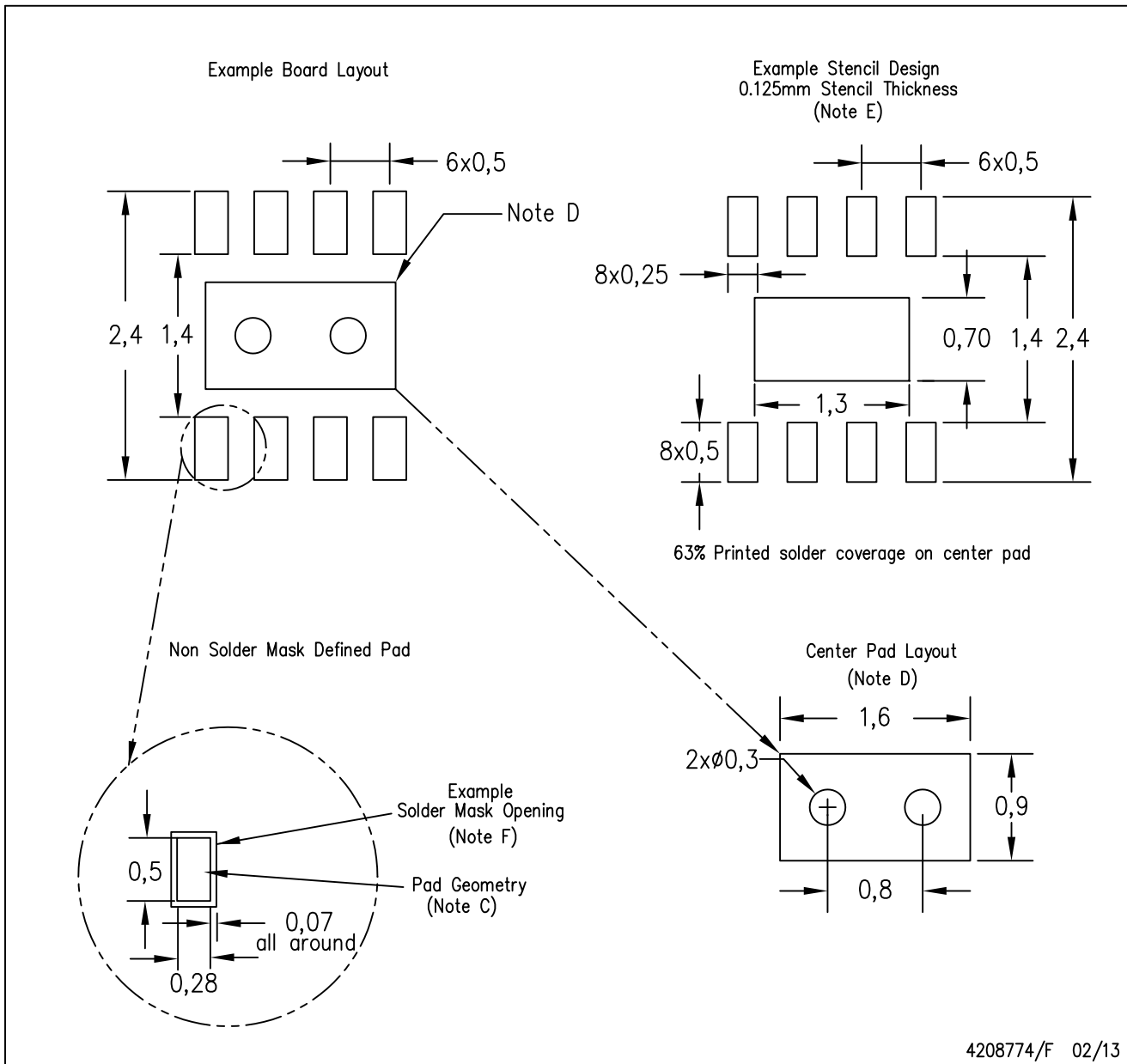
Exposed Thermal Pad Dimensions

4208347/G 08/13

NOTE: All linear dimensions are in millimeters

DSG (S-PWSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for solder mask tolerances.

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