500nA I_Q, 150mA, Ultra-Low Quiescent Current Low-Dropout Linear Regulator

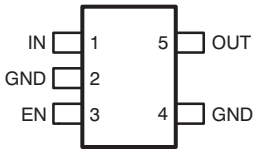
FEATURES

- **Low I_Q: 500nA**
- **150mA, Low-Dropout Regulator**
- **Low-Dropout at +25°C, 130mV at 150mA**
- **Low-Dropout at +85°C, 175mV at 150mA**
- **3% Accuracy Over Load/Line/Temperature**
- **Available in Fixed Voltage Options Using Innovative Factory EEPROM Programming**
- **Stable with a 1.0μF Ceramic Capacitor**
- **Thermal Shutdown and Overcurrent Protection**
- **CMOS Logic Level-Compatible Enable Pin**
- **DDC (TSOT23-5) Package**

APPLICATIONS

- **TI MSP430 Attach Applications**
- **Power Rails with Programming Mode**
- **Wireless Handsets, Smartphones, PDAs, MP3 Players, and Other Battery-Operated Handheld Products**

TPS783xxDDC
TSOT23-5
(TOP VIEW)



DESCRIPTION

The TPS783 family of low-dropout regulators (LDOs) offers the benefits of ultra-low power (I_Q = 500nA), and miniaturized packaging.

This LDO is designed specifically for battery-powered applications where ultra-low quiescent current is a critical parameter. The TPS783, with ultra-low I_Q (500nA), is ideal for microprocessors, microcontrollers, and other battery-powered applications.

The absence of pulldown circuitry at the output of the TPS783 LDO gives an application the flexibility to use the regulator output capacitor as a temporary backup power supply for a short period of time without the presence of the battery when the LDO is disabled (during battery replacement).

The ultra-low power and miniaturized packaging allow designers to customize power consumption for specific applications. Consult with your local factory representative for exact voltage options and ordering information; minimum order quantities may apply.

The TPS783 family is designed to be compatible with the TI MSP430 and other similar products. The enable pin (EN) is compatible with standard CMOS logic. This LDO is stable with any output capacitor greater than 1.0μF. Therefore, this device requires minimal board space because of miniaturized packaging and a potentially small output capacitor. The TPS783 series also features thermal shutdown and current limit to protect the device during fault conditions. All packages have an operating temperature range of T_J = –40°C to +105°C.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

AVAILABLE OPTIONS(1)

	TPS78315	TPS78318	TPS78319	TPS78320	TPS78322	TPS78323	TPS78325	TPS78326
Output Voltage (V)	1.5	1.8	1.9	2.0	2.2	2.3	2.5	2.6
	TPS78328	**TPS78329**	**TPS78330**	**TPS78332**	**TPS78333**	**TPS78336**	**TPS78342**	
Output Voltage (V)	2.8	2.9	3.0	3.2	3.3	3.6	4.2	

(1) Additional output voltage options are available on a quick-turn basis using innovative, factory EEPROM programming. Minimum-order quantities may apply; contact your sales representative for details and availability

ORDERING INFORMATION(1)

PRODUCT	V_{OUT}
TPS783***xxyyyz***	**XX** is the nominal output voltage **YYY** is the package designator. **Z** is the tape and reel quantity (R = 3000, T = 250).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

At T_J = –40°C to +105°C, unless otherwise noted. All voltages are with respect to GND.

PARAMETER		TPS783xx	UNIT
Input voltage range, V_{IN}		–0.3 to +6.0	V
Enable		–0.3 to V_{IN} + 0.3V	V
Output voltage range, V_{OUT}		–0.3 to V_{IN} + 0.3V	V
Maximum output current, I_{OUT}		Internally limited	
Output short-circuit duration		Indefinite	
Total continuous power dissipation, P_{DISS}		See Dissipation Ratings Table	
ESD rating	Human body model (HBM)	2	kV
	Charged device model (CDM)	500	V
Operating junction temperature range, T_J		–40 to +105	°C
Storage temperature range, T_{STG}		–55 to +150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

DISSIPATION RATINGS

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = +25°C	T_A < +25°C	T_A = +70°C	T_A = +85°C
High-K(1)	DDC	90°C/W	200°C/W	5.0mW/°C	500mW	275mW	200mW

(1) The JEDEC high-K (2s2p) board used to derive this data was a 3-inch × 3-inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

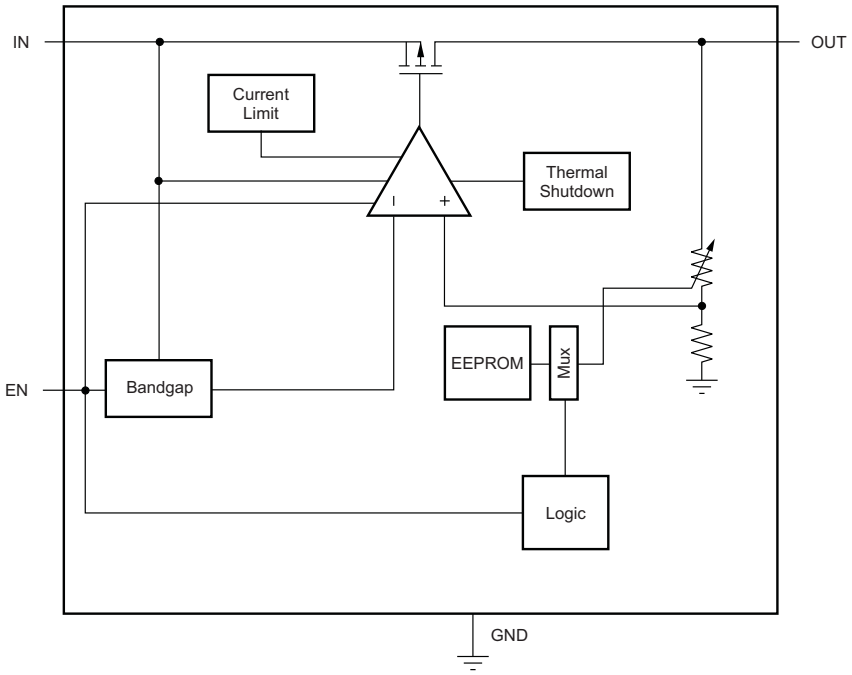
ELECTRICAL CHARACTERISTICS

Over operating temperature range (T_J = –40°C to +105°C), V_{IN} = $V_{OUT(NOM)}$ + 0.5V or 2.2V, whichever is greater; I_{OUT} = 100µA, V_{EN} = V_{IN}, C_{OUT} = 1.0µF, fixed V_{OUT} test conditions, unless otherwise noted. Typical values at T_J = +25°C.

PARAMETER			TEST CONDITIONS		TPS783xx MIN	TPS783xx TYP	TPS783xx MAX	UNIT
V_{IN}	Input voltage range				2.2		5.5	V
V_{OUT}	DC output accuracy	Nominal	T_J = +25°C		–2	±1	+2	%
		Over V_{IN}, I_{OUT}, temperature	V_{OUT} + 0.5V ≤ V_{IN} ≤ 5.5V, 100µA ≤ I_{OUT} ≤ 150mA		–3.0	±2.0	+3.0	%
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation		$V_{OUT(NOM)}$ + 0.5V ≤ V_{IN} ≤ 5.5V			±1.0		%
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation		100µA ≤ I_{OUT} ≤ 150mA			±1.0		%
V_{DO}	Dropout voltage(1)		V_{IN} = 95% $V_{OUT(NOM)}$, I_{OUT} = 150mA			130	250	mV
V_N	Output noise voltage		BW = 100Hz to 100kHz, V_{IN} = 2.2V, V_{OUT} = 1.2V, I_{OUT} = 1mA			86		μV_{RMS}
I_{CL}	Output current limit		V_{OUT} = 0.90 × $V_{OUT(NOM)}$		150	230	400	mA
I_{GND}	Ground pin current		I_{OUT} = 0mA			420	800	nA
			I_{OUT} = 150mA			8		µA
I_{SHDN}	Shutdown current (I_{GND})		V_{EN} ≤ 0.4V, $V_{IN(MIN)}$ ≤ V_{IN} < 5.5V			18	150	nA
$I_{OUT-SHDN}$	Output leakage current at shutdown(2)		V_{IN} = Open, V_{EN} = 0.4V, V_{OUT} = $V_{OUT(NOM)}$			170	500	nA
V_{ENHI}	Enable high-level voltage		V_{IN} = 5.5V		1.2		V_{IN}	V
V_{ENLO}	Enable low-level voltage		V_{IN} = 5.5V		0		0.4	V
I_{EN}	EN pin current		V_{IN} = V_{EN} = 5.5V			3	40	nA
PSRR	Power-supply rejection ratio		V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 150mA	f = 10Hz		40		dB
				f = 100Hz		20		dB
				f = 1kHz		15		dB
t_{STR}	Startup time(3)		C_{OUT} = 1.0µF, V_{OUT} = 10% $V_{OUT(NOM)}$ to V_{OUT} = 90% $V_{OUT(NOM)}$			500		µs
T_{SD}	Thermal shutdown temperature		Shutdown, temperature increasing			+160		°C
			Reset, temperature decreasing			+140		°C
T_J	Operating junction temperature				–40		+105	°C

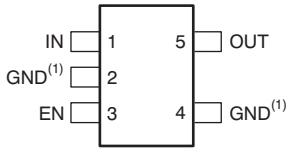
(1) V_{DO} is not measured for devices with $V_{OUT(NOM)}$ ≤ 2.3V because minimum V_{IN} = 2.2V.
(2) See *Shutdown* in the *Application Information* section for more details.
(3) Time from V_{EN} = 1.2V to V_{OUT} = 90% ($V_{OUT(NOM)}$).

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS

DDC PACKAGE
TSOT23-5
(TOP VIEW)



(1) All ground pins must be connected to ground for proper operation.

Table 1. PIN DESCRIPTIONS

PIN		DESCRIPTION
NAME	DDC	
OUT	5	Regulated output voltage pin. A small (1μF) ceramic capacitor is needed from this pin to ground to assure stability. See the *Input and Output Capacitor Requirements* in the Application Information section for more details.
N/C	—	Not connected.
EN	3	Driving the enable pin (EN) over 1.2V turns ON the regulator. Driving this pin below 0.4V puts the regulator into shutdown mode, reducing operating current to 18nA typical.
GND	2, 4	ALL ground pins must be tied to ground for proper operation.
IN	1	Input pin. A small capacitor is needed from this pin to ground to assure stability. Typical input capacitor = 1.0μF. Both input and output capacitor grounds should be tied back to the IC ground with no significant impedance between them.
Thermal pad	—	It is recommended that the thermal pad on the SON-6 package be connected to ground.

TYPICAL CHARACTERISTICS

Over the operating temperature range of T_J = –40°C to +105°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.2V, whichever is greater; I_{OUT} = 100µA, V_{EN} = V_{IN}, C_{OUT} = 1µF, and C_{IN} = 1µF, unless otherwise noted.

TPS78330 LINE REGULATION
I_{OUT} = 5mA, $V_{OUT(NOM)}$ = 3.0V

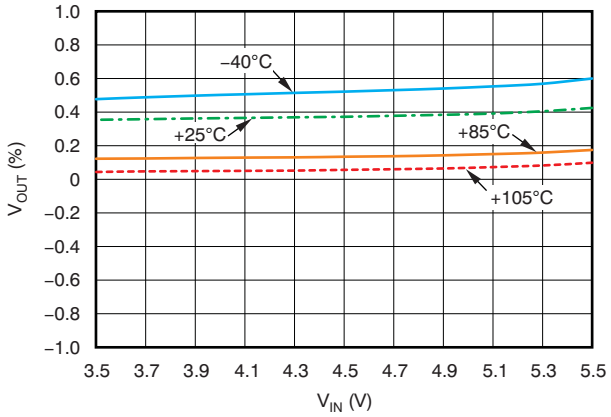


Figure 1.

TPS78330 LINE REGULATION
I_{OUT} = 150mA, $V_{OUT(NOM)}$ = 3.0V

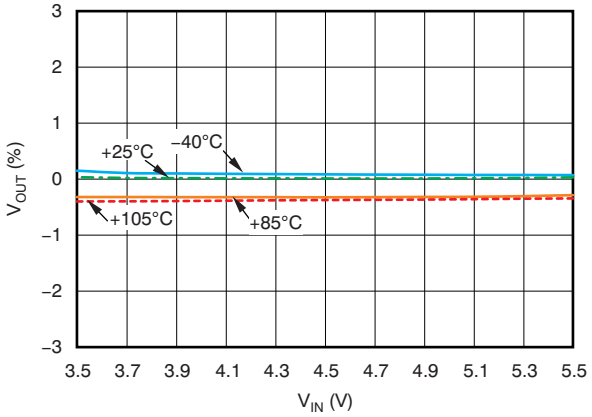


Figure 2.

TPS78330 LOAD REGULATION
V_{IN} = 3.5V, $V_{OUT(NOM)}$ = 3.0V

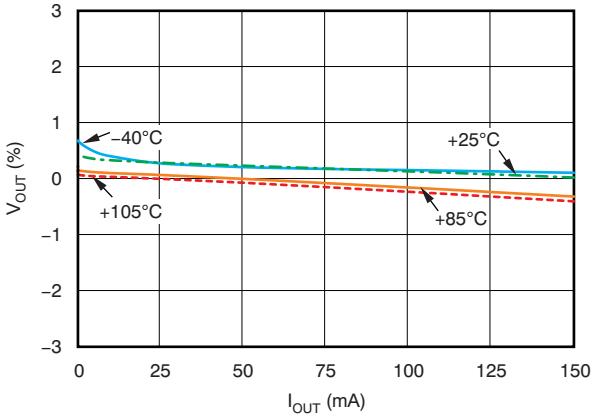


Figure 3.

TPS78330 DROPOUT VOLTAGE vs OUTPUT CURRENT
$V_{OUT(NOM)}$ = 3.0V, V_{IN} = 0.95 × $V_{OUT(NOM)}$

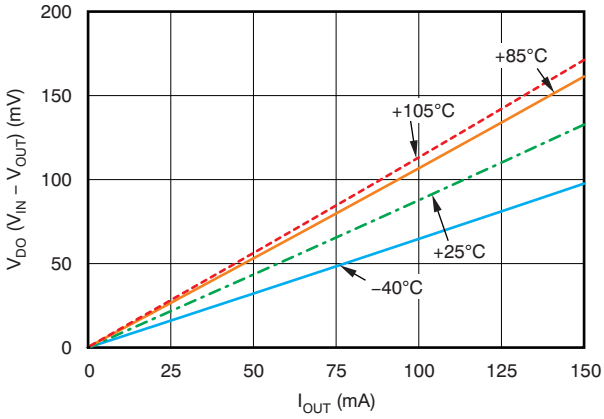


Figure 4.

TPS78330 DROPOUT VOLTAGE vs JUNCTION TEMPERATURE
$V_{OUT(NOM)}$ = 3.0V, V_{IN} = 0.95 × $V_{OUT(NOM)}$

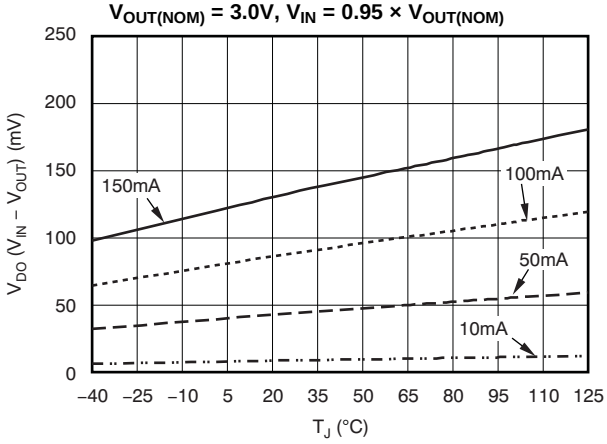


Figure 5.

TYPICAL CHARACTERISTICS (continued)

Over the operating temperature range of T_J = –40°C to +105°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.2V, whichever is greater; I_{OUT} = 100µA, V_{EN} = V_{IN}, C_{OUT} = 1µF, and C_{IN} = 1µF, unless otherwise noted.

TPS78330 GROUND PIN CURRENT vs INPUT VOLTAGE
I_{OUT} = 0mA, $V_{OUT(NOM)}$ = 3.0V

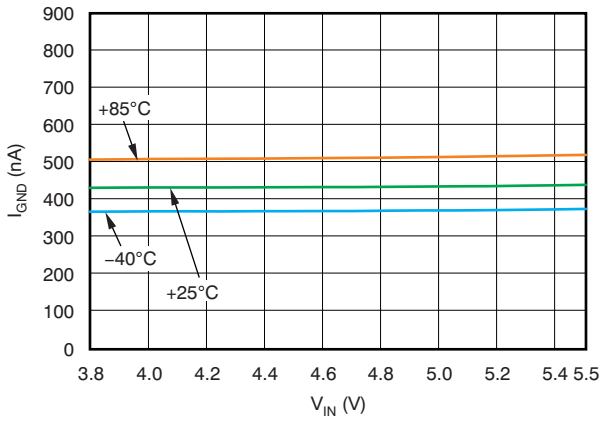


Figure 6.

TPS78330 CURRENT LIMIT vs INPUT VOLTAGE
V_{OUT} = 95% $V_{OUT(NOM)}$, $V_{OUT(NOM)}$ = 3.0V

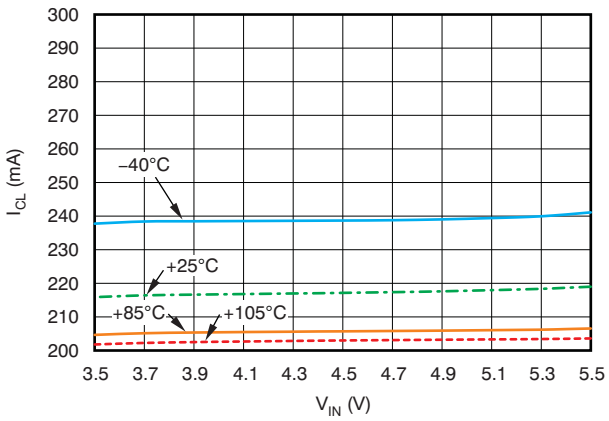


Figure 7.

TPS78330 ENABLE PIN CURRENT vs INPUT VOLTAGE
I_{OUT} = 100µA, $V_{OUT(NOM)}$ = 3.0V

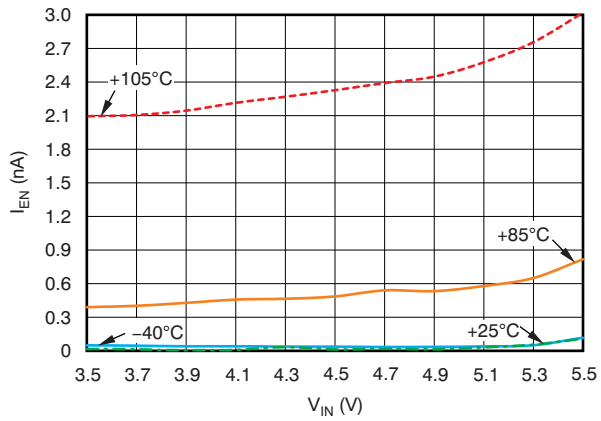


Figure 8.

TPS78330 ENABLE PIN HYSTERESIS vs
JUNCTION TEMPERATURE, I_{OUT} = 1mA, $V_{OUT(NOM)}$ = 3.0V

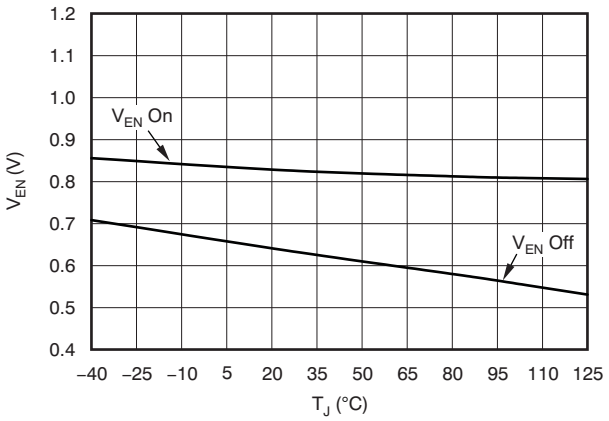


Figure 9.

TPS78330 OUTPUT CURRENT LEAKAGE AT SHUTDOWN
V_{OUT} = $V_{OUT(NOM)}$ = 3.0V, V_{EN} = 0.4V

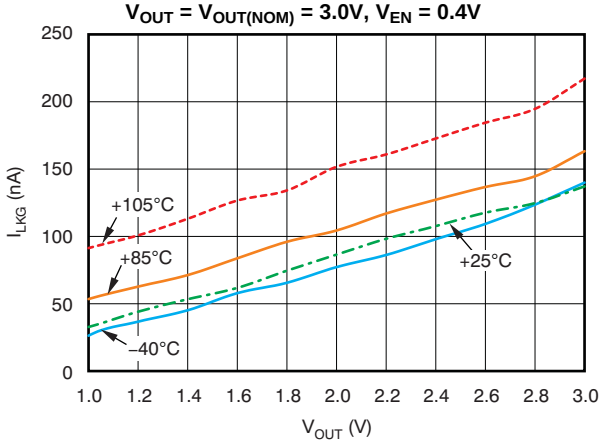


Figure 10.

TYPICAL CHARACTERISTICS (continued)

Over the operating temperature range of T_J = –40°C to +105°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.2V, whichever is greater; I_{OUT} = 100μA, V_{EN} = V_{IN}, C_{OUT} = 1μF, and C_{IN} = 1μF, unless otherwise noted.

TPS78330 OUTPUT SPECTRAL NOISE DENSITY
C_{IN} = 1μF, C_{OUT} = 2.2μF, V_{IN} = 3.5V, $V_{OUT(NOM)}$ = 3.0V

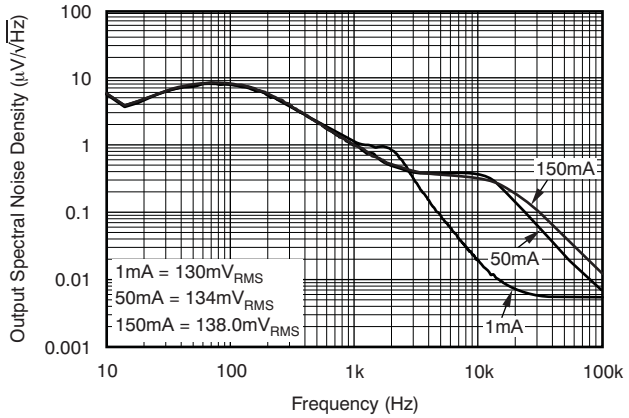


Figure 11.

TPS78330
%ΔV$_{OUT}$ vs JUNCTION TEMPERATURE
V_{IN} = 3.5V, $V_{OUT(NOM)}$ = 3.0V

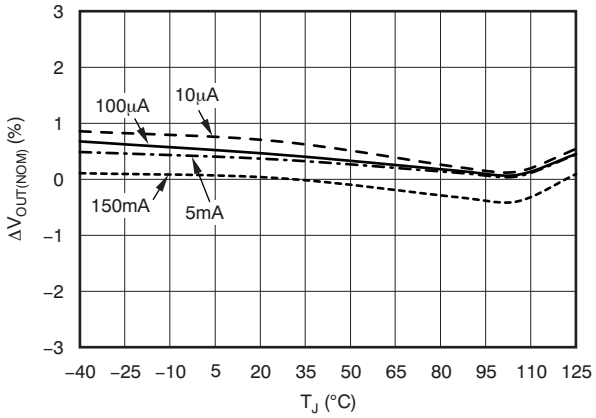


Figure 12.

TPS78330 RIPPLE REJECTION vs FREQUENCY
V_{IN} = 3.5V, $V_{OUT(NOM}$ = 3.0V, C_{OUT} = 2.2μF

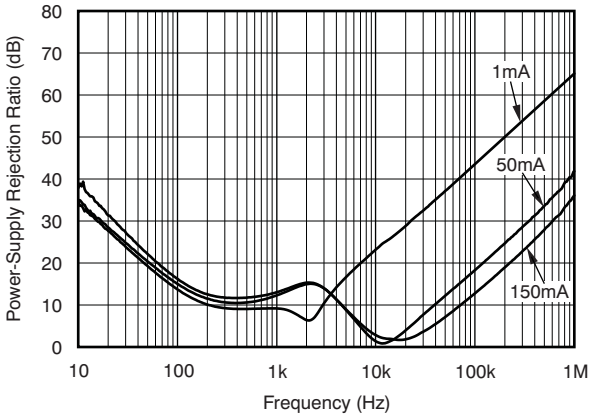


Figure 13.

TPS78330 INPUT VOLTAGE RAMP vs OUTPUT VOLTAGE

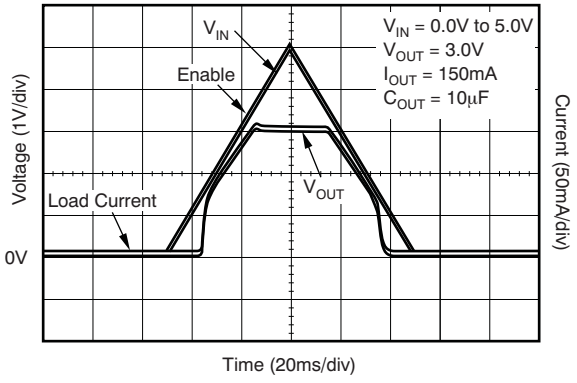


Figure 14.

TPS78330 OUTPUT VOLTAGE vs ENABLE (SLOW RAMP)

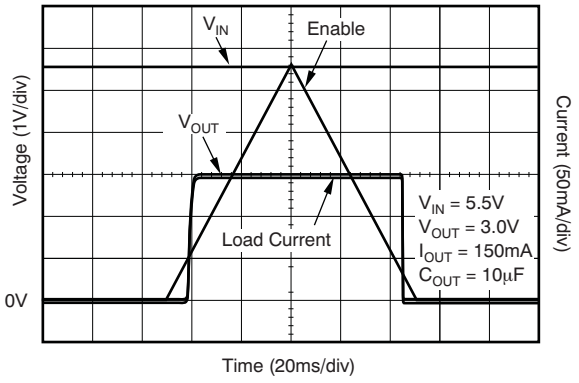


Figure 15.

TPS78330 INPUT VOLTAGE vs DELAY TO OUTPUT

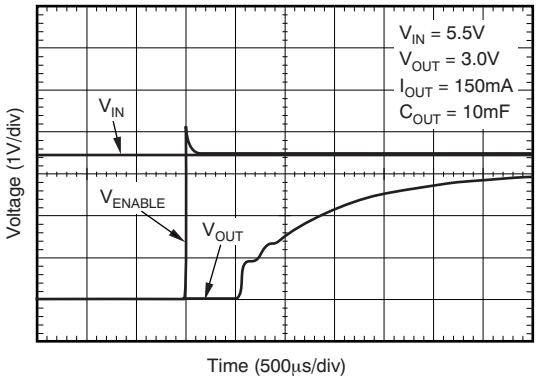


Figure 16.

TYPICAL CHARACTERISTICS (continued)

Over the operating temperature range of T_J = –40°C to +105°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.2V, whichever is greater; I_{OUT} = 100μA, V_{EN} = V_{IN}, C_{OUT} = 1μF, and C_{IN} = 1μF, unless otherwise noted.

TPS78330
LOAD TRANSIENT RESPONSE

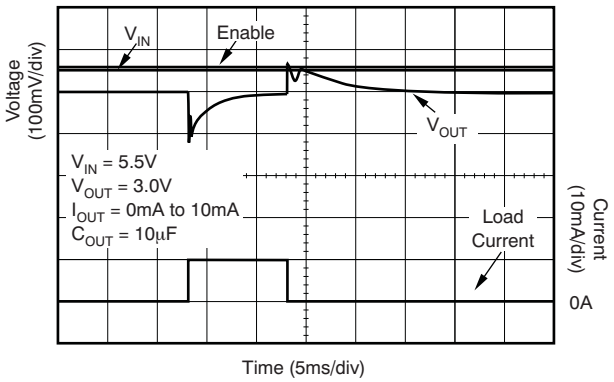


Figure 17.

APPLICATION INFORMATION

APPLICATION EXAMPLES

The TPS783 family of LDOs is factory-programmable to have a fixed output. Note that during startup or steady-state conditions, it is important that the EN pin voltage never exceed V_{IN} + 0.3V.

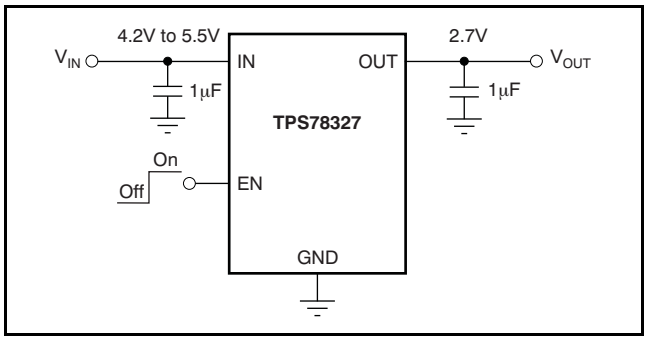


Figure 18. Typical Application Circuit

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

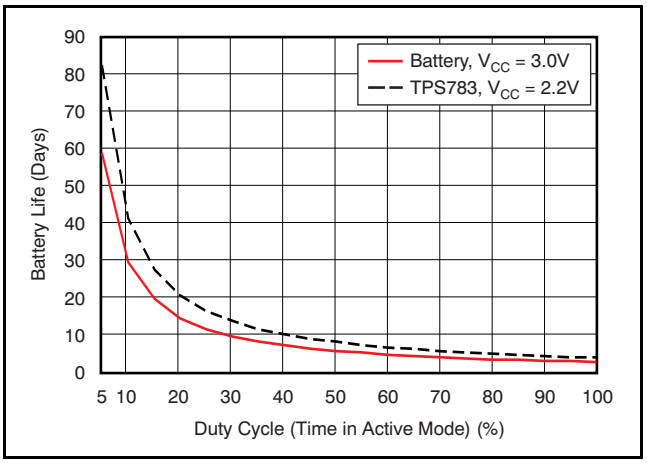
Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1µF to 1.0µF low equivalent series resistance (ESR) capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located near the power source. If source impedance is not sufficiently low, a 0.1µF input capacitor may be necessary to ensure stability.

The TPS783 series are designed to be stable with standard ceramic capacitors with values of 1.0µF or larger at the output.

X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR should be less than 1.0Ω. With tolerance and dc bias effects, the minimum capacitance to ensure stability is 1µF.

EXTENDING BATTERY LIFE IN *KEEP-ALIVE* CIRCUITRY APPLICATIONS FOR MSP430 AND OTHER LOW-POWER MICROCONTROLLERS

One of the primary advantages of a low quiescent current LDO is its extremely low energy requirement. Counter-intuitively, this requirement enables a longer battery life compared to using only the battery as an unregulated voltage supply for low-power microcontrollers such as the MSP430. Figure 19 illustrates the characteristic performance of an unregulated (3.0V) battery supply versus a regulated TPS783 supply for a typical MSP430 application.



Calculated with an MSP430***F*** model, operating at 6MHz.

Figure 19. Battery Life Comparison vs Duty Cycle for MSP430 Application

Table 2 summarizes this comparison.

Table 2. Battery Life Comparison vs Active Mode Time for MSP430 Application

CONDITION/PERFORMANCE	DUTY CYCLE (%)	TPS783xx (NO. OF DAYS)	BATTERY (NO. OF DAYS)	1µA LDO (NO. OF DAYS)
Efficiency with V_{BAT} = 3.0V and V_{CC} = 2.2V (V_O/V_I)	—	73%	100%	73%
LDO quiescent current (I_Q)	—	0.5µA	0	1µA
MSP430 active current	—	2.19mA	3.09mA	2.19mA
MSP430 low-power current	—	0.5µA	0.6µA	0.5µA
Active mode, 1 sec/hour	0.028	5742	6286	4373
Active mode, 10 sec/hour	0.28	1320	998	1085
Active mode, 100 sec/hour	2.8	151	106	148
Active mode, 1000 sec/hour	28	15.4	10.7	15.4
Active mode, 100% duty cycle (on all the time)	100	4.2	3.0	4.2

SUPERCAPACITOR-BASED BACKUP POWER

The very low leakage current at the LDO output gives a system the flexibility to use the device output capacitor as a temporary backup power supply for a short period of time, without the presence of the battery when the LDO is disabled (during battery replacement). The leakage current going into the regulator output from the output capacitor, when the LDO is disabled, is typically 170nA, see Figure 10.

SYSTEM EXAMPLE

When the system is active, a voltage supervisor enables the regulator and puts the MSP430 into active mode when there is a battery installed and its voltage is above a certain threshold, as shown in Figure 20. (The dashed red line indicates the ground current.)

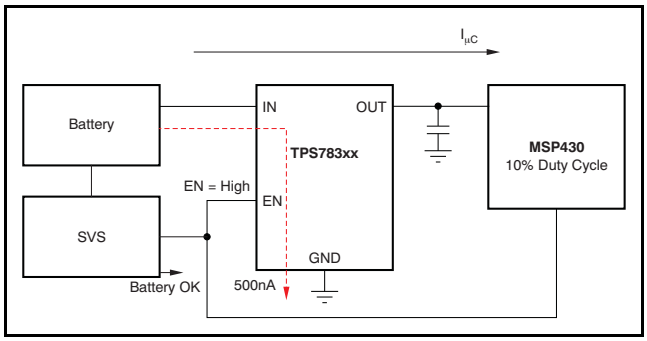


Figure 20. MSP430 Application in Active Mode

When the battery is depleted, the voltage supervisor signals the user to replace the system battery. Once the battery is removed, the voltage supervisor disables the regulator and signals the MSP430 to go into low-power mode. At this moment, the output capacitor acts as a power supply for the MSP430 during the absence of the battery while it is being replaced, as Figure 21 illustrates. (The dashed red line indicates the ground current.)

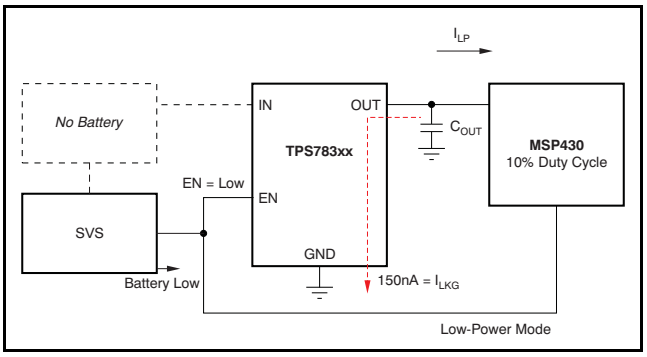


Figure 21. MSP430 Application While Battery is Replaced

The time that the capacitor can provide an appropriate voltage level to the MSP430 (that is, the maximum time it should take to replace a depleted battery with a new battery), or t_{MAX}, can vary from a few seconds to a few minutes, depending on several factors, as Equation 1 shows:

- the nominal output of the regulator, $V_{OUT(Nom)}$ (equivalent to the initial voltage of the capacitor when the regulator is disabled);
- the minimum voltage required by the MSP430, V_{MIN};
- the leakage current into the regulator output, or I_{LKG};
- the current demand from the MSP430 in low-power mode, or I_{LP}; and
- the size of the output capacitor C_{OUT}

$$C_{OUT} = \frac{t_{MAX}}{\left[\frac{V_{OUT(Nom)} - V_{MIN}}{I_{LKG} + I_{LP}}\right]} \quad (1)$$

The PMOS pass element in the TPS783 series has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting up to the maximum rated current for the device may be appropriate.

BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac performance (such as PSRR, output noise, and transient response), it is recommended that the printed circuit board (PCB) be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the output capacitor must be as near to the ground pin of the device as possible to ensure a common reference for regulation purposes. High ESR capacitors may degrade PSRR.

INTERNAL CURRENT LIMIT

The TPS783 is internally current-limited to protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in a current limit state for extended periods of time.

SHUTDOWN

The enable pin (EN) is active high and is compatible with standard and low-voltage CMOS levels. When shutdown capability is not required, EN should be connected to the IN pin, as shown in Figure 22.

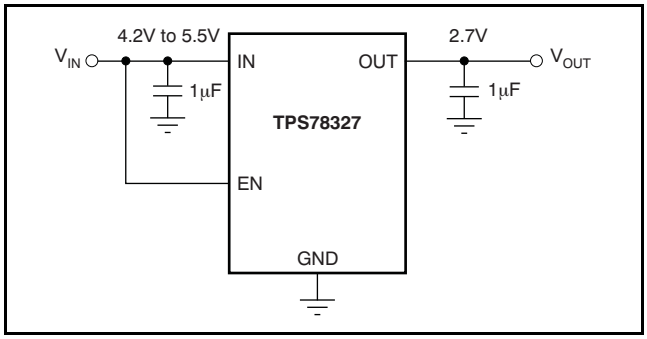


Figure 22. Circuit Showing EN Tied High when Shutdown Capability is Not Required

DROPOUT VOLTAGE

The TPS783 series use a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} approximately scales with output current because the PMOS device behaves like a resistor in dropout. As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout. This effect is shown in the Typical Characteristics section. Refer to application report SLVA207, *Understanding LDO Dropout*, available for download from www.ti.com.

TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response. For more information, see Figure 17.

MINIMUM LOAD

The TPS783 series are stable with no output load. Traditional PMOS LDO regulators suffer from lower loop gain at very light output loads. The TPS783 employs an innovative, low-current circuit under very light or no-load conditions, resulting in improved output voltage regulation performance down to zero output current. See Figure 17 for the load transient response.

THERMAL INFORMATION

THERMAL PROTECTION

Thermal protection disables the device output when the junction temperature rises to approximately +160°C, allowing the device to cool. Once the junction temperature cools to approximately +140°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off again. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +105°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The internal protection circuitry of the TPS783 series has been designed to protect against overload conditions. However, it is not intended to replace proper heatsinking. Continuously running the TPS783 series into thermal shutdown degrades device reliability.

POWER DISSIPATION

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the Dissipation Ratings table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness. Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}), as shown in Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

PACKAGE MOUNTING

Solder pad footprint recommendations for the TPS783 series are available from the Texas Instruments web site at www.ti.com through the TPS783 series product folders.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS78318DDCR	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SIO	Samples
TPS78318DDCT	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SIO	Samples
TPS78319DDCR	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SIP	Samples
TPS78319DDCT	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SIP	Samples
TPS78326DDCR	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SIB	Samples
TPS78326DDCT	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SIB	Samples
TPS78330DDCR	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAZ	Samples
TPS78330DDCT	ACTIVE	SOT	DDC	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAZ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

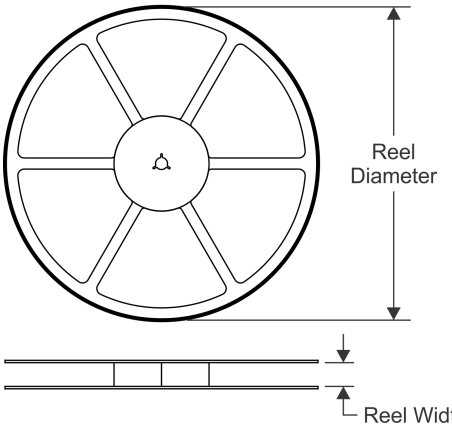
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

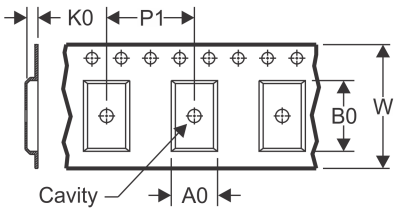
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

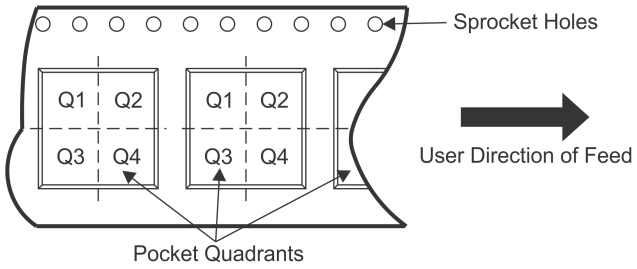


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

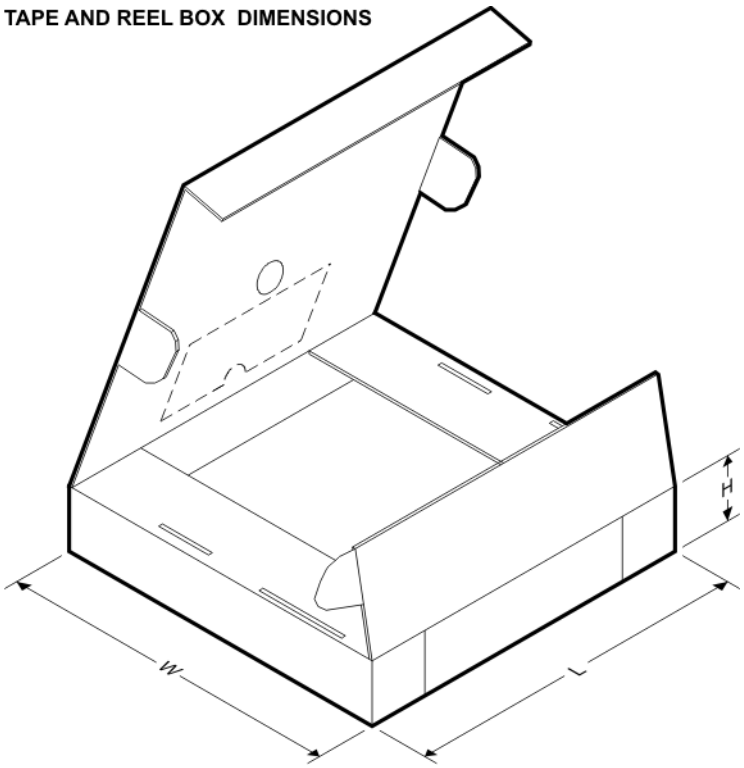
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS78318DDCR	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78318DDCT	SOT	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78319DDCR	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78319DDCT	SOT	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78326DDCR	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78326DDCT	SOT	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78330DDCR	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78330DDCT	SOT	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

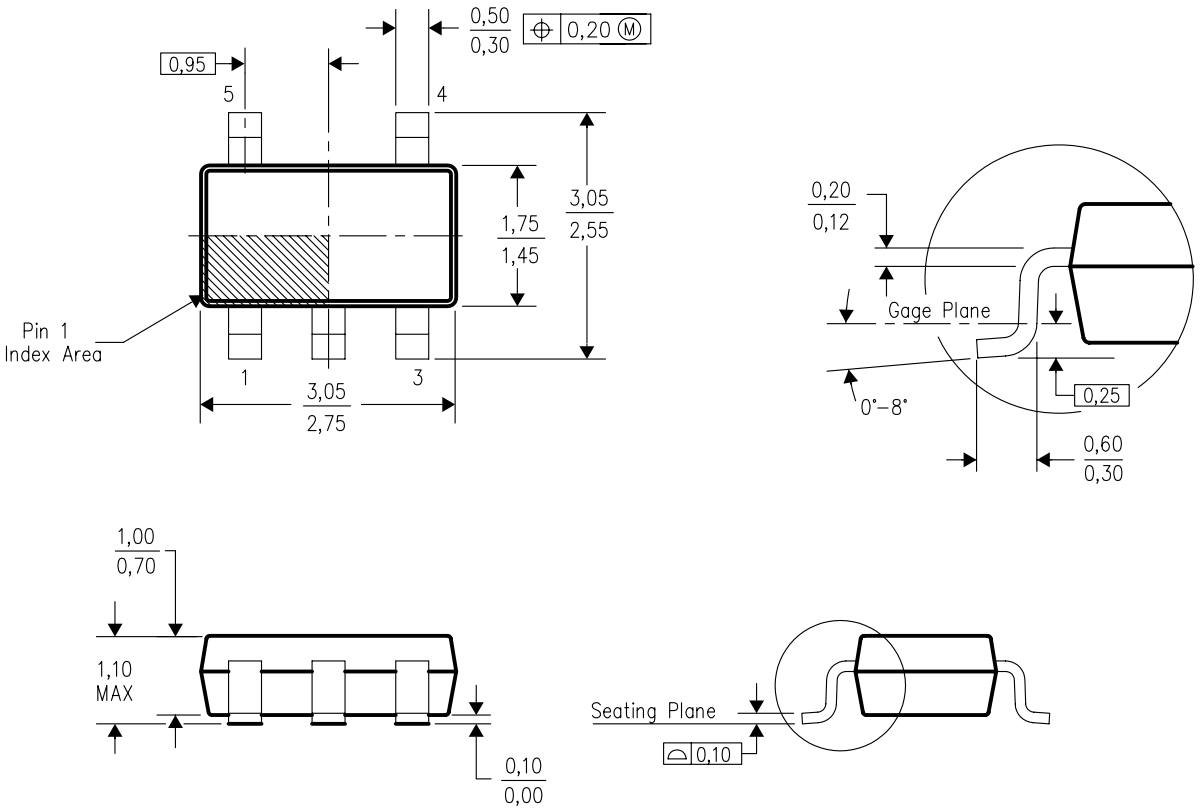
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS78318DDCR	SOT	DDC	5	3000	195.0	200.0	45.0
TPS78318DDCT	SOT	DDC	5	250	195.0	200.0	45.0
TPS78319DDCR	SOT	DDC	5	3000	195.0	200.0	45.0
TPS78319DDCT	SOT	DDC	5	250	195.0	200.0	45.0
TPS78326DDCR	SOT	DDC	5	3000	195.0	200.0	45.0
TPS78326DDCT	SOT	DDC	5	250	195.0	200.0	45.0
TPS78330DDCR	SOT	DDC	5	3000	195.0	200.0	45.0
TPS78330DDCT	SOT	DDC	5	250	195.0	200.0	45.0

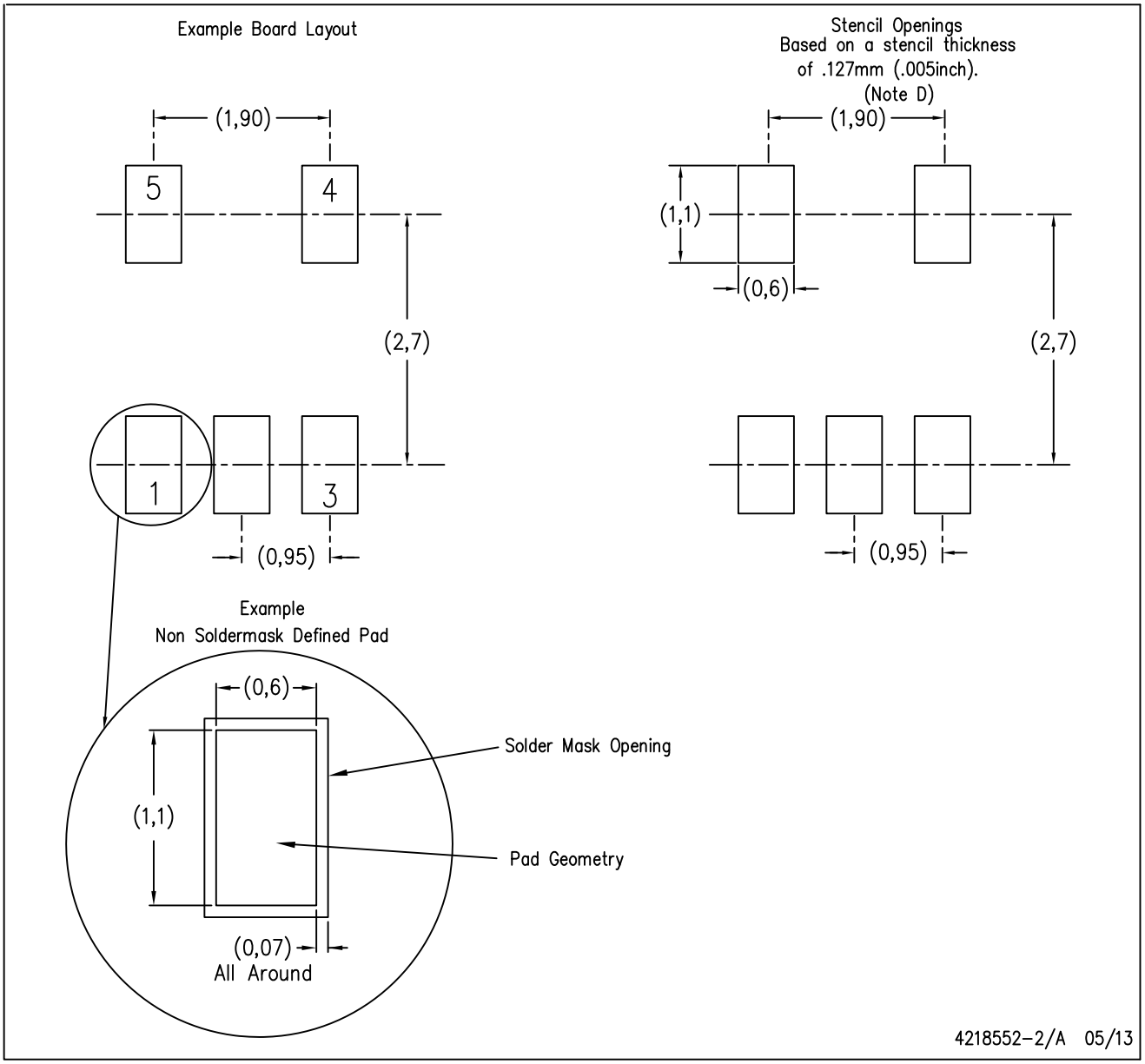
DDC (R–PDSO–G5) PLASTIC SMALL–OUTLINE



4204403–2/E 06/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–193 variation AB (5 pin).

DDC (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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