DRV8811 Stepper Motor Controller IC

1 Features

- Pulse Width Modulation (PWM) Microstepping Motor Driver
  - Up to 1/8-Step Microstepping Indexer
  - Step and Direction Control
  - Programmable Mixed Decay, Blanking, and Off-Time
- Up to 1.9-A Current Per Winding
- Low 1.0-Ω (HS+LS) MOSFET $R_{DS(on)}$ (25°C)
- 8-V to 38-V Operating Supply Voltage Range
- Pin-to-Pin Compatible With the DRV8818
- Thermally Enhanced Surface Mount Package
- Protection Features:
  - VM Undervoltage Lockout (UVLO)
  - Overcurrent Protection (OCP)
  - Thermal Shutdown (TSD)

2 Applications

- Printers
- Scanners
- Office Automation Machines
- Gaming Machines
- Factory Automation
- Robotics

3 Description

The DRV8811 device provides an integrated stepper motor driver solution for printers, scanners, and other automated equipment applications. The device has two H-bridge drivers, as well as microstepping indexer logic to control a stepper motor.

The output driver block consists of N-channel power MOSFETs configured as full H-bridges to drive the motor windings.

A simple STEP-and-DIR interface allows easy interfacing to controller circuits. Step mode pins allow for configuration of the motor in full-step, half-step, quarter-step, or eighth-step modes. Decay mode and PWM off-time are programmable.

Internal shutdown functions are provided for overcurrent protection, short-circuit protection, undervoltage lockout and overtemperature.

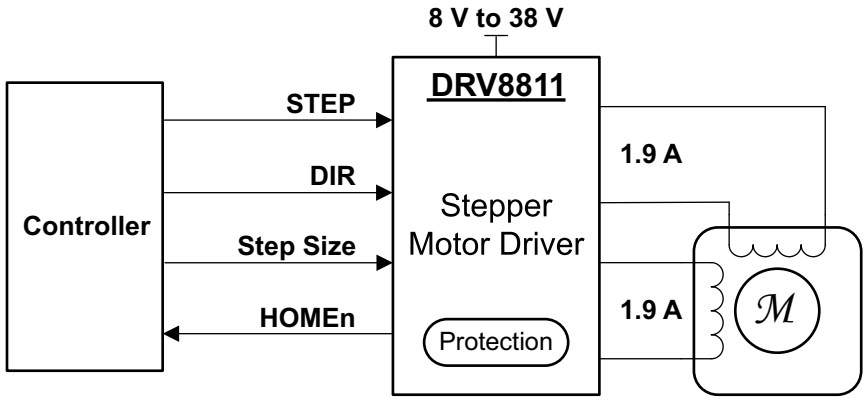
The DRV8811 device is packaged in a PowerPAD™ 28-pin HTSSOP package with thermal pad.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8811	HTSSOP (28)	9.70 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (January 2015) to Revision J — **Page**

- Changed the pinout diagram ... 3
- Added a row for the thermal pad to the *Pin Functions* table ... 4
- Changed multiple entries in the *Absolute Maximum Ratings* table ... 4
- Added two rows to the *Recommended Operating Conditions* table ... 5
- Deleted "active" or "inactive" from several timing requirements definitions ... 7
- Changed Equation 1 ... 12
- Added units to Equation 2 ... 12
- Added units to Equation 3 ... 12
- Added units to Equation 4 ... 13
- Changed V_{VREF} from 1.56 V to 1 V ... 18

Changes from Revision H (November 2013) to Revision I — **Page**

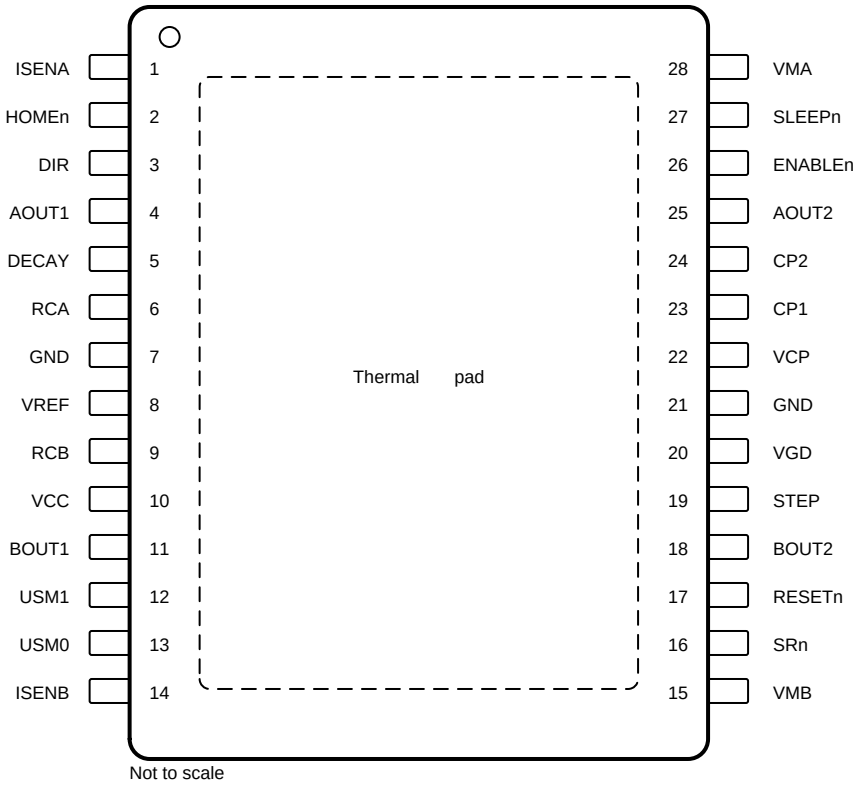
- Changed *Features* list ... 1
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 5

Changes from Revision G (May 2010) to Revision H — **Page**

- Changed Features bullet ... 1
- Changed $I_{O(peak)}$ and deleted I_O in Absolute Maximum Ratings table ... 4
- Changed maximum digital pin voltage ... 4
- Added parameters to Logic-Level Inputs section of the ELECTRICAL CHARACTERISTICS ... 5
- Changed *Timing Requirements* ... 7

5 Pin Configuration and Functions

PWP PowerPAD™ Package
28-Pin HTSSOP With Exposed Thermal Pad
Top View



Not to scale

Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
AOUT1	4	O	Bridge A output 1. Connect to bipolar stepper motor winding A
AOUT2	25	O	Bridge A output 2. Positive current is AOUT1 → AOUT2
BOUT1	11	O	Bridge B output 1. Connect to bipolar stepper motor winding B
BOUT2	18	O	Bridge B output 2. Positive current is BOUT1 → BOUT2
CP1	23	PWR	Charge pump flying capacitor. Connect a 0.22-μF capacitor between CP1 and CP2
CP2	24	PWR	Charge pump flying capacitor. Connect a 0.22-μF capacitor between CP1 and CP2
DECAY	5	I	Decay mode select. Voltage applied sets decay mode - see motor driver description for details. Bypass to GND with a 0.1-μF ceramic capacitor
DIR	3	I	Direction input. Level sets the direction of stepping
ENABLEn	26	I	Enable input. Logic high to disable device outputs, logic low to enable outputs
GND	7, 21	—	Device ground
HOMEn	2	O	Home position. Logic low when at home state of step table, logic high at other states
ISENA	1	I	Bridge A ground / I_{SENSE}. Connect to current sense resistor for bridge A
ISENB	14	I	Bridge B ground / I_{SENSE}. Connect to current sense resistor for bridge B
RCA	6	I	Bridge A blanking and off time adjust. Connect a parallel resistor and capacitor to GND - see motor driver description for details
RCB	9	I	Bridge B blanking and off time adjust. Connect a parallel resistor and capacitor to GND - see motor driver description for details

(1) Directions: I = input, O = output, I/O = input/output, PWR = power

Pin Functions (continued)

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
RESETn	17	I	Reset input. Active-low reset input initializes the indexer logic and disables the H-bridge outputs
SLEEPn	27	I	Sleep mode input. Logic high to enable device, logic low to enter low-power sleep mode
SRn	16	I	Synchronous rectification enable input. Active-low. When low, synchronous rectification is enabled. Weak internal pulldown.
STEP	19	I	Step input. Rising edge causes the indexer to move one step
USM0	13	I	Microstep mode 0. USM0 and USM1 set the step mode - full step, half step, quarter step, or eight microsteps/step
USM1	12	I	Microstep mode 1. USM0 and USM1 set the step mode - full step, half step, quarter step, or eight microsteps/step
VCC	10	PWR	Logic supply voltage. Connect to 3-V to 5-V logic supply. Bypass to GND with a 0.1-μF ceramic capacitor
VCP	22	PWR	High-side gate drive voltage. Connect a 0.22-μF ceramic capacitor to V_M
VGD	20	PWR	Low-side gate drive voltage. Bypass to GND with a 0.22-μF ceramic capacitor
VMA	28	PWR	Bridge A power supply. Connect to motor supply (8 V to 38 V). Both VMA and VMB must be connected to same supply.
VMB	15	PWR	Bridge B power supply. Connect to motor supply (8 V to 38 V). Both VMA and VMB must be connected to same supply.
VREF	8	I	Current set reference input. Reference voltage for winding current set
Thermal pad	—	—	Thermal pad. Connect to system ground with large copper plane for improved thermal dissipation.

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1) (2) (3)

		MIN	MAX	UNIT
Power supply voltage range	VMA, VMB	–0.3	40	V
Power supply voltage range	VCC	–0.3	7	V
Digital pin voltage range	V_I: DIR, DECAY, ENABLEn, HOME, RCA, RCB, RESETn, SLEEPn, SRn, STEP, USM0, USM1	–0.5	7	V
Reference pin voltage range	VREF	–0.3	7	V
Sense pin voltage range	ISENA, ISENB (4)	–0.875	0.875	V
Output pin voltage range	AOUT1, AOUT2, BOUT1, BOUT2	–0.7	V_{VM} + 0.7	V
Gate-drive pin-voltage range	VGD	–0.3	8	V
Charge pump pin voltage range	VCP, CP2	–0.3	V_{VM} + 12	V
	CP1	–0.3	V_{VM}	
Peak motor drive output current, $I_{O(peak)}$		Internally limited		
Operating virtual junction temperature range, T_J		–40	150	°C
Operating ambient temperature range, T_A		–40	85	°C
Storage temperature range, T_{stg}		–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Power dissipation and thermal limits must be observed.
(4) Transients of ±1 V for less than 25 ns are acceptable.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VMx}	Motor power supply voltage range[1]	8		38	V
V_{CC}	Logic power supply voltage range	3		5.5	V
V_{VREF}	VREF input voltage	0		V_{CC}	V
R_X	R_X resistance value	12	56	100	kΩ
C_X	C_X capacitance value	470	680	1500	pF

(1) Both VMx pins must be connected to the same supply voltage.

6.4 Thermal Information

THERMAL METRIC[1]		DRV8811 PWP (HTSSOP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	19.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.8	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

6.5 Electrical Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VM}	V_M operating supply current	V_M = 35 V, f_{PWM} < 50 KHz		4.5	8	mA
I_{VCC}	V_{CC} operating supply current	f_{PWM} < 50 KHz		0.4	4	mA
I_{VMQ}	V_M sleep mode supply current	V_M = 35 V		12	20	µA
I_{VCCQ}	V_{CC} sleep mode supply current			5	20	µA
V_{UVLO}	V_M undervoltage lockout voltage	V_M rising		6.7	8	V
	V_{CC} undervoltage lockout voltage	V_{CC} rising		2.71	2.95	
VREF INPUT, CURRENT CONTROL ACCURACY						
I_{VREF}	VREF input current	V_{VREF} = 3.3 V	–3		3	µA
ΔI_{CHOP}	Chopping current accuracy	V_{VREF} = 2 V, 70% to 100% current	–5%		5%	
		V_{VREF} = 2 V, 20% to 56% current	–10%		10%	
LOGIC-LEVEL INPUTS						
V_{IL}	Input low voltage				0.3 × V_{CC}	V
V_{IH}	Input high voltage		0.7 × V_{CC}			V
I_{IL}	Input low current	V_I = 0.3 × V_{CC}	–20		20	µA
I_{IH}	Input high current	VIN = 0.3 × V_{CC}	–20		20	µA
R_{PU}	Pullup resistance	ENABLEn, RESETn		1		MΩ
R_{PD}	Pulldown resistance	DIR, STEP, SLEEPn, USM1, USM0, SRn		1		MΩ

Electrical Characteristics (continued)

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HOMEn OUTPUT						
V_{OL}	Output low voltage	I_O = 200 μA			0.3 × VCC	V
V_{OH}	Output high voltage	I_O = –200 μA	0.7 × VCC			V
DECAY INPUT						
V_{IL}	Input low threshold voltage	For fast decay mode		0.21 × VCC		V
V_{IH}	Input high threshold voltage	For slow decay mode		0.6 × VCC		V
H-BRIDGE FETS						
$r_{DS(on)}$	HS FET on resistance	V_M = 24 V, I_O = 2.5 A, T_J = 25°C		0.50		Ω
		V_M = 24 V, I_O = 2.5 A, T_J = 85°C		0.60	0.75	
$r_{DS(on)}$	LS FET on resistance	V_M = 24 V, I_O = 2.5 A, T_J = 25°C		0.50		Ω
		V_M = 24 V, I_O = 2.5 A, T_J = 85°C		0.60	0.75	
I_{OFF}			–20		20	μA
MOTOR DRIVER						
t_{OFF}	Off-time	Rx = 56 kΩ, Cx = 680 pF	30	38	46	μs
t_{BLANK}	Current-sense blanking time	Rx = 56 kΩ, Cx = 680 pF	700	950	1200	ns
t_{DT}	Dead time(1)	SRn = 0	100	475	800	ns
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level		2.5	4.5	6.5	A
t_{TSD}	Thermal shutdown temperature(1)	Die temperature	150	160	180	°C

(1) Not tested in production - guaranteed by design.

6.6 Timing Requirements

over operating ambient temperature range (unless otherwise noted) (see Figure 1)

			MIN	TYP	MAX	UNIT
1	f_{STEP}	Step frequency			500	kHz
2	$t_{WH(STEP)}$	Pulse duration, STEP high	1			µs
3	$t_{WL(STEP)}$	Pulse duration, STEP low	1			µs
4	$t_{SU(STEP)}$	Setup time, command before STEP rising	200			ns
5	$t_{H(STEP)}$	Hold time, command after STEP rising	200			ns
6	t_{WAKE}	Wakeup time, SLEEPn high to STEP input accepted			1	ms
7	t_{SLEEP}	Sleep time, SLEEPn low to outputs disabled			5	µs
8	t_{ENABLE}	Enable time, ENABLEn high to outputs enabled			20	µs
9	$t_{DISABLE}$	Disable time, ENABLEn low to outputs disabled			20	µs
10	t_{RESETR}	Reset release time, RESETn high to outputs enabled			5	µs
11	t_{RESET}	Reset time, RESETn low to outputs disabled			5	µs

6.7 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MOTOR DRIVER						
t_{OFF}	Off-time	Rx = 56 kΩ, Cx = 680 pF	30	38	46	µs
t_{BLANK}	Current-sense blanking time	Rx = 56 kΩ, Cx = 680 pF	700	950	1200	ns
t_{DT}	Dead time(1)	SRn = 0	100	475	800	ns

(1) Not tested in production - guaranteed by design.

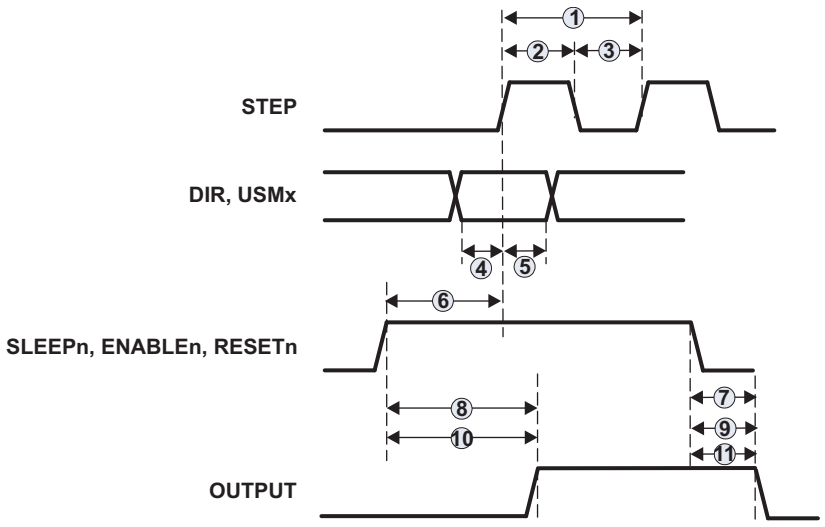


Figure 1. Timing Diagram

6.8 Typical Characteristics

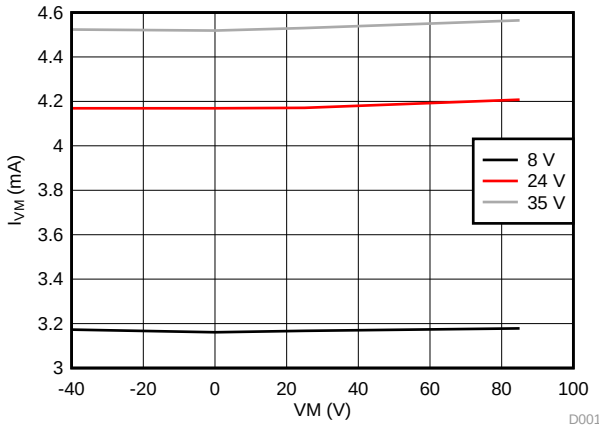


Figure 2. I_{VM} vs VM

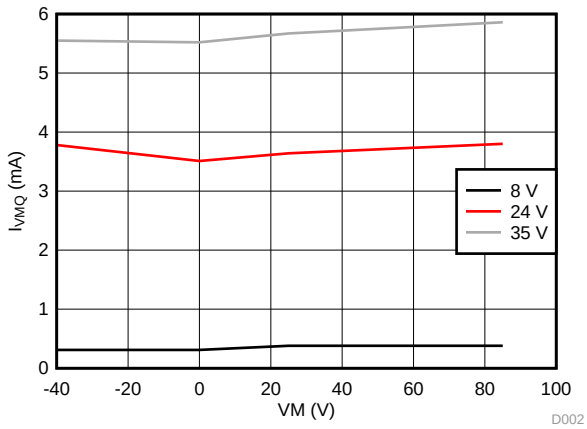


Figure 3. I_{VMQ} vs VM

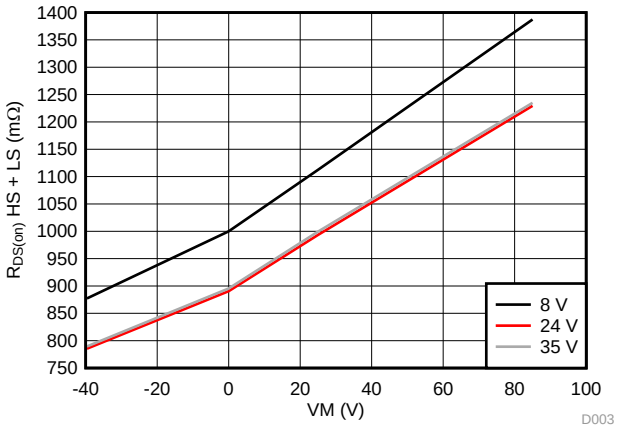


Figure 4. $r_{DS(on)}$ HS and LS vs VM

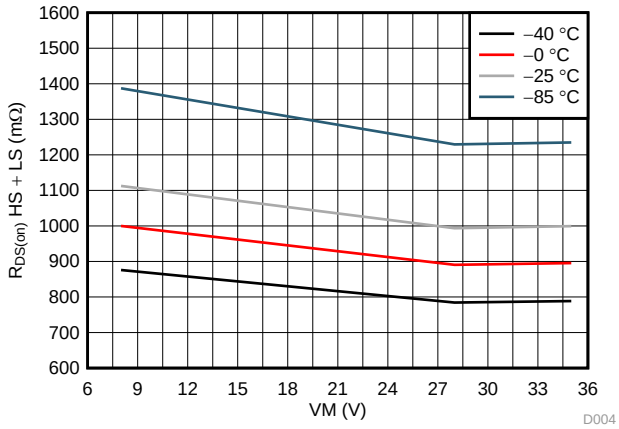


Figure 5. $r_{DS(on)}$ HS and LS vs Temperature

7 Detailed Description

7.1 Overview

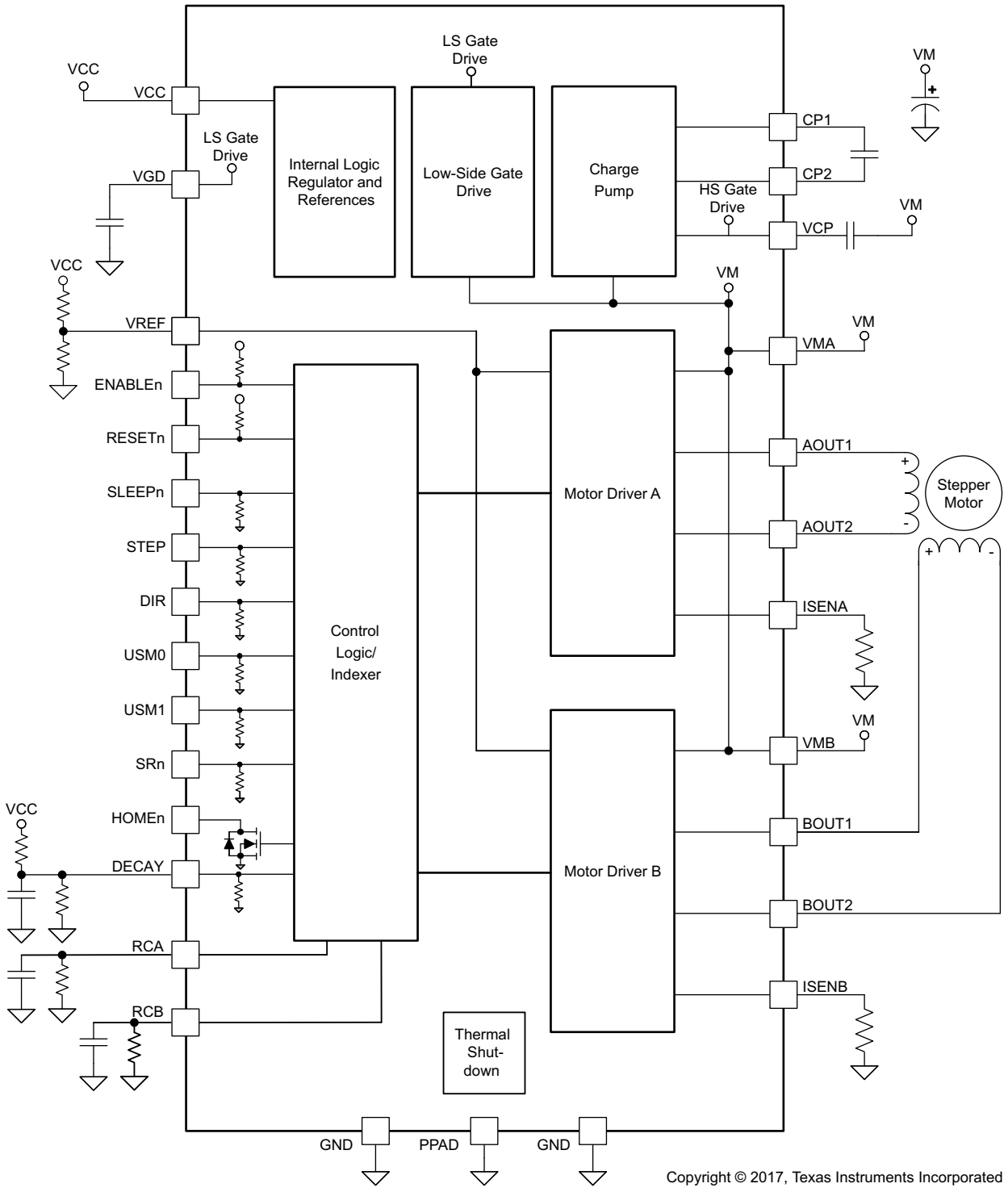
The DRV8811 device is a highly configurable, integrated motor driver solution for bipolar stepper motors. The device integrates two H-bridges, current sense and regulation circuitry, and a microstepping indexer. The DRV8811 device can be powered with a supply voltage between 8 V and 38 V and is capable of providing an output current up to 1.9 A full-scale.

A simple STEP and DIR interface allows for easy interfacing to the controller. The internal indexer is able to execute high-accuracy microstepping without requiring the controller to manage the current regulation loop.

The current regulation is highly configurable, with three decay modes of operation. They are fast, slow, and mixed decay, which can be selected depending on the application requirements. The DRV8811 device also provides configurable blanking, off time, and mixed decay, in order to adjust to a wide range of motors.

A low-power sleep mode is incorporated which allows for minimal power consumption when the system is idle.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM H-Bridge Drivers

The DRV8811 device contains two H-bridge motor drivers with current-control PWM circuitry, and a microstepping indexer. A block diagram of the motor control circuitry is shown in Figure 6.

Feature Description (continued)

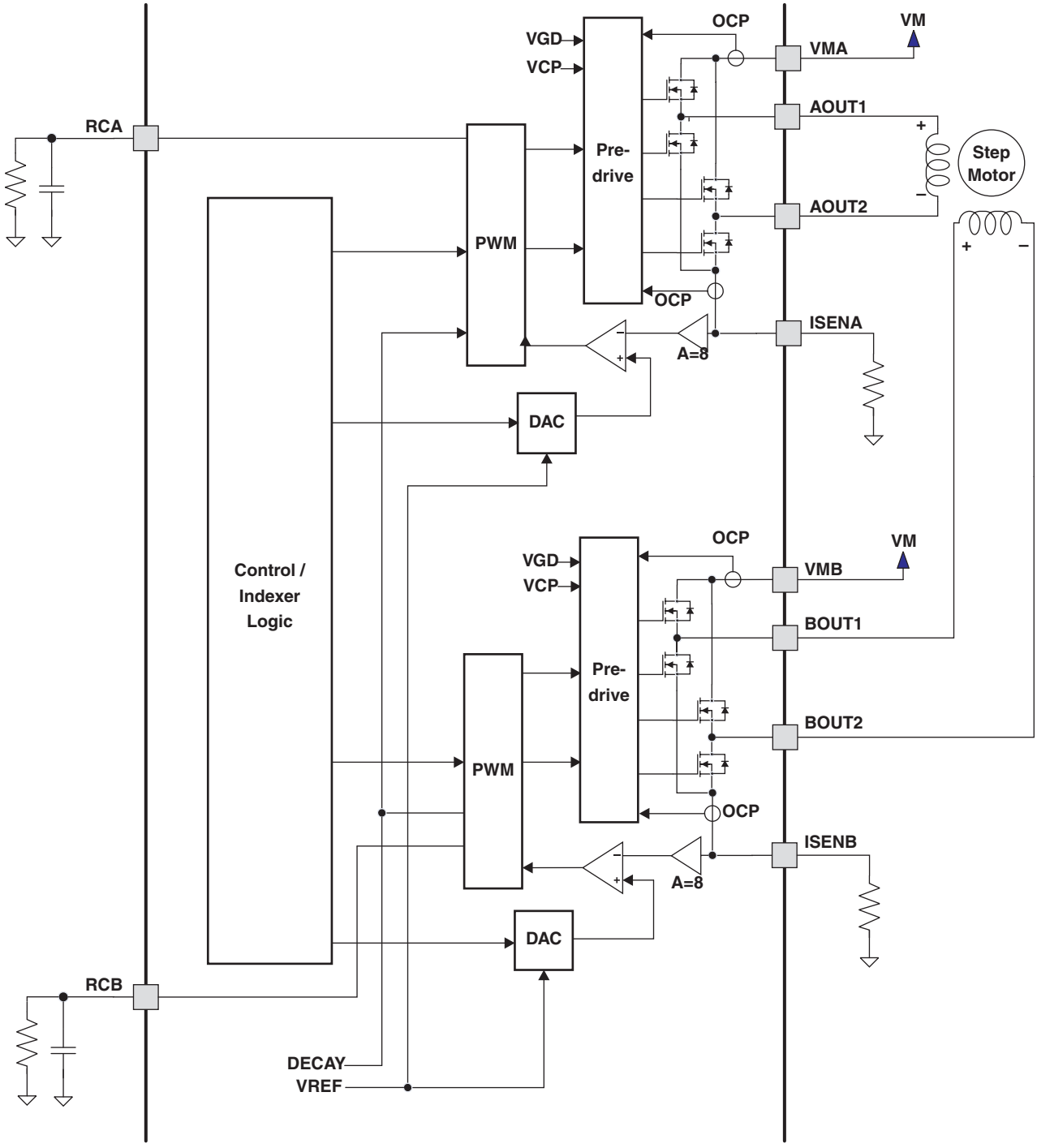


Figure 6. Motor Control Circuitry

7.3.2 Current Regulation

The PWM chopping current is set by a comparator, which compares the voltage across a current-sense resistor, multiplied by a factor of 8, with a reference voltage. The reference voltage is input from the VREF pin. The full-scale (100%) chopping current is calculated as follows:

Feature Description (continued)

$$I_{CHOP}\ (A) = \frac{V_{VREF}\ (V)}{8 \times R_{SENSE}\ (\Omega)} \quad (1)$$

Example:

If a 0.22-Ω sense resistor is used and the VREF pin is 3.3 V, the full-scale (100%) chopping current is 3.3 V / (8 × 0.22 Ω) = 1.875 A.

The reference voltage is also scaled by an internal DAC that allows torque control for fractional stepping of a bipolar stepper motor, as described in the *Microstepping Indexer* section.

When a winding is activated, the current through it rises until it reaches the chopping current threshold described previously; then the current is switched off for a fixed off-time. The off-time is determined by the values of a resistor and capacitor connected to the RCA (for bridge A) and RCB (for bridge B) pins. The off-time is approximated by:

$$t_{OFF}\ (\mu s) = R\ (\Omega) \times C\ (nF) \quad (2)$$

To avoid falsely tripping on transient currents when the winding is first activated, a blanking period is used immediately after turning on the FETs, during which the state of the current-sense comparator is ignored. The blanking time is determined by the value of the capacitor connected to the RCx pin and is approximated by:

$$t_{BLANK}\ (ns) = 1400\ (\Omega) \times C\ (nF) \quad (3)$$

7.3.3 Decay Mode

During PWM current chopping, the H-bridge is enabled to drive through the motor winding until the PWM current chopping threshold is reached. This is shown in Figure 7, Item 1. The current flow direction shown indicates positive current flow in Table 2.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay.

In fast decay mode, once the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. If synchronous rectification is enabled (SRn pin logic low), the opposite FETs are turned on; as the winding current approaches zero, the bridge is disabled to prevent any reverse current flow. If SRn is high, current is recirculated through the body diodes, or through external Schottky diodes. Fast-decay mode is shown in Figure 7, Item 2.

In slow-decay mode, winding current is recirculated by enabling both of the low-side FETs in the bridge. This is shown in Figure 7, Item 3.

Feature Description (continued)

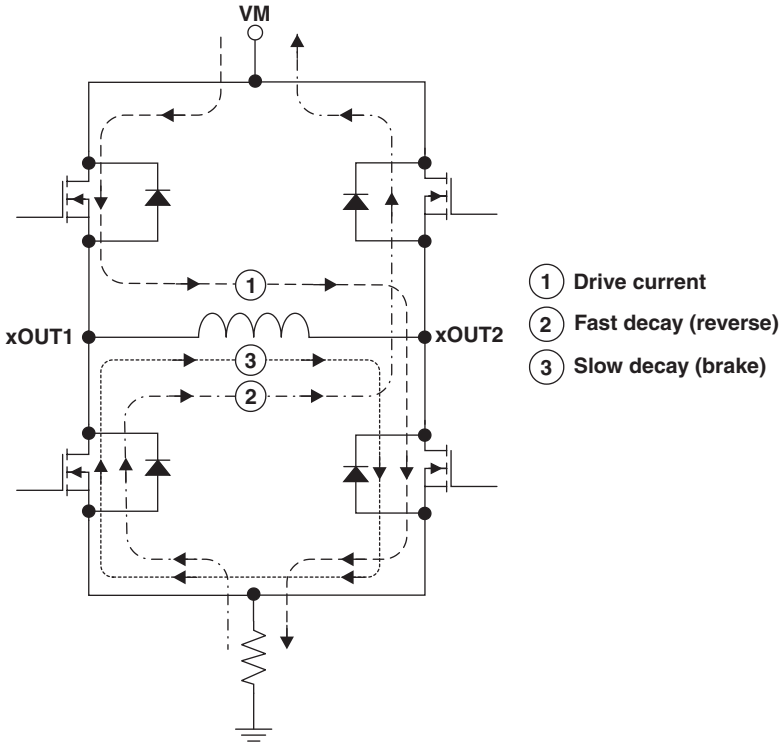


Figure 7. Decay Mode

The DRV8811 device also supports a mixed decay mode. Mixed decay mode begins as fast decay, but after a period of time switches to slow decay mode for the remainder of the fixed off-time.

Fast and mixed decay modes are only active if the current through the winding is decreasing; if the current is increasing, then slow decay is always used.

Which decay mode is used is selected by the voltage on the DECAY pin. If the voltage is greater than 0.6 × V_{CC}, slow decay mode is always used. If DECAY is less than 0.21 × V_{CC}, the device operates in fast decay mode when the current through the winding is decreasing. If the voltage is between these levels, mixed decay mode is enabled.

In mixed decay mode, the voltage on the DECAY pin sets the point in the cycle that the change to slow decay mode occurs. This time can be approximated by:

$$t_{FD}\ (\mu s) = R\ (\Omega) \times C\ (nF) \times \ln\left(\frac{0.6 \times V_{CC}\ (V)}{V_{DECAY}\ (V)}\right) \quad (4)$$

Operation of the blanking, fixed off time, and mixed decay mode is illustrated in Figure 8.

Feature Description (continued)

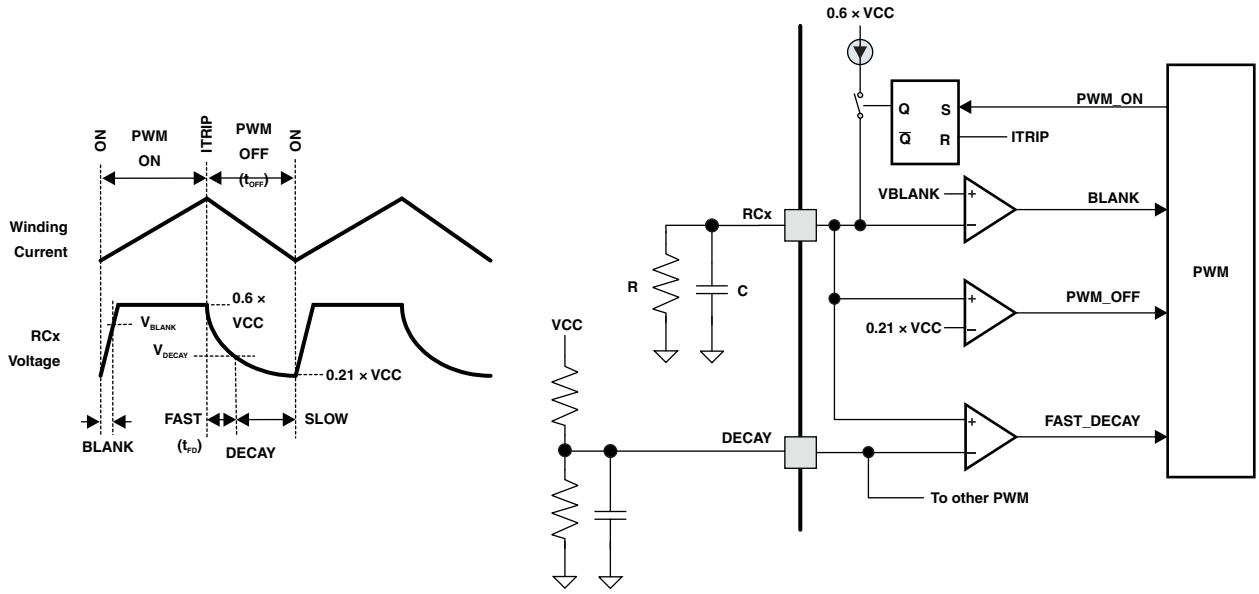


Figure 8. PWM

7.3.4 Microstepping Indexer

Built-in indexer logic in the DRV8811 device allows a number of different stepping configurations. The USM1 and USM0 pins are used to configure the stepping format as shown in Table 1:

Table 1. Microstepping Selection Bits

USM1	USM0	STEP MODE
0	0	Full step (2-phase excitation)
0	1	1/2 step (1-2 phase excitation)
1	0	1/4 step (W1-2 phase excitation)
1	1	1/8 step (phase excitation)

Table 2 shows the relative current and step directions for different settings of USM1 and USM0. At each rising edge of the STEP input, the indexer travels to the next state in the table. The direction is shown with the DIR pin high; if the DIR pin is low the sequence is reversed. Positive current is defined as xOUT1 = positive with respect to xOUT2.

Note that the home state is 45 degrees. This state is entered at power up or device reset. The HOMEn output pin is driven low in this state. In all other states it is driven logic high.

Table 2. Microstepping Indexer

FULL STEP USM = 00	1/2 STEP USM = 01	1/4 STEP USM = 10	1/8 STEP USM = 11	AOUTx CURRENT (% FULL-SCALE)	BOUTx CURRENT (% FULL-SCALE)	STEP ANGLE (DEGREES)
	1	1	1	100	0	0
			2	98	20	11.325
		2	3	92	38	22.5
			4	83	56	33.75
1	2	3	5	71	71	45 (home state)
			6	56	83	56.25
		4	7	38	92	67.5
			8	20	98	78.75

Table 2. Microstepping Indexer (continued)

FULL STEP USM = 00	1/2 STEP USM = 01	1/4 STEP USM = 10	1/8 STEP USM = 11	AOUTx CURRENT (% FULL-SCALE)	BOUTx CURRENT (% FULL-SCALE)	STEP ANGLE (DEGREES)
	3	5	9	0	100	90
			10	–20	98	101.25
		6	11	–38	92	112.5
			12	–56	83	123.75
2	4	7	13	–71	71	135
			14	–83	56	146.25
		8	15	–92	38	157.5
			16	–98	20	168.75
	5	9	17	–100	0	180
			18	–98	–20	191.25
		10	19	–92	–38	202.5
			20	–83	–56	213.75
3	6	11	21	–71	–71	225
			22	–56	–83	236.25
		12	23	–38	–92	247.5
			24	–20	–98	258.75
	7	13	25	0	–100	270
			26	20	–98	281.25
		14	27	38	–92	292.5
			28	56	–83	303.75
4	8	15	29	71	–71	315
			30	83	–56	326.25
		16	31	92	–38	337.5
			32	98	–20	348.75

7.3.5 Protection Circuits

7.3.5.1 Overcurrent Protection (OCP)

If the current through any FET exceeds the preset overcurrent threshold, all FETs in the H-bridge are disabled until the ENABLEn pin has been brought high and then back low, or power is removed and re-applied. Overcurrent conditions are sensed in both directions; that is, any short to ground, supply, or across the motor winding results in an overcurrent shutdown.

Note that overcurrent protection does not use the current-sense circuitry used for PWM current control and is independent of the I_{SENSE} resistor value or V_{VREF} voltage. Additionally, in the case of an overcurrent event, the microstepping indexer is reset to the home state.

7.3.5.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all drivers in the device are shut down and the indexer is reset to the home state. Once the die temperature has fallen to a safe level, operation resumes.

7.3.5.3 Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pins falls below the undervoltage-lockout threshold voltage, all circuitry in the device is disabled and the indexer is reset to the home state. Operation resumes when VM rises above the UVLO threshold.

7.4 Device Functional Modes

7.4.1 RESETn, ENABLEn and SLEEPn Operation

The RESETn pin, when driven low, resets the indexer to the home position shown in Table 2. It also disables the H-bridge drivers. The STEP input is ignored while RESETn is active.

The ENABLEn pin is used to control the output drivers. When ENABLEn is low, the output H-bridges are enabled. When ENABLEn is high, the H-bridges are disabled and the outputs are in a high-impedance state.

Note that when ENABLEn is high, the input pins and control logic, including the indexer (STEP and DIR pins) are still functional.

The SLEEPn pin is used to put the device into a low-power state. If SLEEPn is low, the H-bridges are disabled, the gate drive charge pump is stopped, and all internal clocks are stopped. In this state, all inputs are ignored until the SLEEPn pin returns high.

8 Application and Implementation

NOTE

Information in the following application section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8811 device is used for bipolar stepper-motor control. The microstepping motor driver provides precise regulation of the coil current and ensures a smooth rotation from the stepper motor.

8.2 Typical Application

Figure 9 shows a common system application of the DRV8811 device.

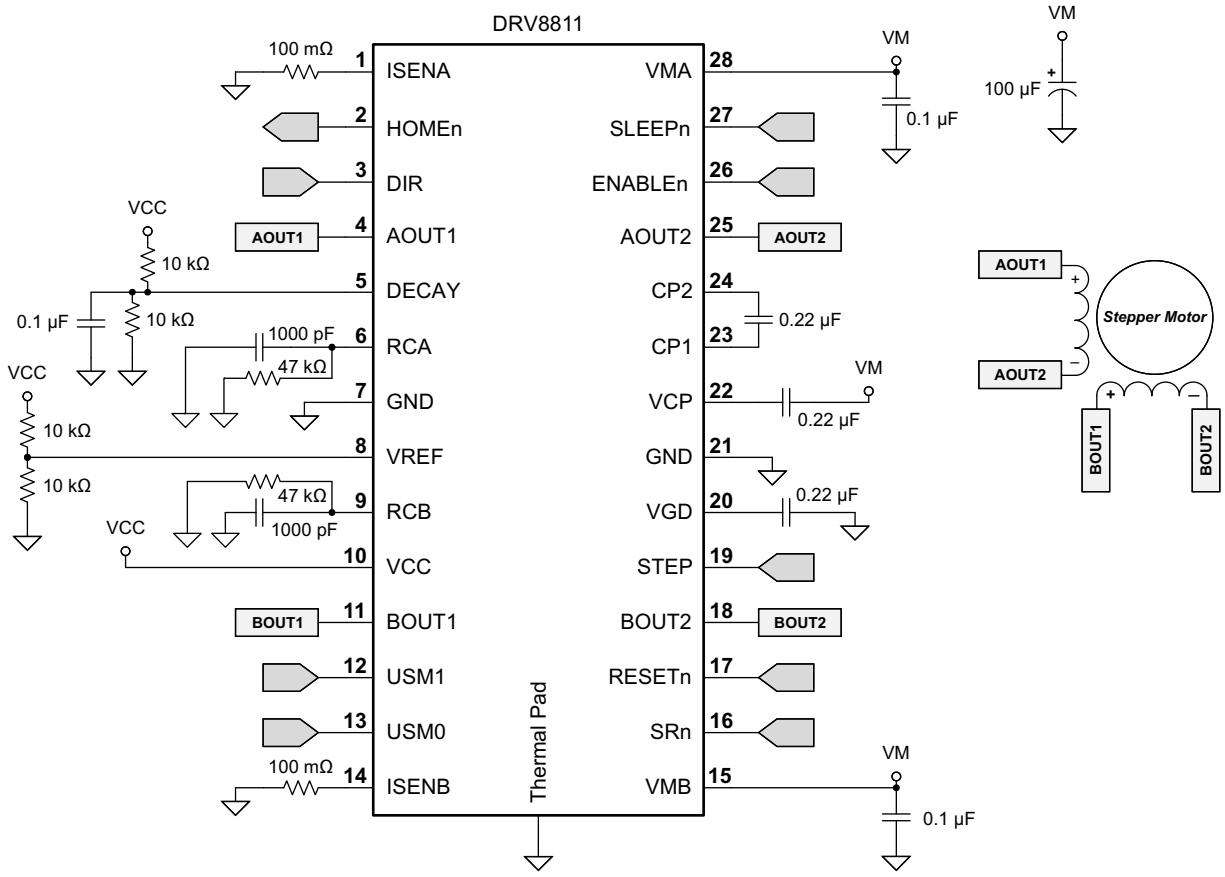


Figure 9. Typical Application Schematic

Typical Application (continued)

8.2.1 Design Requirements

Table 3. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	VM	24 V
Motor winding resistance	R_L	4 Ω
Motor winding inductance	I_L	3.7 mH
Motor full-step angle	θ_{step}	1.8°
Target microstepping level	n_m	8 µsteps per step
Target motor speed	V	120 rpm
Target full-scale current	I_{FS}	1.25 A

8.2.2 Detailed Design Procedure

8.2.2.1 Stepper Motor Speed

The first step in configuring the DRV8811 device requires the desired motor speed and microstepping level. If the target application requires a constant speed, then a square wave with frequency f_{step} must be applied to the STEP pin.

If the target motor start-up speed is too high, the motor does not spin. Make sure that the motor can support the target speed, or implement an acceleration profile to bring the motor up to speed.

For a desired motor speed (v), microstepping level (nm), and motor full step angle (θ_{step}),

$$f_{step}\left(\mu steps/second\right)=\frac{v\left(\frac{rotations}{minute}\right)\times 360\left(\frac{^\circ}{rotation}\right)\times n_m\left(\frac{\mu steps}{step}\right)}{60\left(\frac{seconds}{minute}\right)\times\theta_{step}\left(\frac{^\circ}{step}\right)} \quad (5)$$

$$f_{step}\left(\mu steps/second\right)=\frac{120\left(\frac{rotations}{minute}\right)\times 360\left(\frac{^\circ}{rotation}\right)\times 8\left(\frac{\mu steps}{step}\right)}{60\left(\frac{seconds}{minute}\right)\times 1.8\left(\frac{^\circ}{step}\right)} \quad (6)$$

θ_{step} can be found in the stepper motor data sheet or written on the motor itself.

For the DRV8811 device, the microstepping level is set by the USMx pins. Higher microstepping means a smother motor motion and less audible noise, but increases switching losses and require a higher f_{step} to achieve the same motor speed.

8.2.2.2 Current Regulation

In a stepper motor, the set full-scale current (I_{FS}) is the maximum current driven through either winding. This quantity depends on the V_{VREF} analog voltage and the sense resistor value (R_{SENSE}). During stepping, I_{FS} defines the current chopping threshold (I_{TRIP}) for the maximum current step. The gain of DRV8811 device is set for 8 V/V.

$$I_{FS}\left(A\right)=\frac{V_{VREF}\left(V\right)}{A_v\times R_{SENSE}\left(\Omega\right)}=\frac{V_{VREF}\left(V\right)}{8\times R_{SENSE}\left(\Omega\right)} \quad (7)$$

To achieve I_{FS} = 1.25 A with R_{SENSE} of 0.1 Ω, V_{VREF} should be 1 V.

8.2.2.3 Decay Modes

The DRV8811 device supports three different decay modes: slow decay, fast decay, and mixed decay. The current through the motor windings is regulated using a fixed off-time scheme.

This means that the current increases until it reaches the current chopping threshold (I_{TRIP}), after which it enters the configured decay mode for a fixed period of time. The cycle then repeats after the decay period expires.

The blanking time t_{BLANK} defines the minimum drive time for the current chopping. I_{TRIP} is ignored during t_{BLANK}, so the winding current may overshoot the trip level.

8.2.3 Application Curves

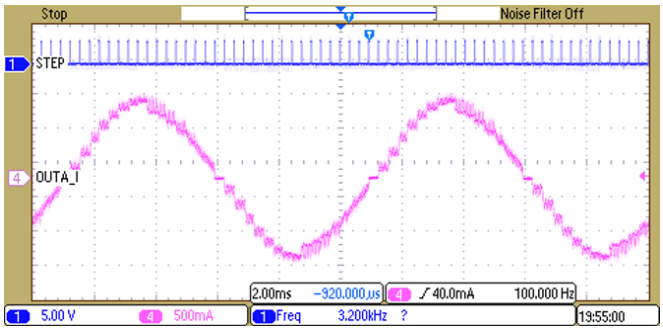


Figure 10. Mixed Decay

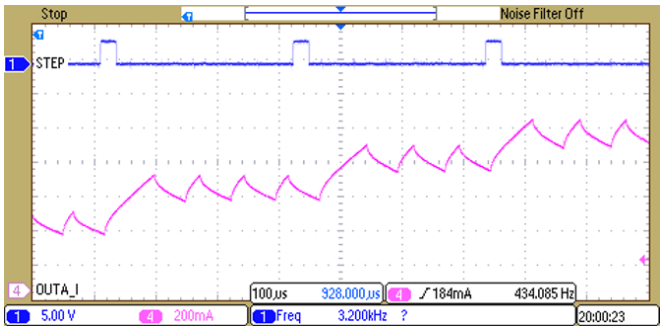


Figure 11. Slow Decay on Increasing Steps

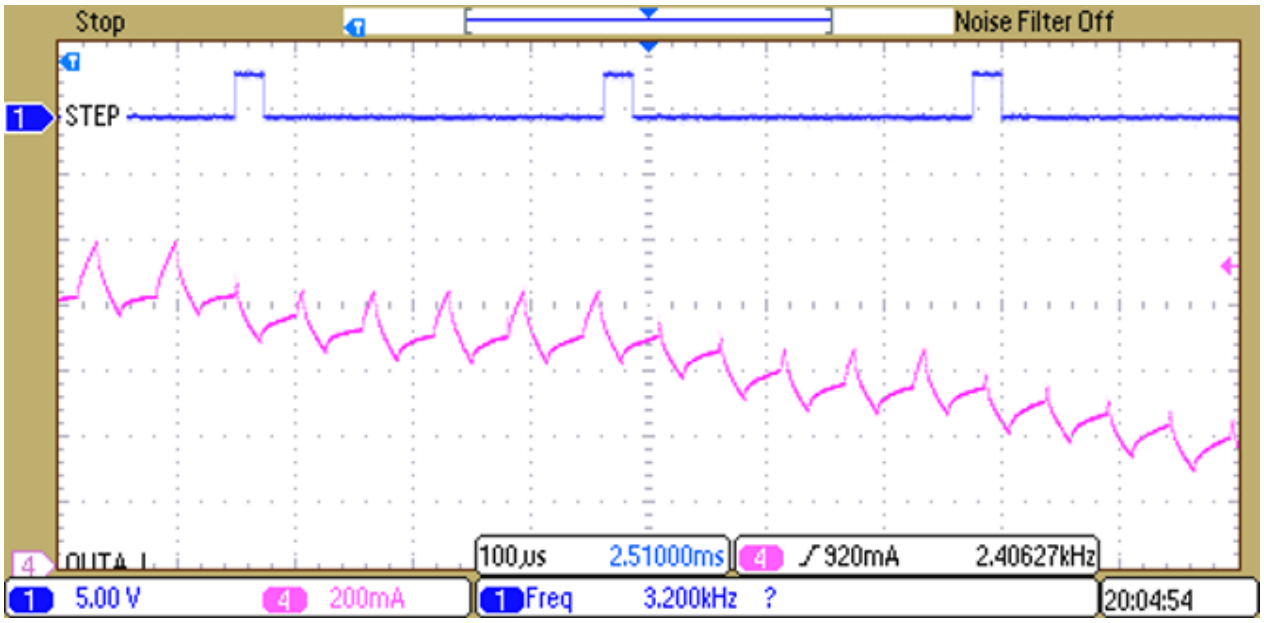


Figure 12. Mixed Decay on Decreasing Steps

9 Power Supply Recommendations

9.1 Bulk Capacitance

Having an appropriate local bulk capacitance is an important factor in motor-drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed dc, brushless dc, stepper)
- The motor braking method

The inductance between the power supply and the motor drive system limits the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The device data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

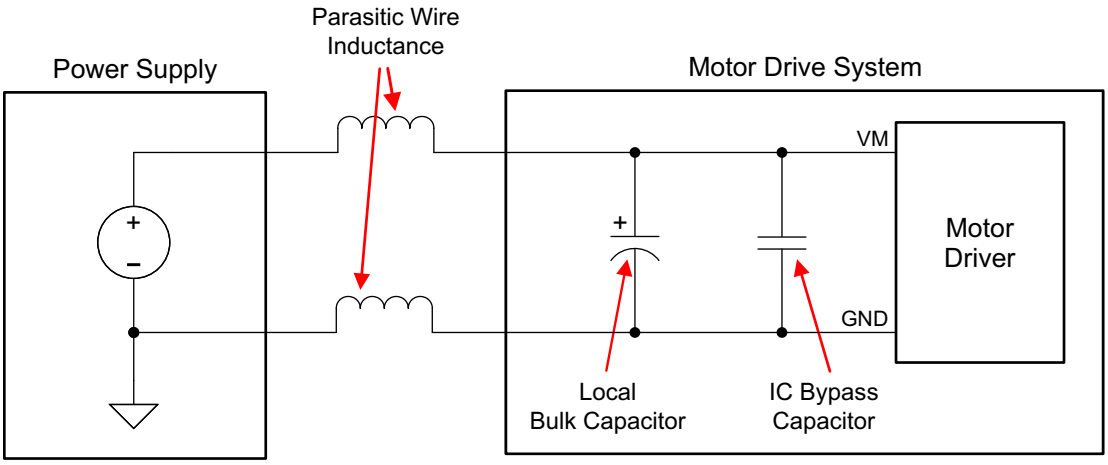


Figure 13. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

10 Layout

10.1 Layout Guidelines

The VMA and VMB pins should be bypassed to GND using low-ESR ceramic bypass capacitors with a recommended value of 0.1 μF rated for VM. This capacitor should be placed as close to the VMA and VMB pins as possible with a thick trace or ground plane connection to the device GND pin.

The VMA and VMB pins must be bypassed to ground using an appropriate bulk capacitor. This component may be an electrolytic and should be located close to the DRV8811 device.

A low-ESR ceramic capacitor must be placed between the CP1 and CP2 pins. TI recommends a value of 0.22 μF rated for VM. Place this component as close to the pins as possible.

A low-ESR ceramic capacitor must be placed between the VM and VCP pins. TI recommends a value of 0.22 μF rated for 16 V. Place this component as close to the pins as possible.

Ensure proper connection of the DRV8811 thermal pad to the PCB. The thermal pad should be connected to a copper plane that is connected to GND. The copper plane should have a large area to allow for thermal dissipation from the DRV8811 device.

10.2 Layout Example

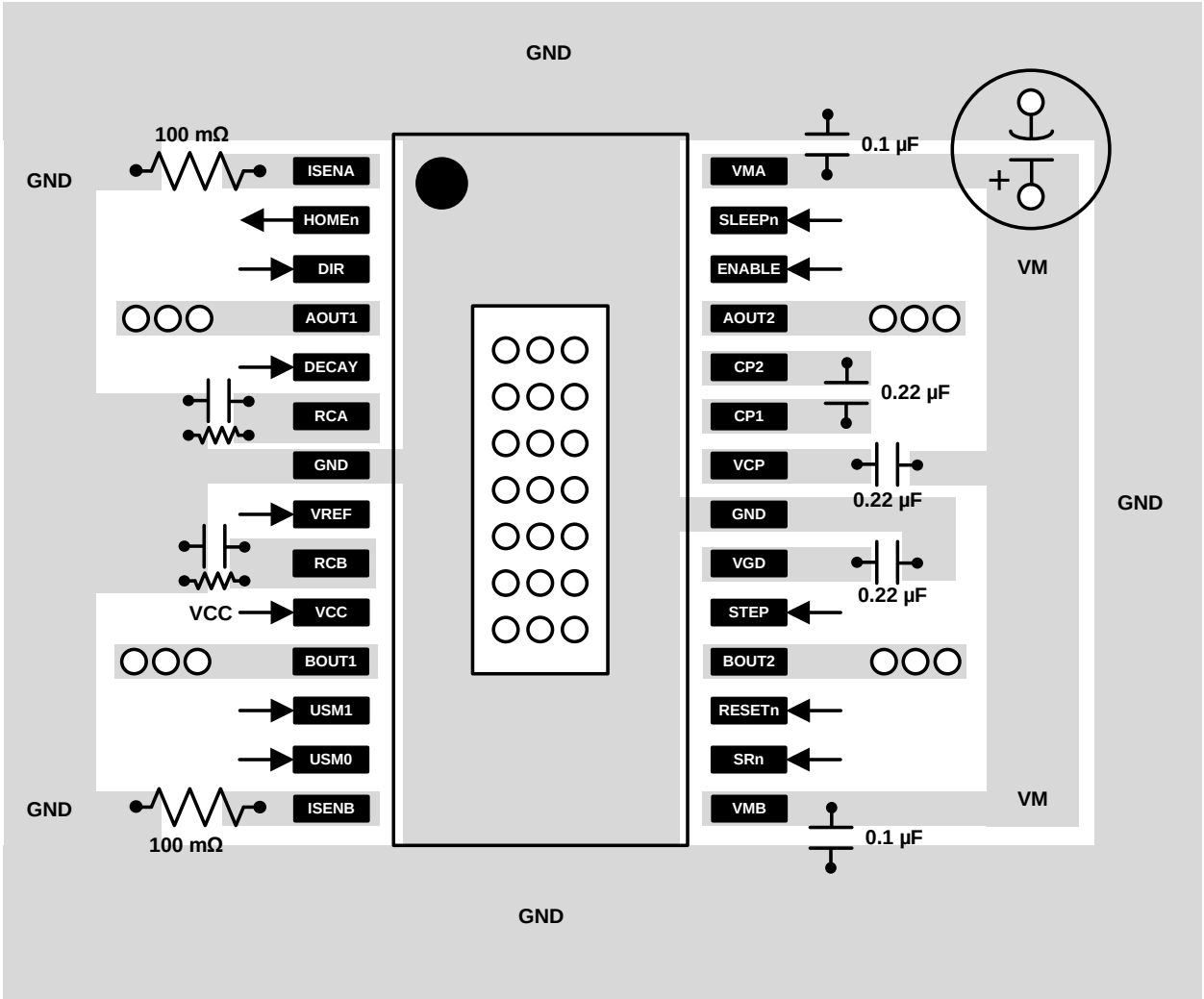


Figure 14. Layout Example Schematic

10.3 Thermal Information

The DRV8811 device has thermal shutdown (TSD) as described in *Thermal Shutdown (TSD)*. If the die temperature exceeds approximately 150°C, the device is disabled until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

10.3.1 Heatsinking

The PowerPAD package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, see TI Application Report SLMA002, *PowerPAD™ Thermally Enhanced Package* and TI Application Brief SLMA004, *PowerPAD™ Made Easy*, available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated. Figure 18 shows thermal resistance vs copper plane area for a single-sided PCB with 2-oz. copper heatsink area. It can be seen that the heatsink effectiveness increases rapidly to about 20 cm^2, then levels off somewhat for larger areas.

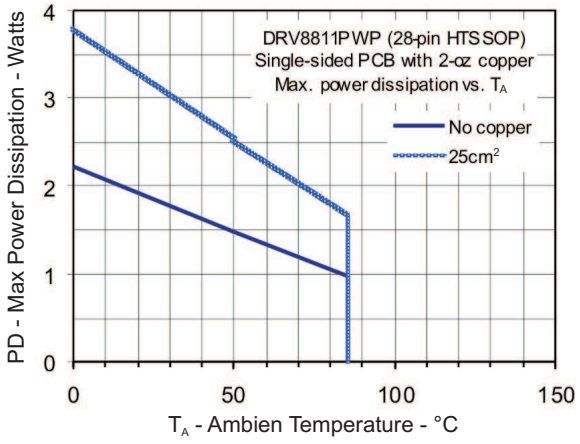


Figure 15. Power Dissipation (2-Layer)

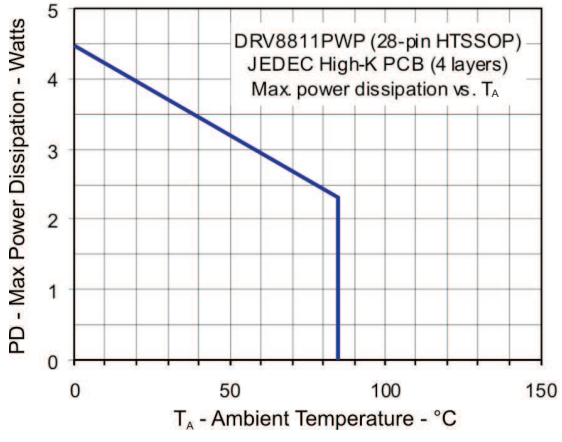


Figure 16. Power Dissipation (4-Layer)

Thermal Information (continued)

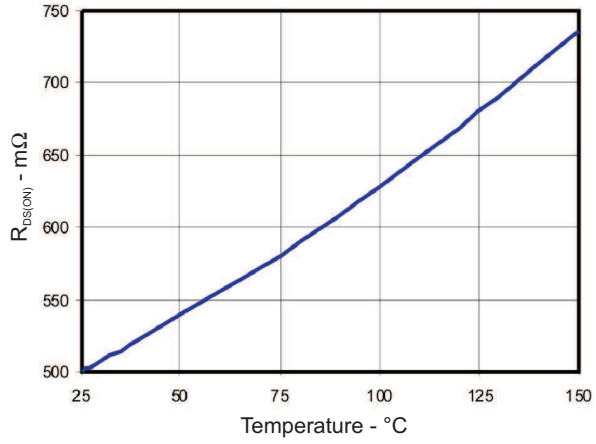


Figure 17. Typical $r_{DS(on)}$ vs Temperature

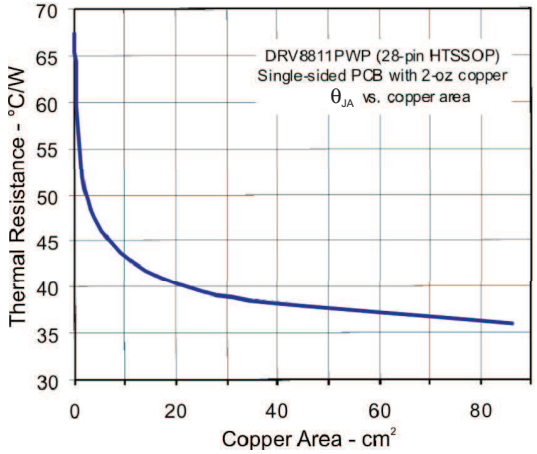


Figure 18. Thermal Resistance vs Copper Area

10.4 Power Dissipation

Power dissipation in the DRV8811 device is dominated by the power dissipated in the output FET resistance, or $r_{DS(on)}$. Average power dissipation when running a stepper motor can be roughly estimated by:

$$P_{TOT} = 4 \times r_{DS(on)} \times (I_{OUT(RMS)})^2 \quad (8)$$

where P_{TOT} is the total power dissipation, $r_{DS(on)}$ is the resistance of each FET, and $I_{OUT(RMS)}$ is the RMS output current being applied to each winding. $I_{OUT(RMS)}$ is equal to the approximately 0.7× the full-scale output current setting. The factor of 4 comes from the fact that there are two motor windings, and at any instant two FETs are conducting winding current for each winding (one high-side and one low-side).

The maximum amount of power that can be dissipated in the DRV8811 device is dependent on ambient temperature and heatsinking. Figure 15 and Figure 16 show how the maximum allowable power dissipation varies according to temperature and PCB construction. Figure 15 shows data for a JEDEC 2-layer low-K board with 2-oz. copper, 76 mm × 114 mm × 1.6 mm thick, with either no backside copper or a 24 cm^2 copper area on the backside. Similarly, Figure 16 shows data for a JEDEC 4-layer high-K board with 1-oz. copper, 76 mm × 114 mm × 1.6 mm thick, and a solid internal ground plane. In this case, the thermal pad is tied to the ground plane using thermal vias, and no additional outer layer copper.

Note that $r_{DS(on)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink. See Figure 17.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

1. *PowerPAD™ Thermally Enhanced Package*
2. *PowerPAD™ Made Easy*
3. *Current Recirculation and Decay Modes*
4. *Calculating Motor Driver Power Dissipation*
5. *Understanding Motor Driver Current Ratings*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8811PWP	ACTIVE	HTSSOP	PWP	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8811	Samples
DRV8811PWPR	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8811	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

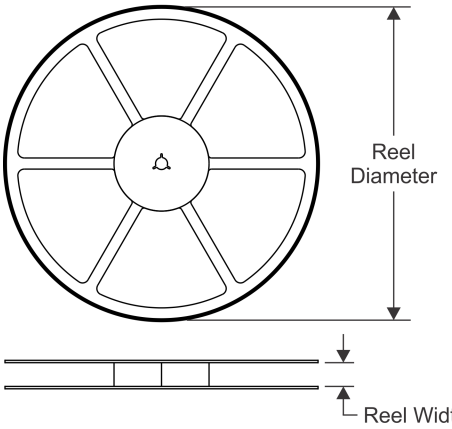
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

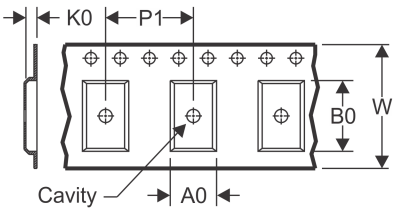
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

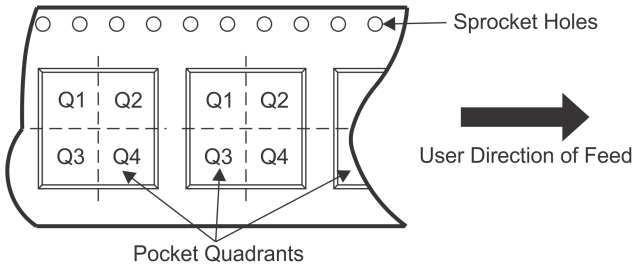


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

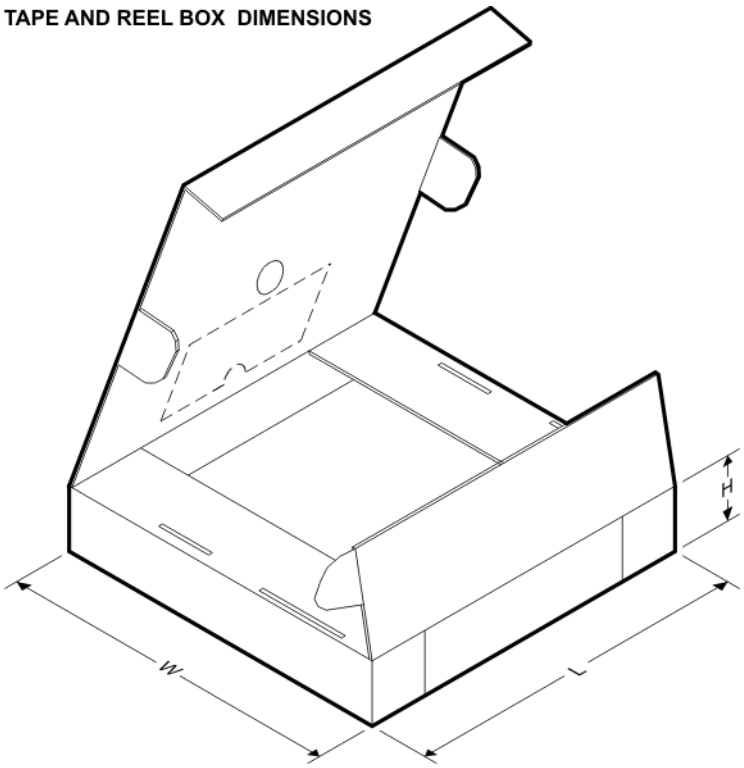
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8811PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

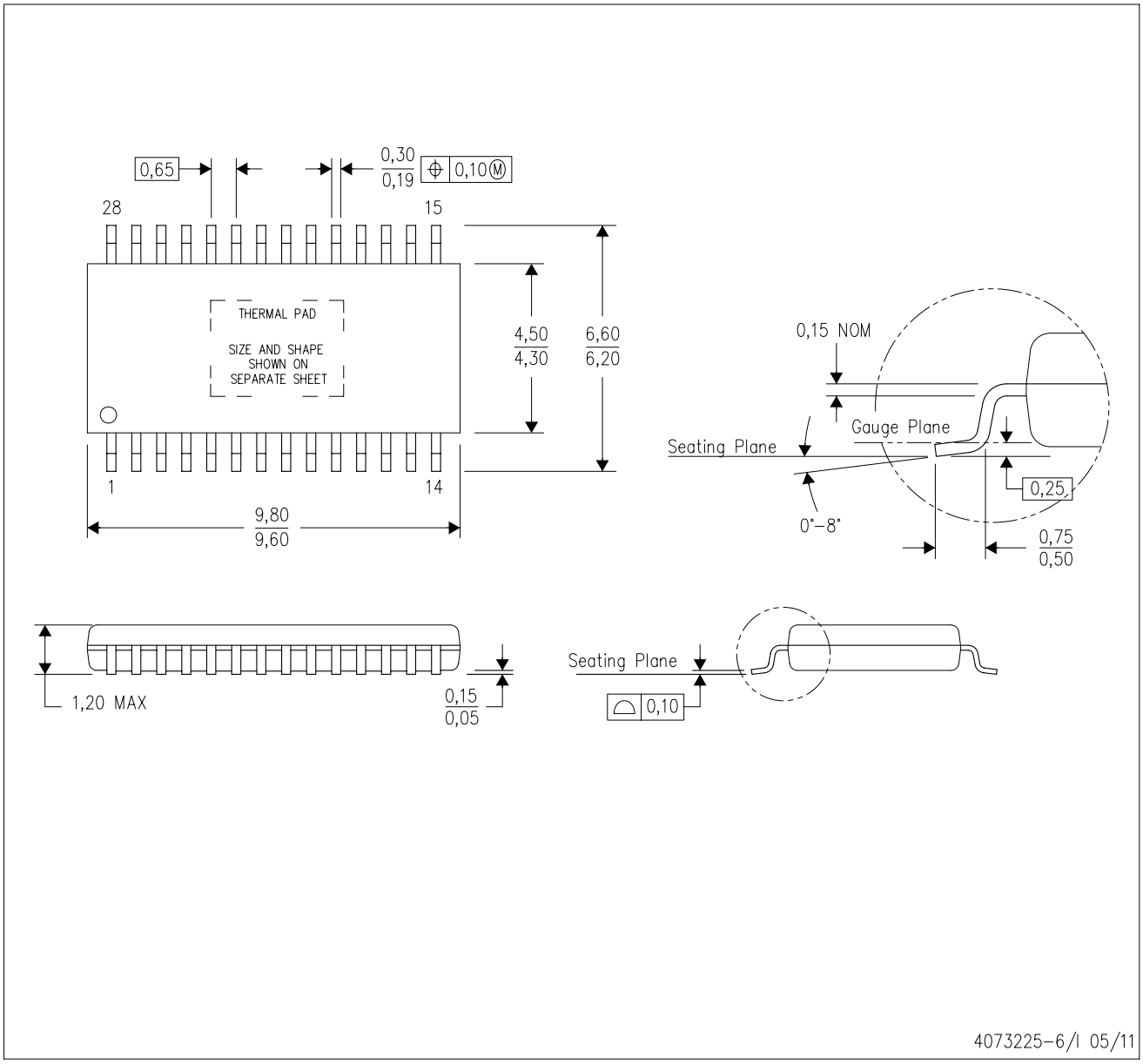
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8811PWPR	HTSSOP	PWP	28	2000	367.0	367.0	38.0

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

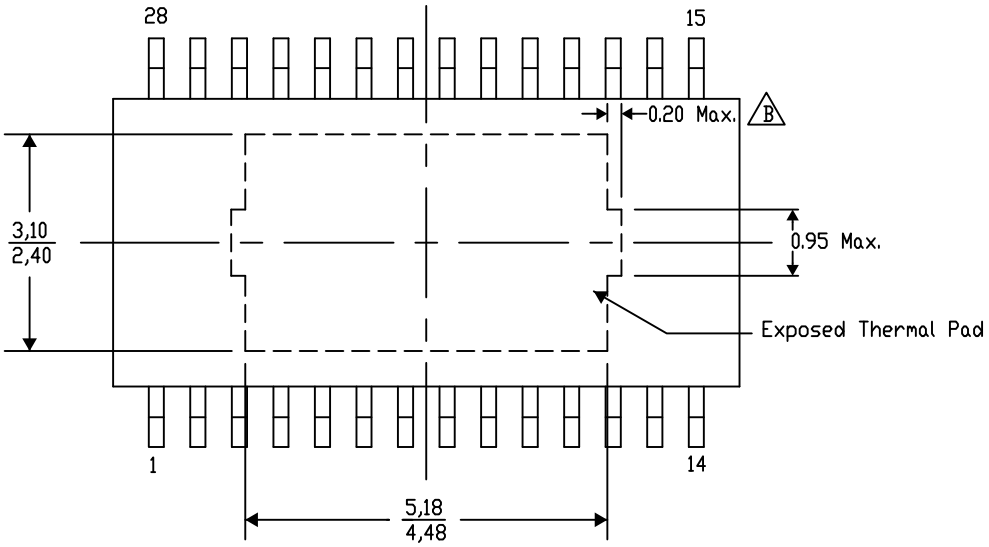
PWP (R–PDSO–G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

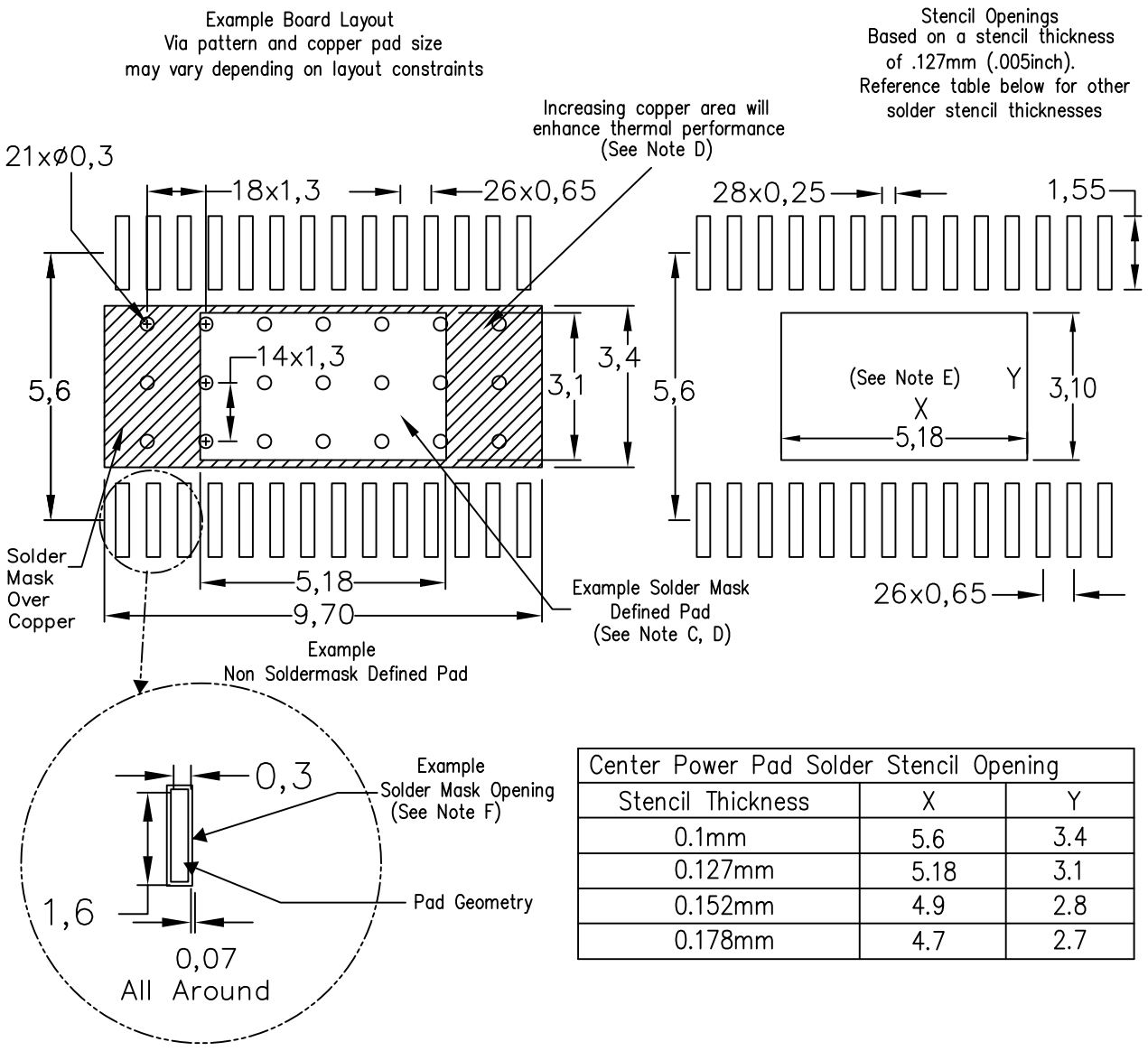
4206332–38/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5.6	3.4
0.127mm	5.18	3.1
0.152mm	4.9	2.8
0.178mm	4.7	2.7

4207609–22/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.
E. For specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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