TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS205I

CD54HC4049, CD74HC4049, CD54HC4050, CD74HC4050

February 1998 - Revised February 2005

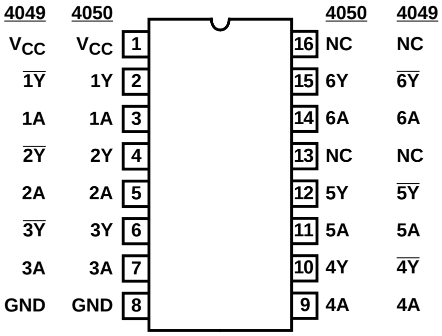
High-Speed CMOS Logic Hex Buffers, Inverting and Non-Inverting

Features

- **Typical Propagation Delay: 6ns at V_{CC} = 5V, C_L = 15pF, T_A = 25^oC**
- **High-to-Low Voltage Level Converter for up to V_I = 16V**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . –55^oC to 125^oC**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30%of V_{CC} at V_{CC} = 5V**

Pinout

CD54HC4049, CD54HC4050
(CERDIP)
CD74HC4049, CD74HC4050
(PDIP, SOIC, SOP, TSSOP)
TOP VIEW



Description

The ’HC4049 and ’HC4050 are fabricated with high-speed silicon gate technology. They have a modified input protection structure that enables these parts to be usedas logic level translators which convert high-level logic to a low-level logic while operating off the low-level logic supply. For example, 15-V input pulse levels can be down-converted to 0-V to 5-V logic levels. The modified input protection structure protects the input from negative electrostatic discharge. These parts also can be used as simple buffers or inverters without level translation. The ’HC4049 and ’HC4050 are enhanced versions of equivalent CMOS types.

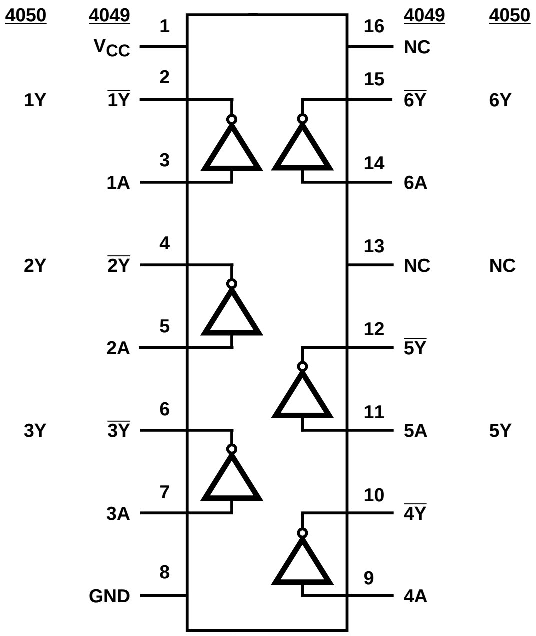
Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE
CD54HC4049F3A	–55 to 125	16 Ld CERDIP
CD54HC4050F3A	–55 to 125	16 Ld CERDIP
CD74HC4049E	–55 to 125	16 Ld PDIP
CD74HC4049M	–55 to 125	16 Ld SOIC
CD74HCT4050MT	–55 to 125	16 Ld SOIC
CD74HC4049M96	–55 to 125	16 Ld SOIC
CD74HC4049NSR	–55 to 125	16 Ld SOP
CD74HC4049PW	–55 to 125	16 Ld TSSOP
CD74HC4049PWR	–55 to 125	16 Ld TSSOP
CD74HC4049PWT	–55 to 125	16 Ld TSSOP
CD74HC4050E	–55 to 125	16 Ld PDIP
CD74HC4050M	–55 to 125	16 Ld SOIC
CD74HC4050MT	–55 to 125	16 Ld SOIC
CD74HC4050M96	–55 to 125	16 Ld SOIC
CD74HC4050NSR	–55 to 125	16 Ld SOP
CD74HC4050PW	–55 to 125	16 Ld TSSOP
CD74HC4050PWR	–55 to 125	16 Ld TSSOP
CD74HC4050PWT	–55 to 125	16 Ld TSSOP

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

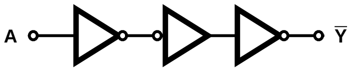
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Functional Diagram

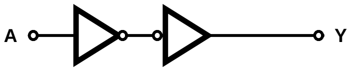


Logic Diagrams

HC4049



HC4050



Absolute Maximum Ratings

DC Supply Voltage, V_{CC}	–0.5V to 7V
Input Voltage Range	–0.5V to 16V
DC Input Diode Current, I_{IK}	
For $V_I < –0.5V$	–20mA
DC Output Diode Current, I_{OK}	
For $V_O < –0.5V$ or $V_O > V_{CC} + 0.5V$	±20mA
DC Output Source or Sink Current per Output Pin, I_O	
For $V_O > –0.5V$ or $V_O < V_{CC} + 0.5V$	±25mA
DC V_{CC} or Ground Current, I_{CC} or I_{GND}	±50mA

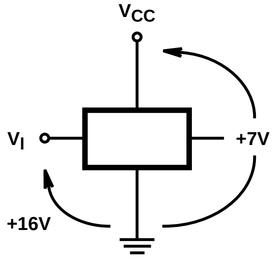
Operating Conditions

Temperature Range (T_A)	–55^{o}C to 125^{o}C
Supply Voltage Range, V_{CC}	
HC Types	2V to 6V
HCT Types	4.5V to 5.5V
DC Input Voltage, V_I	0V to 15V
DC Output Voltage, V_O	0V to V_{CC}
Input Rise and Fall Time	
2V	1000ns (Max)
4.5V	500ns (Max)
6V	400ns (Max)

Thermal Information

Package Thermal Impedance, θ_{JA} (see Note 1):	
E (PDIP) Package	67^{o}C/W
M (SOIC) Package	73^{o}C/W
NS (SOP) Package	64^{o}C/W
PW (TSSOP) Package	108^{o}C/W
Maximum Junction Temperature (Hermetic Package or Die)	175^{o}C
Maximum Junction Temperature (Plastic Package)	150^{o}C
Maximum Storage Temperature Range	–65^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s)	300^{o}C
(SOIC - Lead Tips Only)	

VOLTAGE RELATIONSHIPS MAXIMUM LIMITS



CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

		TEST CONDITIONS		V_{CC} (V)	25^{o}C			–40^{o}C TO 85^{o}C		–55^{o}C TO 125^{o}C		
PARAMETER	SYMBOL	V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNITS
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	–0.02	2	1.9	-	-	1.9	-	1.9	-	V
			–0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			–0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			–4	4.5	3.98	-	-	3.84	-	3.7	-	V
			–5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
		15	-	6	-	-	±0.5	-	±5	-	±5	

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			–40°C TO 85°C		–55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	2	-	20	-	40	µA

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			–40°C TO 85°C		–55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay, nA to $n\overline{Y}$ HC4049 nA to nY HC4050	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	85	-	105	-	130	ns
			4.5	-	-	17	-	21	-	26	ns
			6	-	-	14	-	18	-	22	ns
		C_L = 15pF	5	-	6	-	-	-	-	-	ns
Transition Times (Figure 1)	t_{TLH}, t_{THL}	C_L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C_I	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 2, 3)	C_{PD}	-	5	-	35	-	-	-	-	-	pF

NOTES:

2. C_{PD} is used to determine the dynamic power consumption, per gate.
3. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuit and Waveform

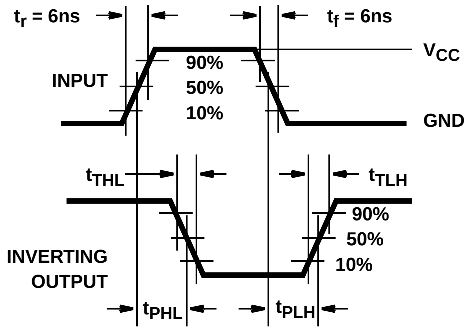


FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8681901EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8681901EA CD54HC4049F3A	Samples
5962-8682001EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8682001EA CD54HC4050F3A	Samples
CD54HC4049F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8681901EA CD54HC4049F3A	Samples
CD54HC4050F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8682001EA CD54HC4050F3A	Samples
CD74HC4049E	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4049E	Samples
CD74HC4049EE4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4049E	Samples
CD74HC4049M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4049M	Samples
CD74HC4049M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4049M	Samples
CD74HC4049M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4049M	Samples
CD74HC4049M96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4049M	Samples
CD74HC4049MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4049M	Samples
CD74HC4049NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4049M	Samples
CD74HC4049NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4049M	Samples
CD74HC4049PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4049	Samples
CD74HC4049PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4049	Samples
CD74HC4050E	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4050E	Samples
CD74HC4050EE4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4050E	Samples

PACKAGE OPTION ADDENDUM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HC4050M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4050M	Samples
CD74HC4050M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4050M	Samples
CD74HC4050ME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4050M	Samples
CD74HC4050MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4050M	Samples
CD74HC4050NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4050M	Samples
CD74HC4050PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4050	Samples
CD74HC4050PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4050	Samples
CD74HC4050PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4050	Samples
CD74HC4050PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4050	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD54HC4049, CD54HC4050, CD74HC4049, CD74HC4050 :

- Catalog: CD74HC4049, CD74HC4050

- Military: CD54HC4049, CD54HC4050

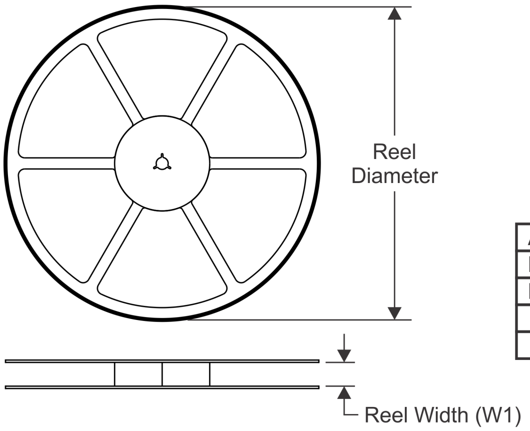
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

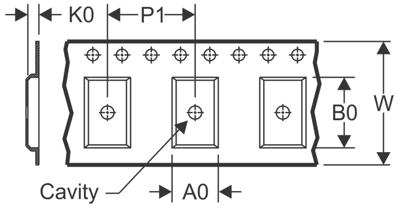
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

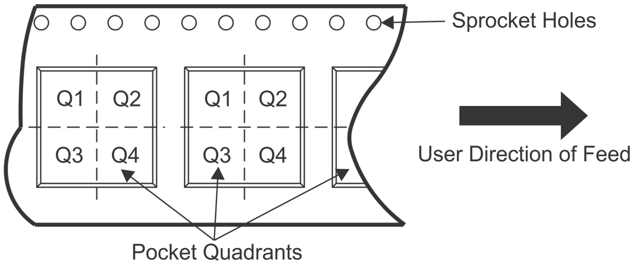


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

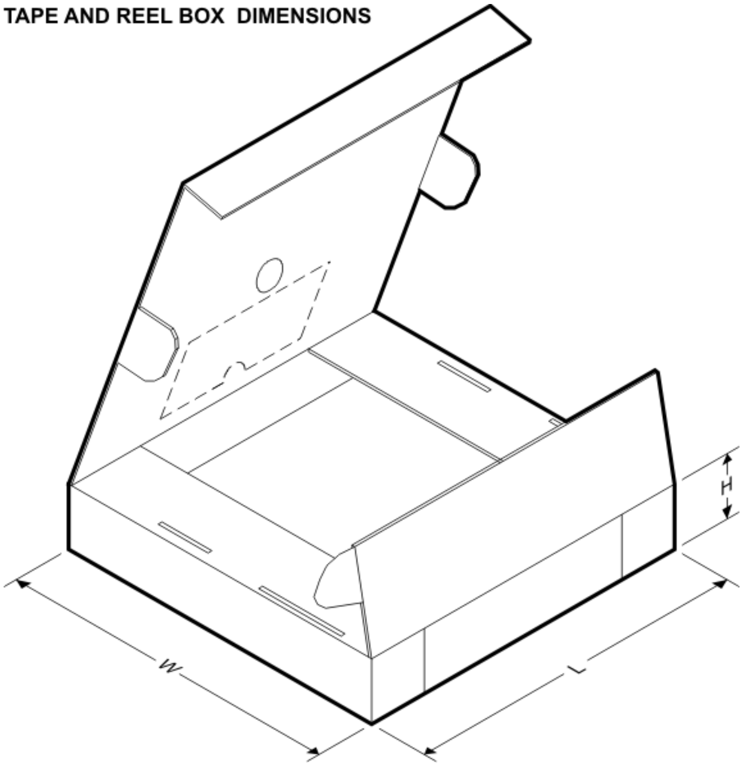
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4049M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4049NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD74HC4049PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4050M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4050NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD74HC4050PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4050PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4049M96	SOIC	D	16	2500	333.2	345.9	28.6
CD74HC4049NSR	SO	NS	16	2000	367.0	367.0	38.0
CD74HC4049PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CD74HC4050M96	SOIC	D	16	2500	333.2	345.9	28.6
CD74HC4050NSR	SO	NS	16	2000	367.0	367.0	38.0
CD74HC4050PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CD74HC4050PWT	TSSOP	PW	16	250	367.0	367.0	35.0

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