

Introduction

The signal integrity characteristics of a Power Delivery Network (PDN) are becoming critical aspects of board level and semiconductor package designs due to higher operating frequencies, larger power demands, and the ever shrinking lower and upper voltage limits around low operating voltages. These power system challenges are coming from mainstream designs with operating frequencies of 300MHz or greater, modest ICs with power demand of 15 watts or more, and operating voltages below 3 volts.

The classic PDN topology is comprised of a series of capacitor stages. Figure 1 is an example of this architecture with multiple capacitor stages.

An ideal capacitor can transfer all its stored energy to a load instantly. A real capacitor has parasitics that prevent instantaneous transfer of a capacitor's stored energy. The true nature of a capacitor can be modeled as an RLC equivalent circuit. For most simulation purposes, it is possible to model the characteristics of a real capacitor with one

capacitor, one resistor, and one inductor. The RLC values in this model are commonly referred to as equivalent series capacitance (ESC), equivalent series resistance (ESR), and equivalent series inductance (ESL).

The ESL of a capacitor determines the speed of energy transfer to a load. The lower the ESL of a capacitor, the faster that energy can be transferred to a load. Historically, there has been a tradeoff between energy storage (capacitance) and inductance (speed of energy delivery). Low ESL devices typically have low capacitance. Likewise, higher capacitance devices typically have higher ESLs. This tradeoff between ESL (speed of energy delivery) and capacitance (energy storage) drives the PDN design topology that places the fastest low ESL capacitors as close to the load as possible. Low Inductance MLCCs are found on semiconductor packages and on boards as close as possible to the load.

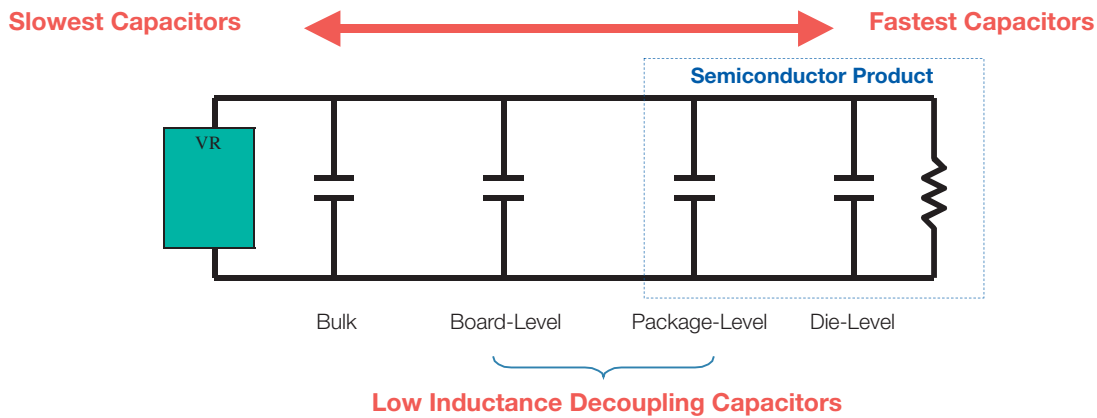


Figure 1 Classic Power Delivery Network (PDN) Architecture

LOW INDUCTANCE CHIP CAPACITORS

The key physical characteristic determining equivalent series inductance (ESL) of a capacitor is the size of the current loop it creates. The smaller the current loop, the lower the ESL. A standard surface mount MLCC is rectangular in shape with electrical terminations on its shorter sides. A Low Inductance Chip Capacitor (LICC) sometimes referred to as Reverse Geometry Capacitor (RGC) has its terminations on the longer side of its rectangular shape.

When the distance between terminations is reduced, the size of the current loop is reduced. Since the size of the current loop is the primary driver of inductance, an 0306 with a smaller current loop has significantly lower ESL than an 0603. The reduction in ESL varies by EIA size, however, ESL is typically reduced 60% or more with an LICC versus a standard MLCC.

INTERDIGITATED CAPACITORS

The size of a current loop has the greatest impact on the ESL characteristics of a surface mount capacitor. There is a secondary method for decreasing the ESL of a capacitor. This secondary method uses adjacent opposing current loops to reduce ESL. The InterDigitated Capacitor (IDC) utilizes both primary and secondary methods of reducing inductance. The IDC architecture shrinks the distance between terminations to minimize the current loop size, then further reduces inductance by creating adjacent opposing current loops.

An IDC is one single capacitor with an internal structure that has been optimized for low ESL. Similar to standard MLCC versus LICCs, the reduction in ESL varies by EIA case size. Typically, for the same EIA size, an IDC delivers an ESL that is at least 80% lower than an MLCC.

Low Inductance Capacitors



Introduction

LAND GRID ARRAY (LGA) CAPACITORS

Land Grid Array (LGA) capacitors are based on the first Low ESL MLCC technology created to specifically address the design needs of current day Power Delivery Networks (PDNs). This is the 3rd low inductance capacitor technology developed by AVX. LGA technology provides engineers with new options. The LGA internal structure and manufacturing technology eliminates the historic need for a device to be physically small to create small current loops to minimize inductance.

The first family of LGA products are 2 terminal devices. A 2 terminal 0306 LGA delivers ESL performance that is equal to or better than an 0306 8 terminal IDC. The 2 terminal 0805 LGA delivers ESL performance that approaches the 0508 8 terminal IDC. New designs that would have used 8 terminal IDCs are moving to 2 terminal LGAs because the layout is easier for a 2 terminal device and manufacturing yield is better for a 2 terminal LGA versus an 8 terminal IDC.

LGA technology is also used in a 4 terminal family of products that AVX is sampling and will formerly introduce in 2008. Beyond 2008, there are new multi-terminal LGA product families that will provide even more attractive options for PDN designers.

LOW INDUCTANCE CHIP ARRAYS (LICA®)

The LICA® product family is the result of a joint development effort between AVX and IBM to develop a high performance MLCC family of decoupling capacitors. LICA was introduced in the 1980s and remains the leading choice of designers in high performance semiconductor packages and high reliability board level decoupling applications.

LICA® products are used in 99.999% uptime semiconductor package applications on both ceramic and organic substrates. The C4 solder ball termination option is the perfect complement to flip-chip packaging technology. Mainframe class CPUs, ultimate performance multi-chip modules, and communications systems that must have the reliability of 5 9's use LICA®.

LICA® products with either Sn/Pb or Pb-free solder balls are used for decoupling in high reliability military and aerospace applications. These LICA® devices are used for decoupling of large pin count FPGAs, ASICs, CPUs, and other high power ICs with low operating voltages.

When high reliability decoupling applications require the very lowest ESL capacitors, LICA® products are the best option.

470 nF 0306 Impedance Comparison

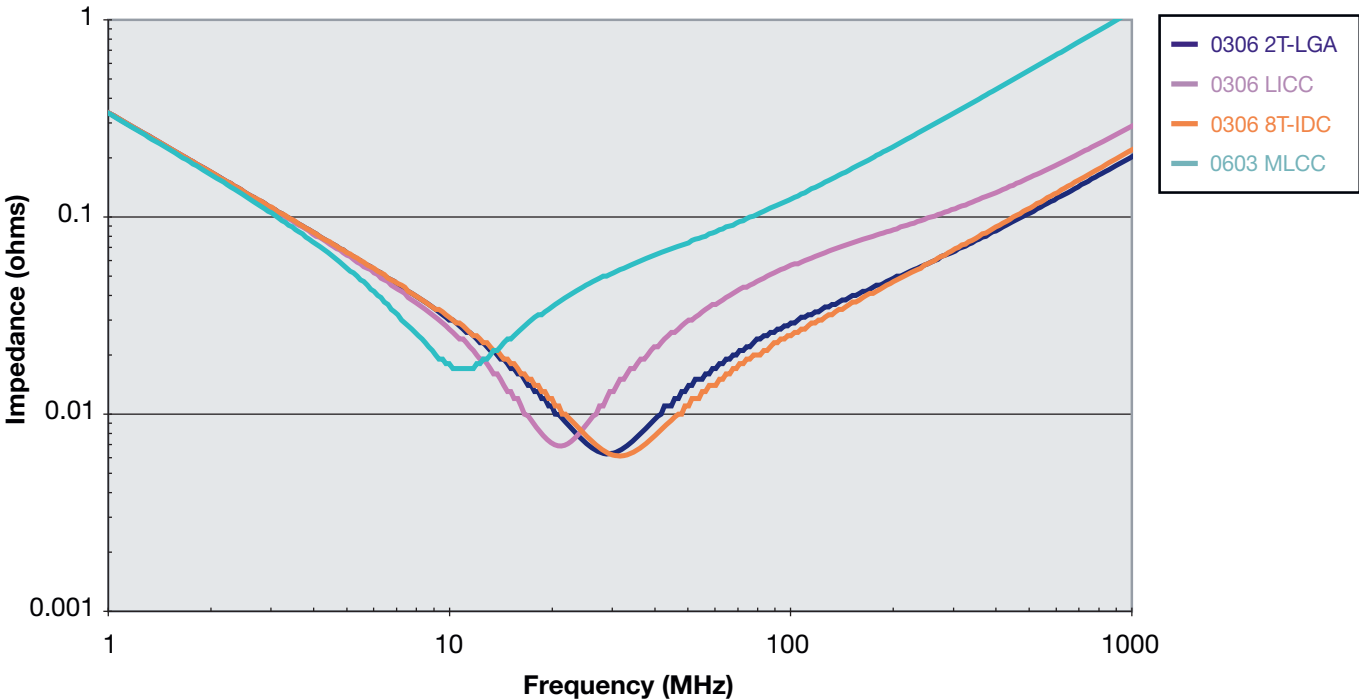
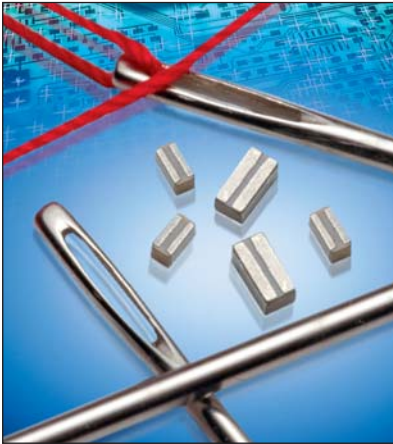


Figure 2 MLCC, LICC, IDC, and LGA technologies deliver different levels of equivalent series inductance (ESL).

LGA Low Inductance Capacitors



0204/0306/0805 Land Grid Arrays



Land Grid Array (LGA) capacitors are the latest family of low inductance MLCCs from AVX. These new LGA products are the third low inductance family developed by AVX. The innovative LGA technology sets a new standard for low inductance MLCC performance. *Electronic Products* awarded its 2006 Product of the Year Award to the LGA Decoupling capacitor.

Our initial 2 terminal versions of LGA technology deliver the performance of an 8 terminal IDC low inductance MLCC with a number of advantages including:

- Simplified layout of 2 large solder pads compared to 8 small pads for IDCs
- Opportunity to reduce PCB or substrate contribution to system ESL by using multiple parallel vias in solder pads
- Advanced FCT manufacturing process used to create uniformly flat terminations on the capacitor that resist "tombstoning"
- Better solder joint reliability

APPLICATIONS

Semiconductor Packages

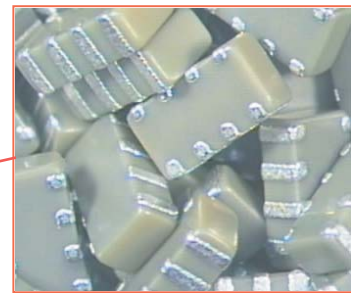
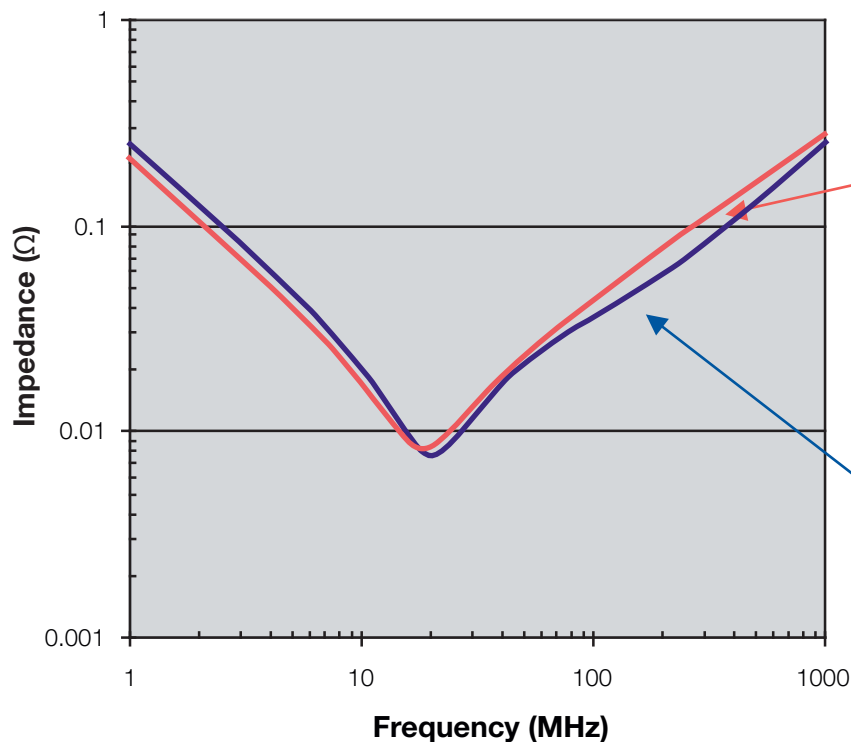
- Microprocessors/CPU's
- Graphics Processors/GPU's
- Chipsets
- FPGA's
- ASIC's

Board Level Device Decoupling

- Frequencies of 300 MHz or more
- IC's drawing 15W or more
- Low voltages
- High speed buses



0306 2 TERMINAL LGA COMPARISON WITH 0306 8 TERMINAL IDC



LGA Low Inductance Capacitors



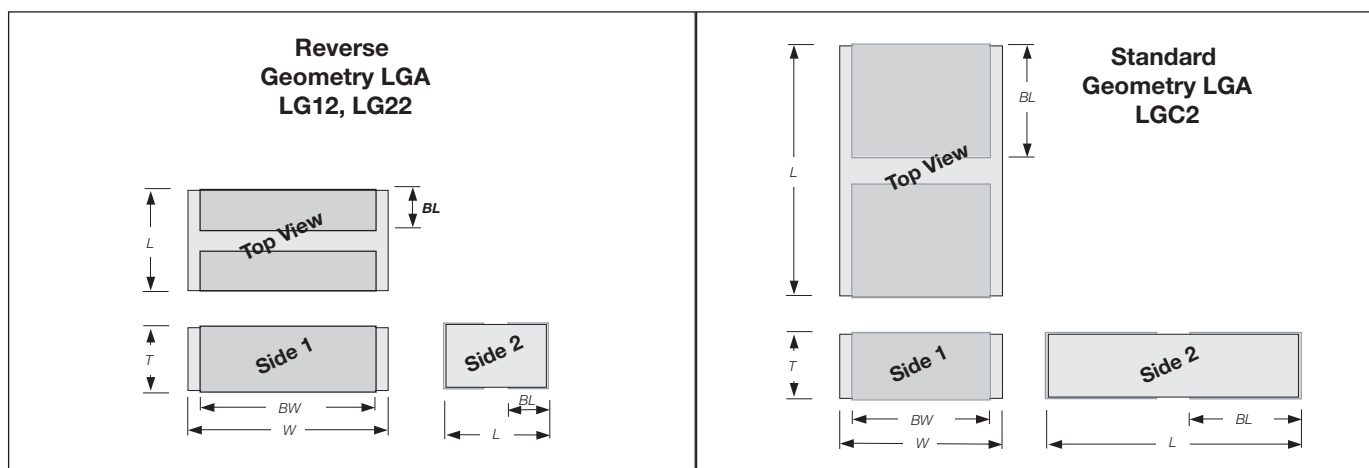
0204/0306/0805 Land Grid Arrays

SIZE	LG12 (0204)						LG22 (0306)						LGC2 (0805)					
Length mm (in.)	0.50 (0.020)						0.76 (0.030)						2.06 (0.081)					
Width mm (in.)	1.00 (0.039)						1.60 (0.063)						1.32 (0.052)					
Temp. Char.	X5R (D)		X7S (Z)		X6S (W)		X7R (C)		X5R (D)		X7S (Z)		X6S (W)		X7R (C)		X5R (D)	
Working Voltage	6.3 (6)	4 (4)	6.3 (6)	4 (4)	6.3 (6)	4 (4)	10 (Z)	6.3 (6)	4 (4)	6.3 (6)	4 (4)	6.3 (6)	4 (4)	6.3 (6)	4 (4)	6.3 (6)	4 (4)	6.3 (6)
Cap (μF)	0.010 (103)																	
	0.022 (223)																	
	0.047 (473)																	
	0.100 (104)																	
	0.220 (224)																	
	0.330 (334)																	
	0.470 (474)																	
	1.000 (105)																	
	2.200 (225)																	

= X7R
 = X5R
 = X7S
 = X6S

HOW TO ORDER

LG	1	2	6	Z	104	M	A	T	2	S	1
Style	Case Size	Number of Terminals	Working Voltage	Temperature Characteristic	Coded Cap	Cap Tolerance	Termination Style	Termination 100% Sn*	Packaging Tape & Reel	Thickness S = 0.55mm max	Number of Capacitors
	1 = 0204 2 = 0306 C = 0805	2	4 = 4V 6 = 6.3V Z = 10V	C = X7R D = X5R Z = X7S W = X6S		M = 20%	A = "U" Land	*Contact factory for other termination finishes	2 = 7" Reel 4 = 13" Reel		

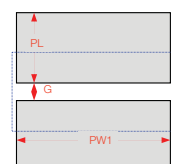


PART DIMENSIONS

Series	L	W	T	BW	BL
LG12 (0204)	0.5 ± 0.05 (0.020 ± 0.002)	1.00 ± 0.10 (0.039 ± 0.004)	0.50 ± 0.05 (0.020 ± 0.002)	0.8 ± 0.10 (0.031 ± 0.004)	0.13 ± 0.08 (0.005 ± 0.003)
LG22 (0306)	0.76 ± 0.10 (0.030 ± 0.004)	1.60 ± 0.10 (0.063 ± 0.004)	0.50 ± 0.05 (0.020 ± 0.002)	1.50 ± 0.10 (0.059 ± 0.004)	0.28 ± 0.08 (0.011 ± 0.003)
LGC2 (0805)	2.06 ± 0.10 (0.081 ± 0.004)	1.32 ± 0.10 (0.052 ± 0.004)	0.50 ± 0.05 (0.020 ± 0.002)	1.14 ± 0.10 (0.045 ± 0.004)	0.90 ± 0.08 (0.035 ± 0.003)

RECOMMENDED SOLDER PAD DIMENSIONS

Series	PL	PW1	G
LG12 (0204)	0.50 (0.020)	1.00 (0.039)	0.20 (0.008)
LG22 (0306)	0.65 (0.026)	1.50 (0.059)	0.20 (0.008)
LGC2 (0805)	1.25 (0.049)	1.40 (0.055)	0.20 (0.008)



Mouser Electronics

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[LG226D474MAT2S1](#)