

Mono class D audio power amplifier with dedicated analog switch

Features

- Wide operating voltage range from $V_{CC} = 2.4 \text{ V}$ to 4.3 V
- Audio amplifier standby mode active low
- Output power: 1.6 W at 4.2 V or 0.75 W at 3.0 V into 4Ω with 1% THD+N maximum
- Output power: 0.95 W at 4.2 V or 0.45 W at 3.0 V into 8Ω with 1% THD+N maximum
- Adjustable gain via external resistors
- Low current consumption 2 mA at 3 V
- Efficiency: 88% typical
- Signal-to-noise ratio: 85 dB typical
- PSRR: 63 dB typical at 217 Hz with 6 dB gain
- PWM base frequency: 250 kHz
- Low pop and click noise
- Dual Power SPST with separated control
- Ultra-high off-isolation on analog switch: -80 dB typical from 20 Hz to 20 kHz

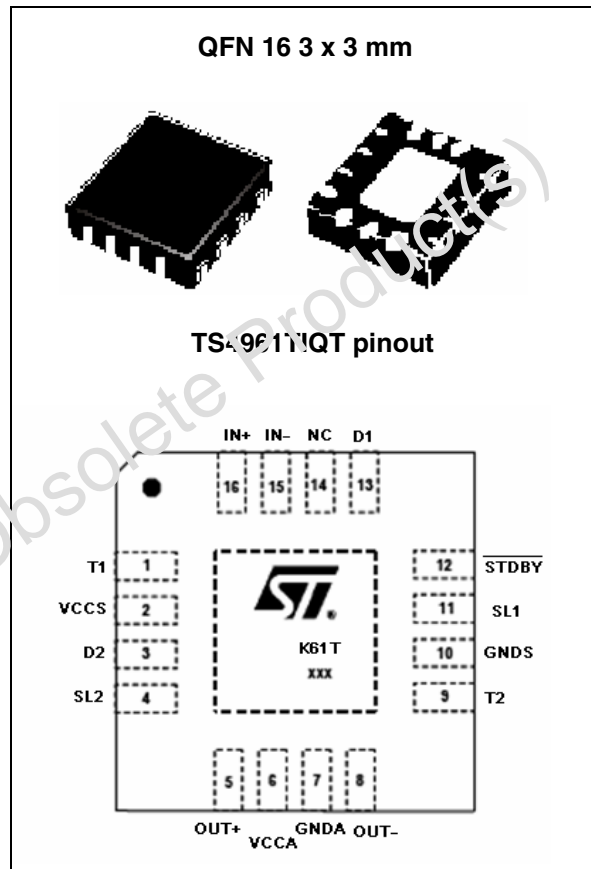
Applications

- Cellular telephones
- PDAs
- Notebook PCs

Description

The TS4961T is a smart combination of one mono class D audio power amplifier and a high-speed CMOS low-voltage dual power analog SPST.

One of the key functions of this device is the switch mode of the various audio signals coming from the codec or baseband through the loudspeaker. It can drive up to 1.6 W into a 4Ω load and 0.95 W into an 8Ω load. It achieves an outstanding efficiency of up to 88% typical.



The audio amplifying gain of the device can be controlled via two external gain-setting resistors. It is designed to operate from 2.4 to 4.3 V, making this device ideal for portable applications.

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1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CCA} & V_{CCS}	Supply voltage ⁽¹⁾ ⁽²⁾	GND to 5.5	V
V_{in}	Input voltage	GND-0.3V / $V_{CC}+0.3V$	V
T_{oper}	Operating free-air temperature range	-40 to + 85	°C
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction to ambient ⁽³⁾	39	°C/W
R_{thjc}	Thermal resistance junction to case	5	°C/W
P_d	Power dissipation	Internally limited ⁽⁴⁾	
ESD	Human body model ⁽⁵⁾	2	kV
	Machine model ⁽⁶⁾	200	V
Latch-up	Latch-up immunity of the Class D Amplifier (All Pins)	200	mA
	Latch-up immunity of the Analog Switch (Supply Pins)	100	
	Latch-up immunity of the Analog Switch Supply (I/O Pins)	200	
V_{STBY}	Standby pin voltage maximum voltage	GND-0.3V / $V_{CC}+0.3V$	V
	Lead temperature (soldering, 10 sec)	260	°C

1. Caution: this device is not protected in the event of abnormal operating conditions, such as short-circuiting between any one output pin and ground, between any one output pin and V_{CC} , and between individual output pins.
2. All voltage values are measured with respect to the ground pin.
3. When mounted on a 4-layers PCB.
4. Exceeding the power derating curves during a long period provokes abnormal operating conditions.
5. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
6. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.

Table 2. Operating conditions for audio amplifier section

Symbol	Parameter	Value	Unit
V_{CCA}	Supply voltage ⁽¹⁾	2.4 to 4.3	V
V_{IC}	Common mode input voltage range ⁽²⁾	0.5 to $V_{CC}-0.8$	V
V_{STBY}	Standby voltage input: ⁽³⁾ Class D amplifier ON Class D amplifier OFF ⁽⁴⁾	$1.4 \leq V_{STBY} \leq V_{CC}$ $GND \leq V_{STBY} \leq 0.4$	V
R_L	Load resistor	≥ 4	Ω

1. For V_{CC} from 2.4 V to 2.5 V, the operating temperature range is reduced to $0^\circ C \leq T_{amb} \leq 70^\circ C$.
2. For V_{CC} from 2.4 V to 2.5 V, the common mode input range must be set at $V_{CC}/2$.
3. Without any signal on V_{STBY} , the device is in standby.
4. Minimum current consumption is obtained when $V_{STBY} = GND$.

Table 3. Operating conditions for analog switch section

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage		2.4 to 4.3	V
V_{in}	Input voltage		0 to V_{CC}	V
V_{IC}	Control input voltage		0 to 4.3	V
V_O	Output voltage		0 to V_{CC}	V
dt/dv	Input rise and fall time control input	$V_{CC} = 2.5\text{ V}$	0 to 20	ns/V
		$V_{CC} = 3.0\text{ V to }4.3\text{ V}$	0 to 10	

Table 4. Audio amplifier standby mode settings

/STDBY	Functional description
Low	OFF Device is in shut-down mode
High	ON Device is in operating mode

Table 5. Analog switch settings truth table

SLn	Switch N°1	Switch N°2
High	ON D1 is connected to T1	ON D2 is connected to T2
Low	OFF High impedance from D1 to T1	OFF High impedance from D2 to T2

Table 6. Pin description

Name	Pin number	Function
VCCA	6	Class D audio amplifier power supply voltage input pin
VCCS	2	Analog switch power supply voltage input pin
/STDBY	12	Standby input pin (active low) to disable the audio amplifier
T1	1	Independent output audio channel 1
D2	3	Common input audio channel 2
SL2	4	Select input pin for D2 to T2 (active high)
OUT+	5	Positive differential audio output
GNDA	7	Audio amplifier input ground
OUT-	8	Negative differential audio output
T2	9	Independent output audio channel 2
GNDS	10	Analog switch input ground
SL1	11	Select input pin for D1 to T1 (active high)
D1	13	Common input audio channel 1
NC	14	No internal connection
IN-	15	Audio negative differential input
IN+	16	Audio positive differential input
E-Pad	-	Exposed pad (should be connected to GND)

2 Electrical characteristics

2.1 Audio amplifier section

Table 7. Electrical characteristics at $V_{CC} = +4.3\text{ V}$ with $GND = 0\text{ V}$, $V_{icm} = 2.1\text{ V}$ and $T_{amb} = 25^\circ\text{ C}$ (unless otherwise specified)⁽¹⁾

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		2.1	3	mA
I_{STBY}	Standby current ⁽²⁾ No input signal, $V_{STBY} = GND$		10	1000	µA
V_{oo}	Output offset voltage No input signal, $R_L = 8\Omega$		3	25	mV
P_{out}	Output power, $G=6\text{dB}$ THD = 1% Max, $f = 1\text{kHz}$, $R_L = 4\Omega$ THD = 10% Max, $f = 1\text{kHz}$, $R_L = 4\Omega$ THD = 1% Max, $f = 1\text{kHz}$, $R_L = 8\Omega$ THD = 10% Max, $f = 1\text{kHz}$, $R_L = 8\Omega$		1.5 1.95 0.9 1.1		W
THD + N	Total harmonic distortion + noise $P_{out} = 600\text{ mW}_{RMS}$, $G = 6\text{dB}$, $20\text{Hz} < f < 20\text{kHz}$ $R_L = 8\Omega + 15\mu\text{H}$, $BW < 30\text{kHz}$ $P_{out} = 700\text{mW}_{RMS}$, $G = 6\text{dB}$, $f = 1\text{kHz}$ $R_L = 8\Omega + 15\mu\text{H}$, $BW < 30\text{kHz}$		2 0.35		%
Efficiency	Efficiency $P_{out} = 1.45\text{ W}_{RMS}$, $R_L = 4\Omega + \geq 15\mu\text{H}$ $P_{out} = 0.9\text{ W}_{RMS}$, $R_L = 8\Omega + \geq 15\mu\text{H}$		78 88		%
PSRR	Power supply rejection ratio with inputs grounded ⁽³⁾ $f = 217\text{Hz}$, $R_L = 8\Omega$, $G=6\text{dB}$, $V_{ripple} = 200\text{mV}_{pp}$		63		dB
CMRR	Common mode rejection ratio $f = 217\text{Hz}$, $R_L = 8\Omega$, $G = 6\text{dB}$, $\Delta V_{ic} = 200\text{mV}_{pp}$		57		dB
Gain	Gain value (R_{in} in $k\Omega$)	$\frac{273k\Omega}{R_{in}}$	$\frac{300k\Omega}{R_{in}}$	$\frac{327k\Omega}{R_{in}}$	V/V
R_{STBY}	Internal resistance from standby to GND	273	300	327	$k\Omega$
F_{PWM}	Pulse width modulator base frequency		280		kHz
SNR	Signal to noise ratio (A-weighting) $P_{out} = 0.8\text{W}$, $R_L = 8\Omega$		85		dB
t_{WU}	Wake-up time		5	10	ms
t_{STBY}	Standby time		5	10	ms

Table 7. Electrical characteristics at $V_{CC} = +4.3$ V with $GND = 0$ V, $V_{icm} = 2.1$ V and $T_{amb} = 25^{\circ}$ C (unless otherwise specified)⁽¹⁾ (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_N	Output voltage noise $f = 20\text{Hz to } 20\text{kHz}$, $G = 6\text{dB}$				
	Unweighted $R_L = 4\Omega$		85		
	A-weighted $R_L = 4\Omega$		60		
	Unweighted $R_L = 8\Omega$		86		
	A-weighted $R_L = 8\Omega$		62		
	Unweighted $R_L = 4\Omega + 15\mu\text{H}$		83		
	A-weighted $R_L = 4\Omega + 15\mu\text{H}$		60		
	Unweighted $R_L = 4\Omega + 30\mu\text{H}$		88		
	A-weighted $R_L = 4\Omega + 30\mu\text{H}$		64		
	Unweighted $R_L = 8\Omega + 30\mu\text{H}$		78		
	A-weighted $R_L = 8\Omega + 30\mu\text{H}$		57		
	Unweighted $R_L = 4\Omega + \text{Filter}$		37		
	A-weighted $R_L = 4\Omega + \text{Filter}$		65		
	Unweighted $R_L = 4\Omega + \text{Filter}$		82		
	A-weighted $R_L = 4\Omega + \text{Filter}$		59		

1. All electrical values are guaranteed with correlation measurements at 2.5 V and 5 V.
2. Standby mode is active when V_{STBY} is tied to GND .
3. Dynamic measurements - $20 \cdot \log(\text{rms}(V_{out}) / \text{rms}(V_{ripple}))$. V_{ripple} is the superimposed sinusoidal signal to V_{CC} at $f = 217$ Hz.

Table 8. Electrical characteristics at $V_{CC} = +3.6\text{ V}$ with $GND = 0\text{ V}$, $V_{icm} = 1.8\text{ V}$, $T_{amb} = 25^\circ\text{ C}$ (unless otherwise specified)⁽¹⁾

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		2	2.8	mA
I_{STBY}	Standby current ⁽²⁾ No input signal, $V_{STBY} = GND$		10	1000	nA
V_{oo}	Output offset voltage No input signal, $R_L = 8\Omega$		3	25	mV
P_{out}	Output power, $G=6\text{dB}$ THD = 1% Max, $f = 1\text{kHz}$, $R_L = 4\Omega$ THD = 10% Max, $f = 1\text{kHz}$, $R_L = 4\Omega$ THD = 1% Max, $f = 1\text{kHz}$, $R_L = 8\Omega$ THD = 10% Max, $f = 1\text{kHz}$, $R_L = 8\Omega$		1.1 1.4 0.7 0.65		W
THD + N	Total harmonic distortion + noise $P_{out} = 450\text{ mW}_{RMS}$, $G = 6\text{dB}$, $20\text{Hz} < f < 20\text{kHz}$ $R_L = 8\Omega + 15\mu\text{H}$, $BW < 30\text{kHz}$ $P_{out} = 500\text{mW}_{RMS}$, $G = 6\text{dB}$, $f = 1\text{kHz}$ $R_L = 8\Omega + 15\mu\text{H}$, $BW < 30\text{kHz}$		2 0.1		%
Efficiency	Efficiency $P_{out} = 1\text{ W}_{RMS}$, $R_L = 4\Omega + \geq 15\mu\text{H}$ $P_{out} = 0.65\text{ W}_{RMS}$, $R_L = 8\Omega + \geq 15\mu\text{H}$		78 88		%
PSRR	Power supply rejection ratio with inputs grounded ⁽³⁾ $f = 217\text{Hz}$, $R_L = 8\Omega$, $G=6\text{dB}$, $V_{ripple} = 200\text{mV}_{pp}$		62		dB
CMRR	Common mode rejection ratio $f = 217\text{Hz}$, $R_L = 8\Omega$, $G = 6\text{dB}$, $\Delta V_{ic} = 200\text{mV}_{pp}$		56		dB
Gain	Gain value (R_{in} in $k\Omega$)	$\frac{273k\Omega}{R_{in}}$	$\frac{300k\Omega}{R_{in}}$	$\frac{327k\Omega}{R_{in}}$	V/V
R_{STBY}	Internal resistance from standby to GND	273	300	327	$k\Omega$
F_{PWM}	Pulse width modulator base frequency		280		kHz
SNR	Signal to noise ratio (A-weighting) $P_{out} = 0.6\text{W}$, $R_L = 8\Omega$		83		dB
t_{WU}	Wake-up time		5	10	ms
t_{STBY}	Standby time		5	10	ms

Table 8. Electrical characteristics at $V_{CC} = +3.6\text{ V}$ with $GND = 0\text{ V}$, $V_{icm} = 1.8\text{ V}$, $T_{amb} = 25^\circ\text{ C}$ (unless otherwise specified)⁽¹⁾ (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_N	Output voltage noise $f = 20\text{Hz to } 20\text{kHz}$, $G = 6\text{dB}$				
	Unweighted $R_L = 4\Omega$		83		
	A-weighted $R_L = 4\Omega$		57		
	Unweighted $R_L = 8\Omega$		83		
	A-weighted $R_L = 8\Omega$		61		
	Unweighted $R_L = 4\Omega + 15\mu\text{H}$		81		
	A-weighted $R_L = 4\Omega + 15\mu\text{H}$		58		
	Unweighted $R_L = 4\Omega + 30\mu\text{H}$		87		
	A-weighted $R_L = 4\Omega + 30\mu\text{H}$		62		
	Unweighted $R_L = 8\Omega + 30\mu\text{H}$		77		
	A-weighted $R_L = 8\Omega + 30\mu\text{H}$		56		
	Unweighted $R_L = 4\Omega + \text{Filter}$		85		
	A-weighted $R_L = 4\Omega + \text{Filter}$		63		
	Unweighted $R_L = 4\Omega + \text{Filter}$		80		
	A-weighted $R_L = 4\Omega + \text{Filter}$		57		

1. All electrical values are guaranteed with correlation measurements at 2.5 V and 5 V.
2. Standby mode is activated when V_{STBY} is tied to GND .
3. Dynamic measurements - $20 \cdot \log(\text{rms}(V_{out}) / \text{rms}(V_{ripple}))$. V_{ripple} is the superimposed sinusoidal signal to V_{CC} at $f = 217\text{ Hz}$.

Table 9. Electrical characteristics at $V_{CC} = +3.0$ V with $GND = 0$ V, $V_{icm} = 1.5$ V, $T_{amb} = 25^\circ$ C (unless otherwise specified)⁽¹⁾

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		1.9	2.7	mA
I_{STBY}	Standby current ⁽²⁾ No input signal, $V_{STBY} = GND$		10	1000	nA
V_{oo}	Output offset voltage No input signal, $R_L = 8\Omega$		3	25	mV
P_{out}	Output power, $G=6$ dB THD = 1% Max, $f = 1$ kHz, $R_L = 4\Omega$ THD = 10% Max, $f = 1$ kHz, $R_L = 4\Omega$ THD = 1% Max, $f = 1$ kHz, $R_L = 8\Omega$ THD = 10% Max, $f = 1$ kHz, $R_L = 8\Omega$		0.7 1 0.5 0.3		W
THD + N	Total harmonic distortion + noise $P_{out} = 300$ mW _{RMS} , $G = 6$ dB, 20 Hz < f < 20 kHz $R_L = 8\Omega + 15\mu$ H, $BW < 30$ kHz $P_{out} = 350$ mW _{RMS} , $G = 6$ dB, $f = 1$ kHz $R_L = 8\Omega + 15\mu$ H, $BW < 30$ kHz		2 0.1		%
Efficiency	Efficiency $P_{out} = 0.7$ W _{RMS} , $R_L = 4\Omega + \geq 15\mu$ H $P_{out} = 0.45$ W _{RMS} , $R_L = 8\Omega + \geq 15\mu$ H		78 88		%
PSRR	Power supply rejection ratio with inputs grounded ⁽³⁾ $f = 217$ Hz, $R_L = 8\Omega$, $G = 6$ dB, $V_{ripple} = 200$ mV _{pp}		60		dB
CMRR	Common mode rejection ratio $f = 217$ Hz, $R_L = 8\Omega$, $G = 6$ dB, $\Delta V_{ic} = 200$ mV _{pp}		54		dB
Gain	Gain value (R_{in} in k Ω)	$\frac{273k\Omega}{R_{in}}$	$\frac{300k\Omega}{R_{in}}$	$\frac{327k\Omega}{R_{in}}$	V/V
R_{STBY}	Internal resistance from standby to GND	273	300	327	k Ω
F_{PWM}	Pulse width modulator base frequency		280		kHz
SNR	Signal to noise ratio (A-weighting) $P_{out} = 0.4$ W, $R_L = 8\Omega$		82		dB
t_{WU}	Wake-up time		5	10	ms
t_{STBY}	Standby time		5	10	ms

Table 9. Electrical characteristics at $V_{CC} = +3.0\text{ V}$ with $GND = 0\text{ V}$, $V_{icm} = 1.5\text{ V}$, $T_{amb} = 25^\circ\text{ C}$ (unless otherwise specified)⁽¹⁾ (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_N	Output voltage noise $f = 20\text{Hz to } 20\text{kHz}$, $G = 6\text{dB}$				
	Unweighted $R_L = 4\Omega$		83		
	A-weighted $R_L = 4\Omega$		57		
	Unweighted $R_L = 8\Omega$		83		
	A-weighted $R_L = 8\Omega$		61		
	Unweighted $R_L = 4\Omega + 15\mu\text{H}$		81		
	A-weighted $R_L = 4\Omega + 15\mu\text{H}$		58		
	Unweighted $R_L = 4\Omega + 30\mu\text{H}$		87		
	A-weighted $R_L = 4\Omega + 30\mu\text{H}$		62		
	Unweighted $R_L = 8\Omega + 30\mu\text{H}$		77		
	A-weighted $R_L = 8\Omega + 30\mu\text{H}$		56		
	Unweighted $R_L = 4\Omega + \text{Filter}$		85		
	A-weighted $R_L = 4\Omega + \text{Filter}$		63		
	Unweighted $R_L = 4\Omega + \text{Filter}$		80		
	A-weighted $R_L = 4\Omega + \text{Filter}$		57		

1. All electrical values are guaranteed with correlation measurements at 2.5 V and 5 V.
2. Standby mode is active when V_{STBY} is tied to GND .
3. Dynamic measurements - $20 \cdot \log(\text{rms}(V_{out}) / \text{rms}(V_{ripple}))$. V_{ripple} is the superimposed sinusoidal signal to V_{CC} at $f = 217\text{ Hz}$.

Table 10. Electrical characteristics at $V_{CC} = +2.5\text{ V}$ with $GND = 0\text{ V}$, $V_{icm} = 1.25\text{ V}$, $T_{amb} = 25^\circ\text{ C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		1.7	2.4	mA
I_{STBY}	Standby current ⁽¹⁾ No input signal, $V_{STBY} = GND$		10	1000	nA
V_{oo}	Output offset voltage No input signal, $R_L = 8\Omega$		3	25	mV
P_{out}	Output power, $G=6\text{dB}$ THD = 1% Max, $f = 1\text{kHz}$, $R_L = 4\Omega$ THD = 10% Max, $f = 1\text{kHz}$, $R_L = 4\Omega$ THD = 1% Max, $f = 1\text{kHz}$, $R_L = 8\Omega$ THD = 10% Max, $f = 1\text{kHz}$, $R_L = 8\Omega$		0.5 0.65 0.33 0.41		W
THD + N	Total harmonic distortion + noise $P_{out} = 180\text{ mW}_{RMS}$, $G = 6\text{dB}$, $20\text{Hz} < f < 20\text{kHz}$ $R_L = 8\Omega + 15\mu\text{H}$, $BW < 30\text{kHz}$ $P_{out} = 200\text{mW}_{RMS}$, $G = 6\text{dB}$, $f = 1\text{kHz}$ $R_L = 8\Omega + 15\mu\text{H}$, $BW < 30\text{kHz}$		1 0.05		%
Efficiency	Efficiency $P_{out} = 0.47\text{ W}_{RMS}$, $R_L = 4\Omega + \geq 15\mu\text{H}$ $P_{out} = 0.3\text{ W}_{RMS}$, $R_L = 8\Omega + \geq 15\mu\text{H}$		78 88		%
PSRR	Power supply rejection ratio with inputs grounded ⁽²⁾ $f = 217\text{Hz}$, $R_L = 8\Omega$, $G = 6\text{dB}$, $V_{ripple} = 200\text{mV}_{pp}$		60		dB
CMRR	Common mode rejection ratio $f = 217\text{Hz}$, $R_L = 8\Omega$, $G = 6\text{dB}$, $\Delta V_{ic} = 200\text{mV}_{pp}$		54		dB
Gain	Gain value (R_{in} in $k\Omega$)	$\frac{273k\Omega}{R_{in}}$	$\frac{300k\Omega}{R_{in}}$	$\frac{327k\Omega}{R_{in}}$	V/V
$R_{S\text{-}BY}$	Internal resistance from standby to GND	273	300	327	$k\Omega$
F_{PWM}	Pulse width modulator base frequency		280		kHz
SNR	Signal to noise ratio (A-weighting) $P_{out} = 0.3\text{W}$, $R_L = 8\Omega$		80		dB
t_{WU}	Wake-up time		5	10	ms
t_{STBY}	Standby time		5	10	ms

Table 10. Electrical characteristics at $V_{CC} = +2.5\text{ V}$ with $GND = 0\text{ V}$, $V_{icm} = 1.25\text{ V}$, $T_{amb} = 25^\circ\text{ C}$ (unless otherwise specified) (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_N	Output voltage noise $f = 20\text{Hz to } 20\text{kHz}$, $G = 6\text{dB}$				
	Unweighted $R_L = 4\Omega$		85		
	A-weighted $R_L = 4\Omega$		60		
	Unweighted $R_L = 8\Omega$		86		
	A-weighted $R_L = 8\Omega$		62		
	Unweighted $R_L = 4\Omega + 15\mu\text{H}$		76		
	A-weighted $R_L = 4\Omega + 15\mu\text{H}$		56		
	Unweighted $R_L = 4\Omega + 30\mu\text{H}$		82		
	A-weighted $R_L = 4\Omega + 30\mu\text{H}$		60		
	Unweighted $R_L = 8\Omega + 30\mu\text{H}$		67		
	A-weighted $R_L = 8\Omega + 30\mu\text{H}$		53		
	Unweighted $R_L = 4\Omega + \text{Filter}$		78		
	A-weighted $R_L = 4\Omega + \text{Filter}$		57		
	Unweighted $R_L = 4\Omega + \text{Filter}$		74		
	A-weighted $R_L = 4\Omega + \text{Filter}$		54		

- Standby mode is active when V_{STBY} is tied to GND .
- Dynamic measurements - $20 \cdot \log(\text{rms}(V_{out})/\text{rms}(V_{ripple}))$. V_{ripple} is the superimposed sinusoidal signal to V_{CC} at $f = 217\text{ Hz}$.

Table 11. Electrical characteristics at $V_{CC} = +2.4$ V with $GND = 0$ V, $V_{icm} = 1.2$ V, $T_{amb} = 25^{\circ}$ C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load		1.7		mA
I_{STBY}	Standby current ⁽¹⁾ No input signal, $V_{STBY} = GND$		10		nA
V_{oo}	Output offset voltage No input signal, $R_L = 8\Omega$		3		mV
P_{out}	Output power, $G=6dB$ THD = 1% Max, $f = 1kHz$, $R_L = 4\Omega$ THD = 10% Max, $f = 1kHz$, $R_L = 4\Omega$ THD = 1% Max, $f = 1kHz$, $R_L = 8\Omega$ THD = 10% Max, $f = 1kHz$, $R_L = 8\Omega$		0.42 0.61 0.3 0.33		W
THD + N	Total harmonic distortion + noise $P_{out} = 150$ mW _{RMS} , $G = 6dB$, $20Hz < f < 20kHz$ $R_L = 8\Omega + 15\mu H$, $BW < 30kHz$		1		%
Efficiency	Efficiency $P_{out} = 0.38$ W _{RMS} , $R_L = 4\Omega + \geq 15\mu H$ $P_{out} = 0.25$ W _{RMS} , $R_L = 8\Omega + \geq 15\mu H$		77 86		%
CMRR	Common mode rejection ratio $f = 217Hz$, $R_L = 8\Omega$, $G = 6dB$, $\Delta V_{ic} = 200mV_{pp}$		54		dB
Gain	Gain value (R_{in} in $k\Omega$)	$\frac{273k\Omega}{R_{in}}$	$\frac{300k\Omega}{R_{in}}$	$\frac{327k\Omega}{R_{in}}$	V/V
R_{STBY}	Internal resistance from standby to GND	273	300	327	$k\Omega$
F_{PWM}	Pulse width modulator base frequency		280		kHz
SNR	Signal to noise ratio (A-weighting) $P_{out} = 0.25W$, $R_L = 8\Omega$		80		dB
t_{WU}	Wake-up time		5		ms
t_{STBY}	Standby time		5		ms

Table 11. Electrical characteristics at $V_{CC} = +2.4\text{ V}$ with $GND = 0\text{ V}$, $V_{icm} = 1.2\text{ V}$, $T_{amb} = 25^\circ\text{ C}$ (unless otherwise specified) (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_N	Output voltage noise $f = 20\text{Hz to } 20\text{kHz}$, $G = 6\text{dB}$				
	Unweighted $R_L = 4\Omega$		85		
	A-weighted $R_L = 4\Omega$		60		
	Unweighted $R_L = 8\Omega$		86		
	A-weighted $R_L = 8\Omega$		62		
	Unweighted $R_L = 4\Omega + 15\mu\text{H}$		76		
	A-weighted $R_L = 4\Omega + 15\mu\text{H}$		56		
	Unweighted $R_L = 4\Omega + 30\mu\text{H}$		82		
	A-weighted $R_L = 4\Omega + 30\mu\text{H}$		60		
	Unweighted $R_L = 8\Omega + 30\mu\text{H}$		67		
	A-weighted $R_L = 8\Omega + 30\mu\text{H}$		53		
	Unweighted $R_L = 4\Omega + \text{Filter}$		78		
	A-weighted $R_L = 4\Omega + \text{Filter}$		57		
	Unweighted $R_L = 4\Omega + \text{Filter}$		74		
	A-weighted $R_L = 4\Omega + \text{Filter}$		54		

1. Standby mode is active when V_{STBY} is tied to GND.

2.2 Analog switch section

Table 12. DC specifications

Symbol	Parameter	V _{CC} (V)	Test conditions	Value					Unit
				T _{amb} = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
V _{IH}	High level input voltage	2.5		1.2			1.2		V
		2.7 –3.0		1.3			1.3		
		3.3 –3.6		1.4			1.4		
		4.3		1.5			1.5		
V _{IL}	Low level input voltage	2.5				0.25		0.25	V
		2.7 –3.0				0.25		0.25	
		3.3 –3.6				0.30		0.30	
		4.3				0.40		0.40	
R _{PEAK} , T _n	Switch T _n ON resistance	4.3	V _S = 0 V to V _{CC} I _S = 100 mA		1.10	1.3		1.5	Ω
		3.6			1.15	1.4		1.6	
		3.0			1.25	1.5		1.8	
		2.7			1.35	1.6		1.9	
ΔR _{ON} , T _n	ON resistance match between T _n channels ⁽¹⁾	4.3	V _S at R _{PEAK} I _S = 100 mA		10				mΩ
		3.6			14				
		3.0			14				
		2.7			15				
R _{FLAT} , T _n	ON resistance flatness for T _n channels ⁽²⁾	4.3	V _S = 0 to V _{CC} I _S = 100 mA		0.45	0.50		0.55	Ω
		3.6			0.45	0.50		0.55	
		3.0			0.50	0.55		0.60	
		2.7			0.55	0.60		0.70	
I _{OFF}	OFF state leakage current (T _n), (D _n)	4.3	V _S = 0.3 or 4 V			±0.1		±1	μA
I _{SEL}	SEL leakage current	0 –4.3	V _{SEL} = 0 to 4.3 V			±0.05		±1	μA
I _{CC}	Quiescent supply current	2.4 –4.3	V _{SEL} = V _{CC} or GND			±0.05		±0.2	μA
I _{CCLV}	Quiescent supply current low voltage driving	4.3	V _{SEL} = 1.65 V		±37	±50		±100	μA
			V _{SEL} = 1.80 V		±33	±40		±50	
			V _{SEL} = 2.60 V		±12	±20		±30	

1. $\Delta R_{ON} = R_{ON(max)} - R_{ON(min)}$.

2. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Table 13. AC electrical characteristics ($C_L = 35 \text{ pF}$, $R_L = 50 \text{ } \Omega$, $t_r = t_f \leq 5 \text{ ns}$)

Symbol	Parameter	V _{CC} (V)	Test conditions	Value					Unit
				T _{amb} = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
t _{PLH} , t _{PHL}	Propagation delay	2.5 —2.7			0.45				ns
		3.0 —3.3			0.30				
		3.6 —4.3			0.30				
t _{ON}	Turn-ON time	2.5 —2.7	V _S = 1.5 V		65	85		90	ns
		3.0 —3.3			42	55		65	
		3.6 —4.3			40	55		65	
t _{OFF}	Turn-OFF time	2.5 —2.7	V _S = 1.5 V		18	30		40	ns
		3.0 —3.3			16	30		40	
		3.6 —4.3			15	30		40	
Q	Charge injection	2.5 —2.7	C _L = 100 pF R _L = 1 MΩ V _{GEN} = 0 V R _{GEN} = 0 Ω		51				pC
		3.0 —3.3			51				
		3.6 —4.3			49				

Table 14. Analog switch characteristics ($C_L = 5 \text{ pF}$, $R_L = 50 \Omega$, $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$)

Symbol	Parameter	V _{CC} (V)	Test conditions	Value					Unit
				T _{amb} = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
OIRR _{Tn}	Off isolation for switch T1,T2	2.5 —4.3	V _S =1 V _{rms} , F=1 MHz, R _L = 50 Ω		-80				dB
			V _S =1 V _{rms} , F = 10 MHz, R _L = 50 Ω		-60				
Xtalk _{Tn}	Crosstalk between T1 and T2	2.5 — 4.3	V _S =1 V _{rms} , F = 1 MHz		-85				dB
			V _S =1 V _{rms} , F = 10 MHz		-74				
BW _{Tn}	-3 dB bandwidth for switch T1, T2	2.5 —4.3	R _L = 50 Ω Signal = 0 dBm		58				MHz
C _{SEL}	Control pin input capacitance		V _{CC} = 0 V		9				pF
C _{ON,Tn}	Tn port capacitance when the switch is enabled	3.3	F = 1 MHz		113				pF
C _{OFF,Tn}	Tn port capacitance when the switch is disabled	3.3	F = 1 MHz		85				pF

3 Electrical characteristics curves

3.1 Audio amplifier section

The graphs included in this section use the following abbreviations:

- $R_L + 15\ \mu\text{H}$ or $30\ \mu\text{H}$ = pure resistor + very low series resistance inductor.
- Filter = LC output filter ($1\ \mu\text{F} + 30\ \mu\text{H}$ for $4\ \Omega$ and $0.5\ \mu\text{F} + 60\ \mu\text{H}$ for $8\ \Omega$).
- All measurements done with $C_{S1} = 1\ \mu\text{F}$ and $C_{S2} = 100\ \text{nF}$ except for PSRR where C_{S1} is removed.

Figure 1. Test diagram for audio amplifier measurements

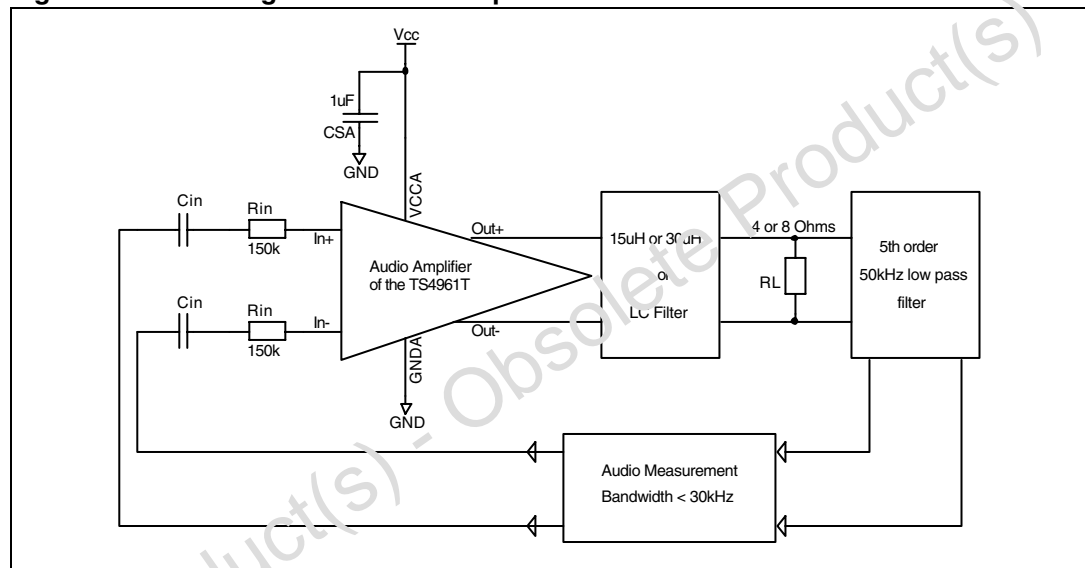


Figure 2. Test diagram for audio amplifier PSRR measurements

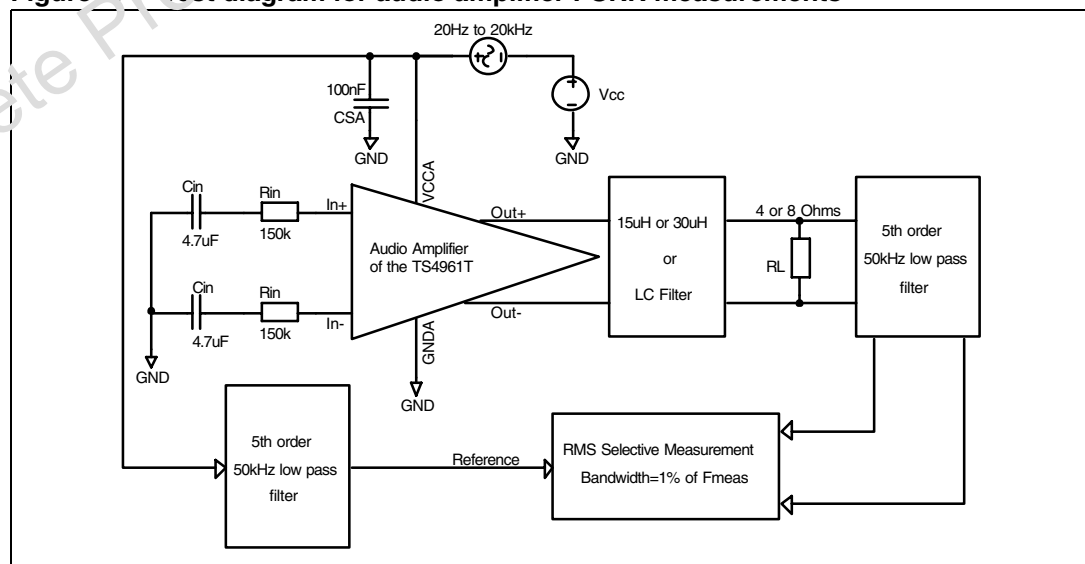


Figure 3. Current consumption vs. power supply voltage

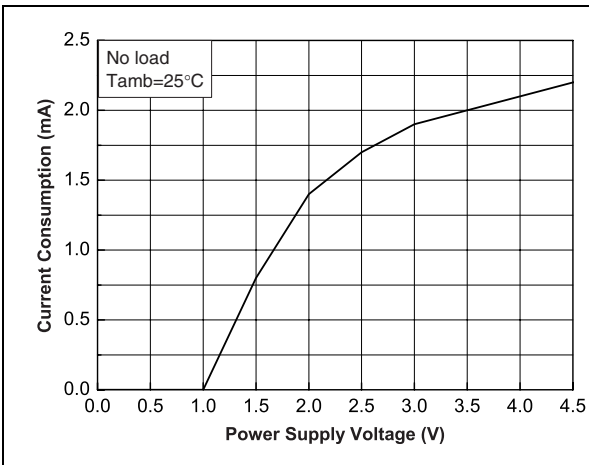


Figure 4. Current consumption vs. standby voltage

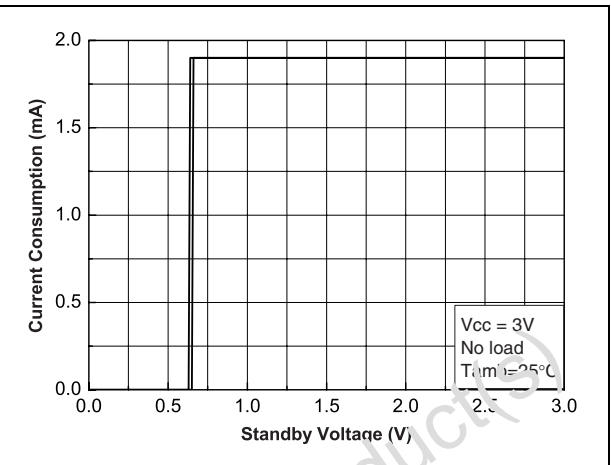


Figure 5. Output offset voltage vs. common mode input voltage

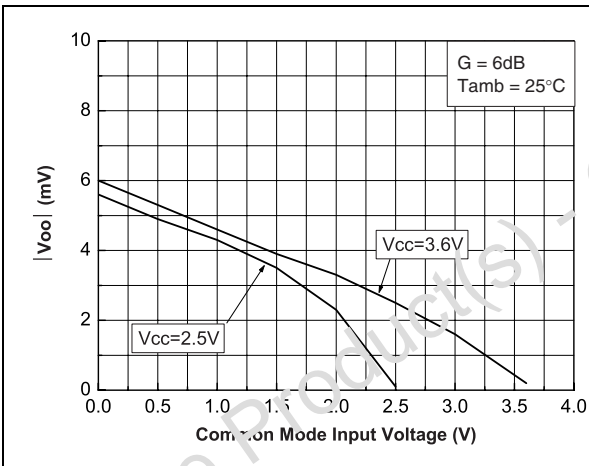


Figure 6. Efficiency vs. output power

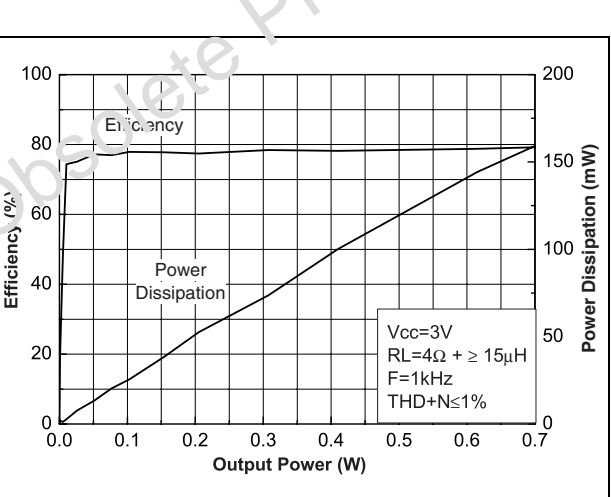


Figure 7. Efficiency vs. output power

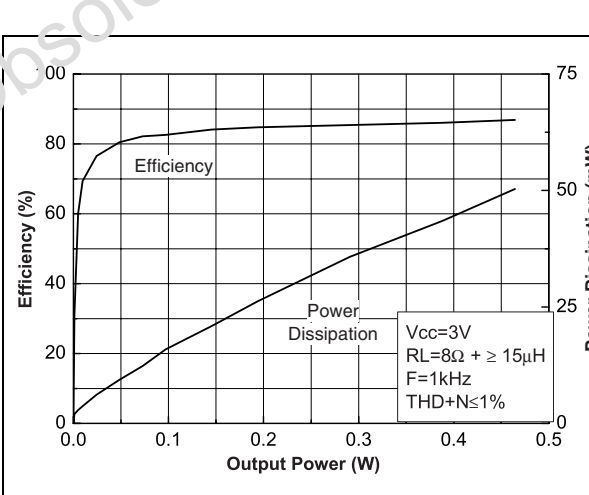


Figure 8. Output power vs. power supply voltage

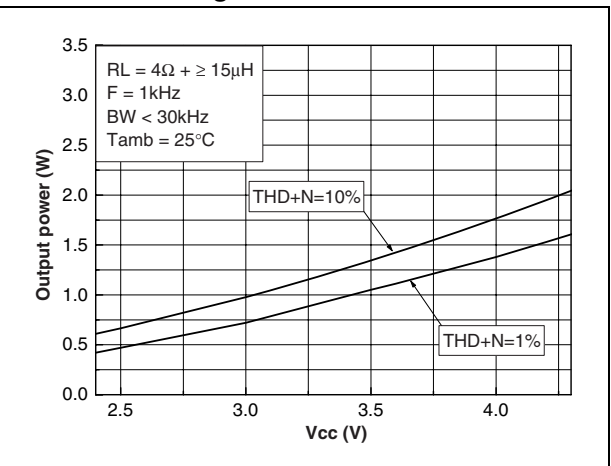


Figure 9. Output power vs. power supply voltage

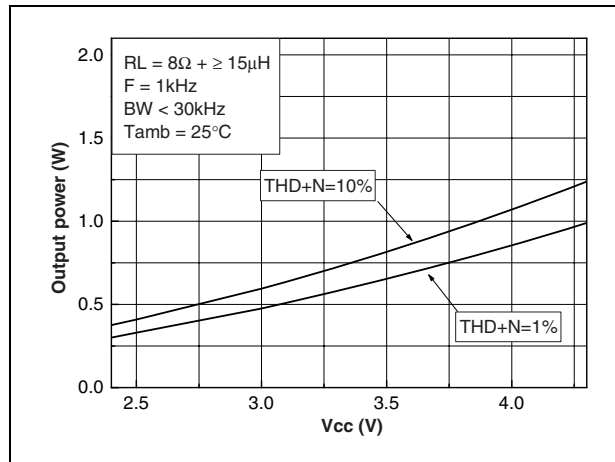


Figure 10. PSSR vs. frequency

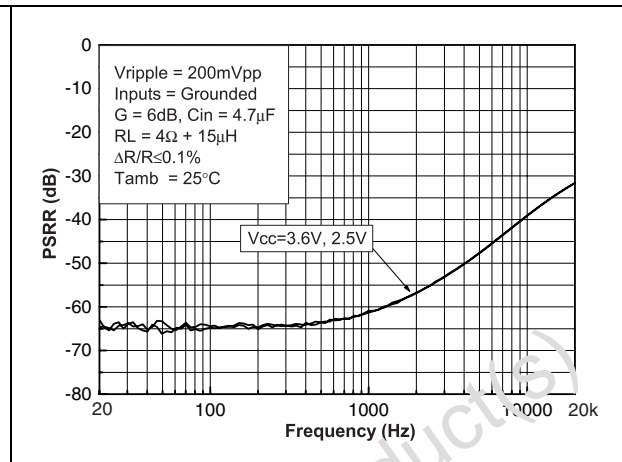


Figure 11. PSSR vs. frequency

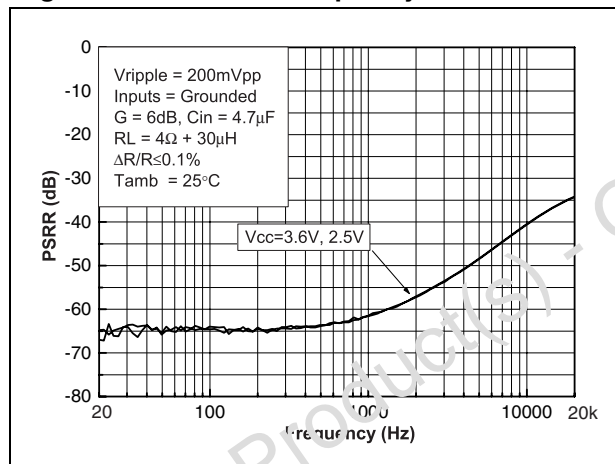


Figure 12. PSSR vs. frequency

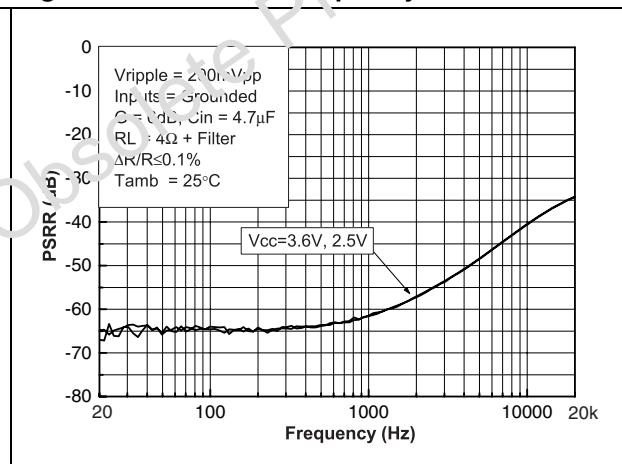


Figure 13. PSSR vs. frequency

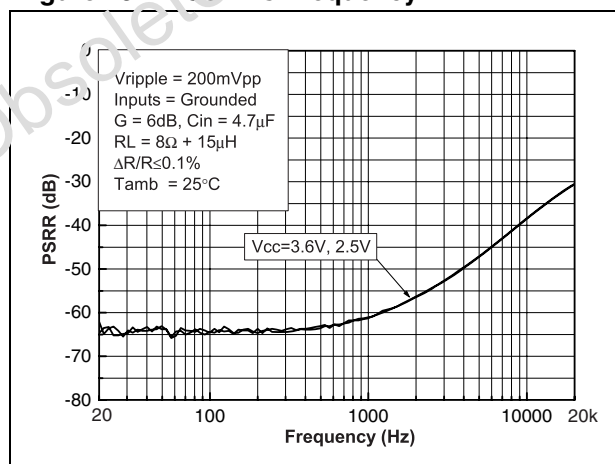


Figure 14. PSSR vs. frequency

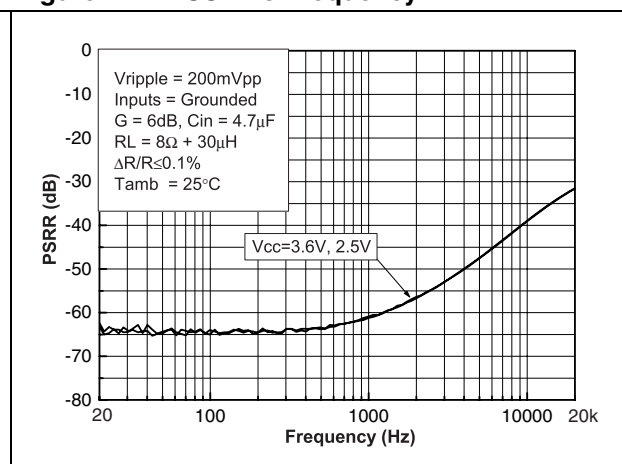


Figure 15. PSSR vs. frequency

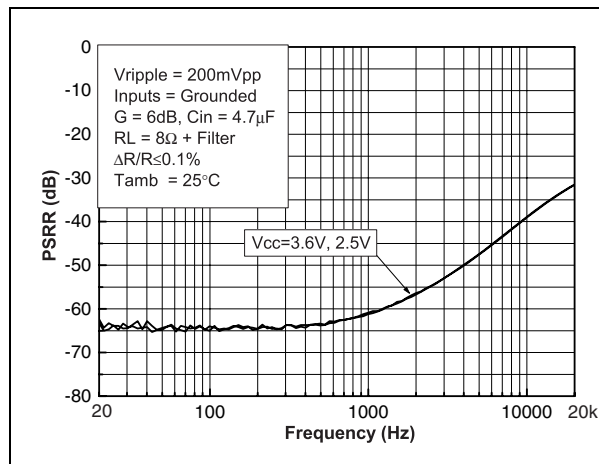


Figure 16. PSSR vs. common mode input voltage

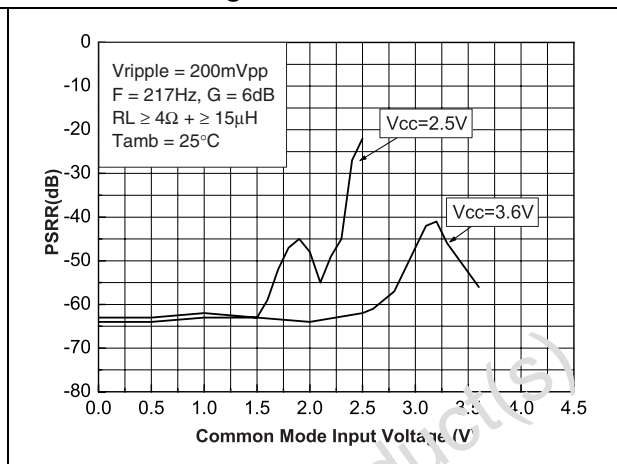


Figure 17. CMRR vs. common mode input voltage

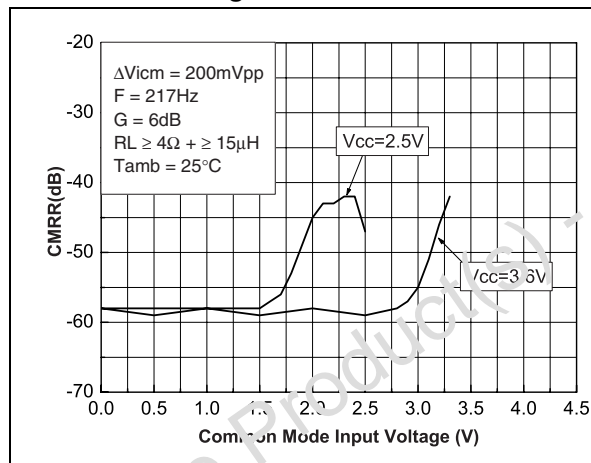


Figure 18. CMRR vs. frequency

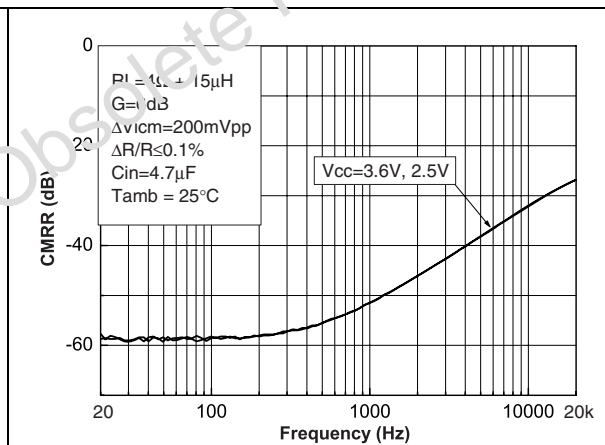


Figure 19. CMRR vs. frequency

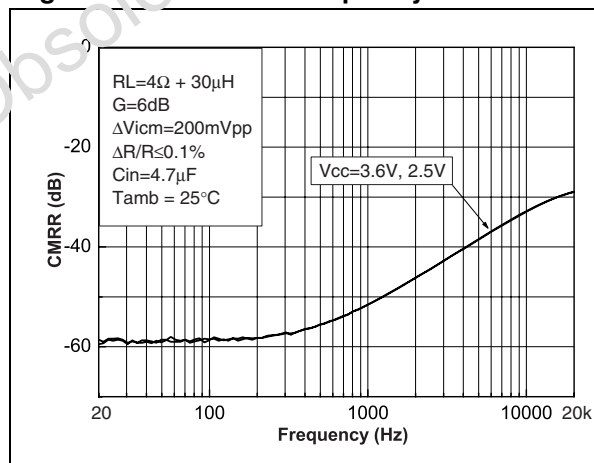


Figure 20. CMRR vs. frequency

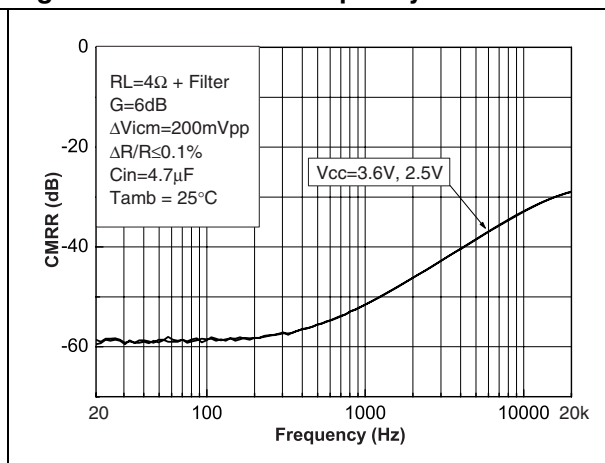


Figure 21. CMRR vs. frequency

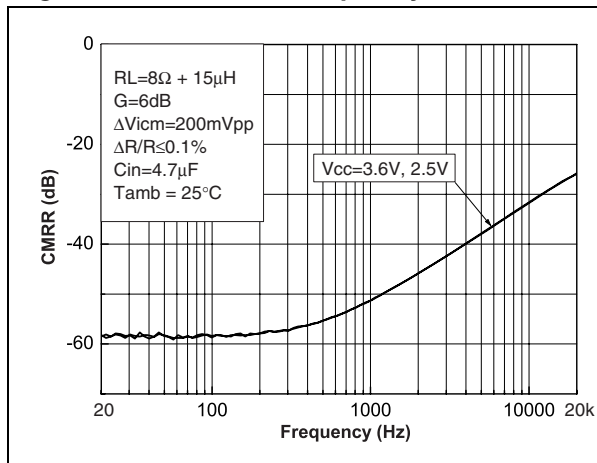


Figure 22. CMRR vs. frequency

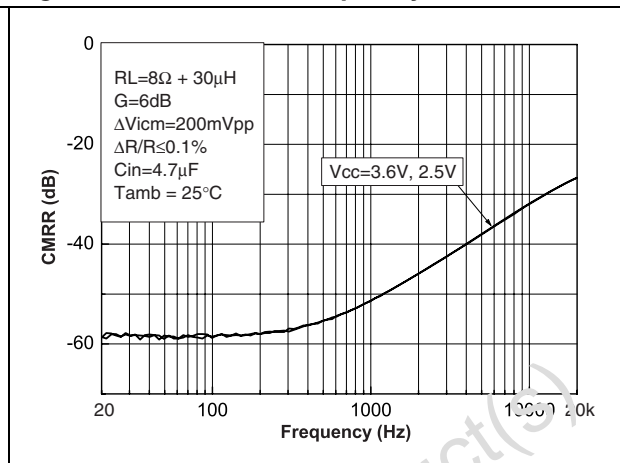


Figure 23. CMRR vs. frequency

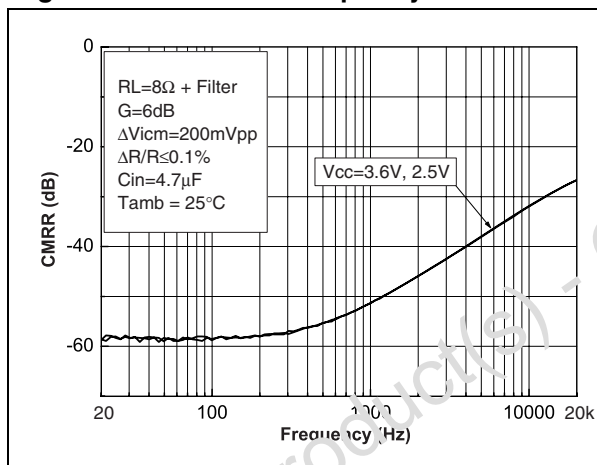


Figure 24. THD+N vs. output power

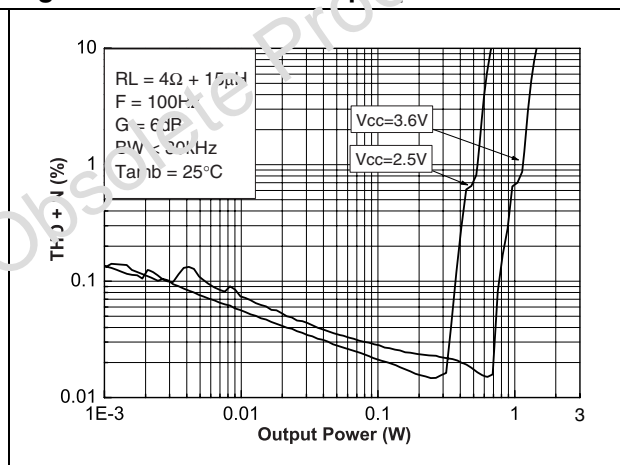


Figure 25. THD+N vs. output power

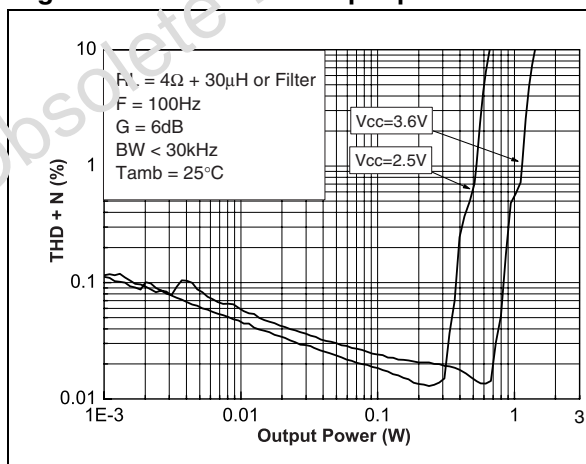


Figure 26. THD+N vs. output power

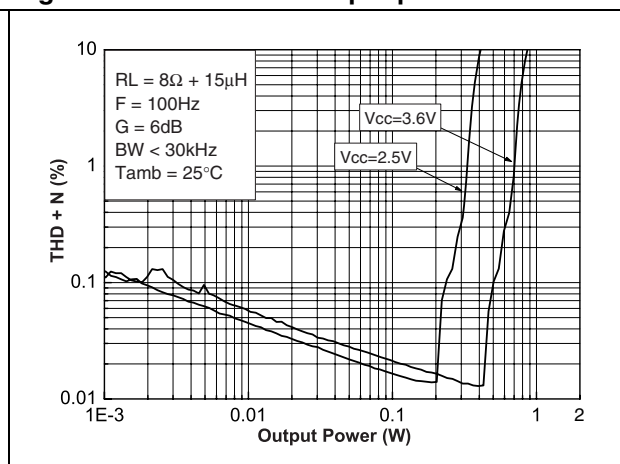


Figure 27. THD+N vs. output power

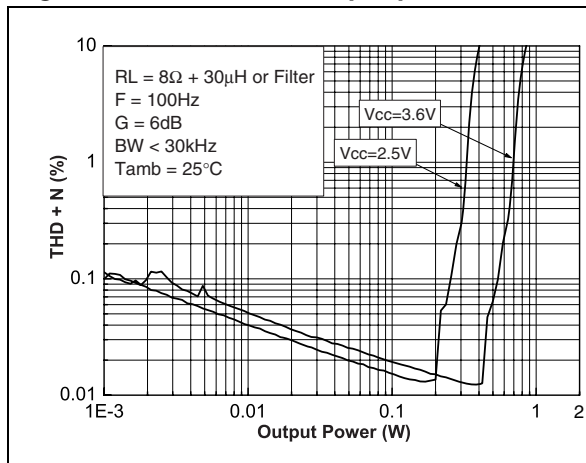


Figure 28. THD+N vs. output power

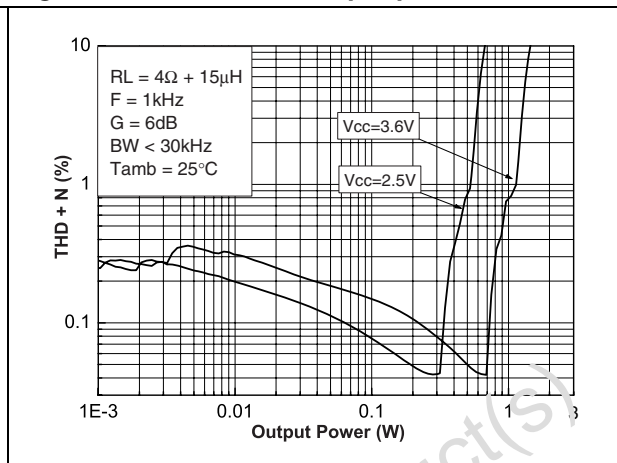


Figure 29. THD+N vs. output power

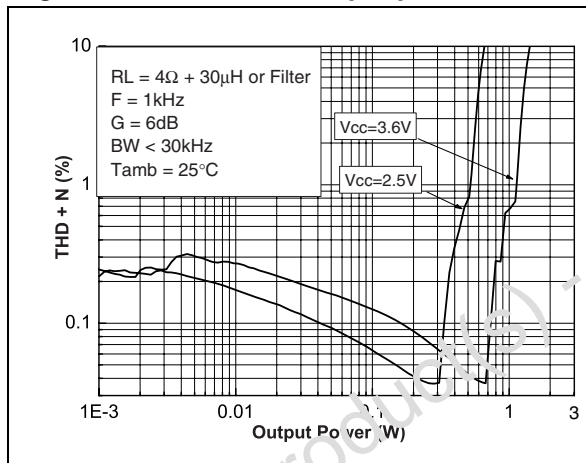


Figure 30. THD+N vs. output power

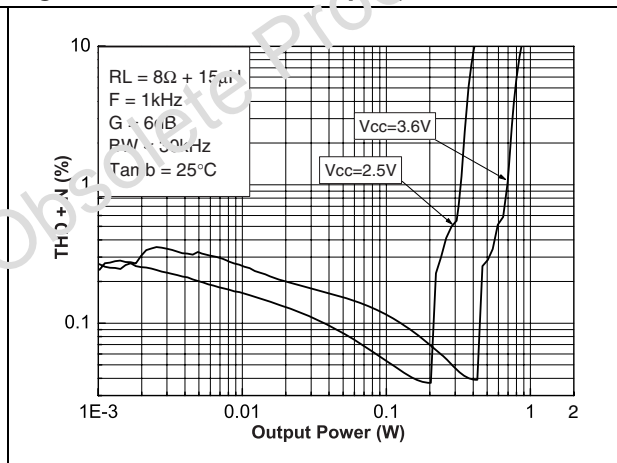


Figure 31. THD+N vs. output power

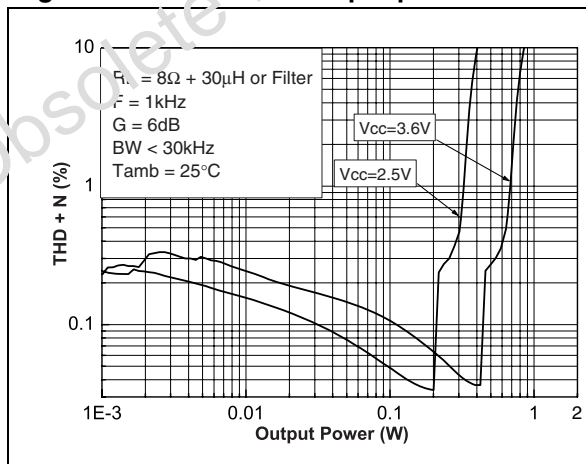


Figure 32. THD+N vs. frequency

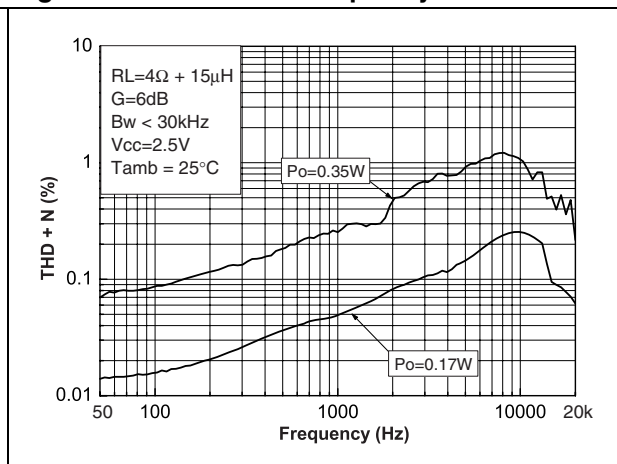


Figure 33. THD+N vs. frequency

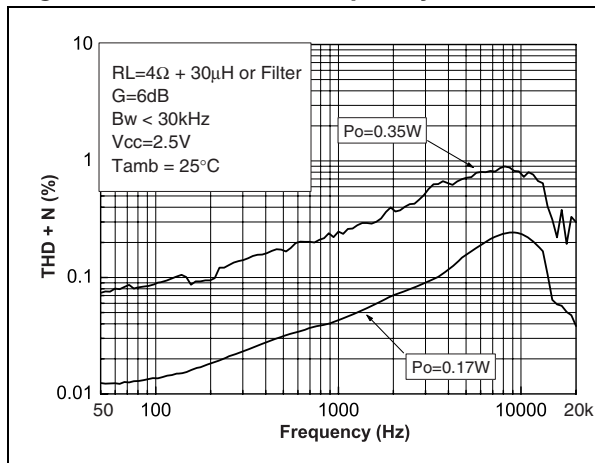


Figure 34. THD+N vs. frequency

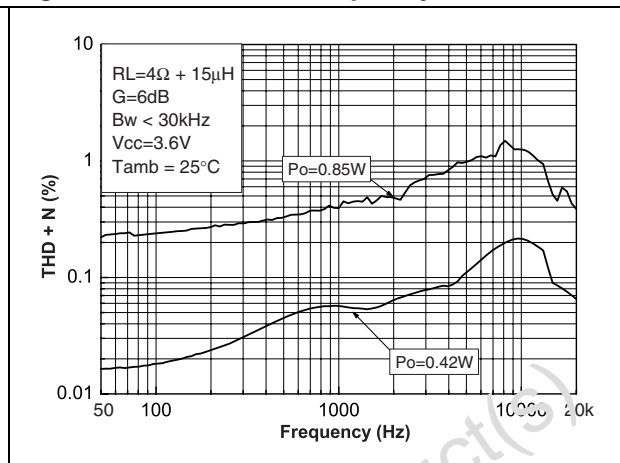


Figure 35. THD+N vs. frequency

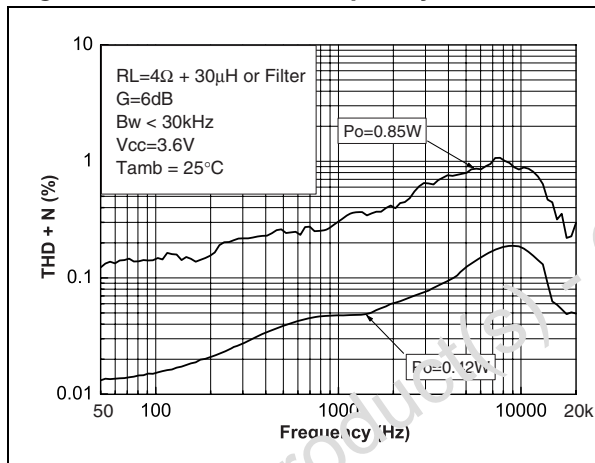


Figure 36. THD+N vs. frequency

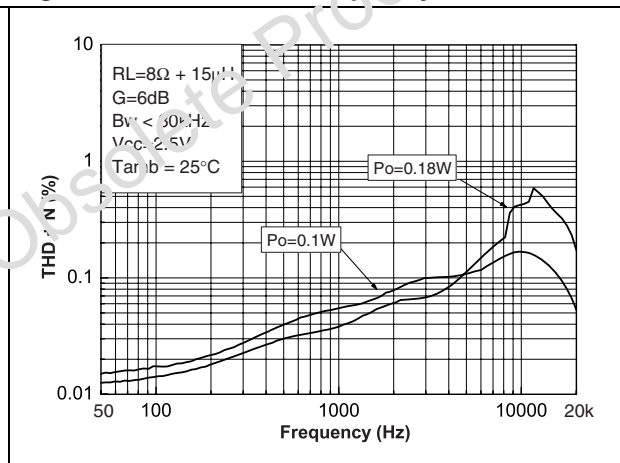


Figure 37. THD+N vs. frequency

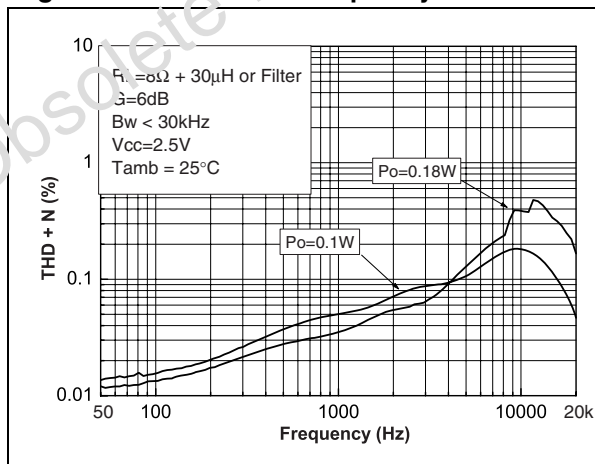


Figure 38. THD+N vs. frequency

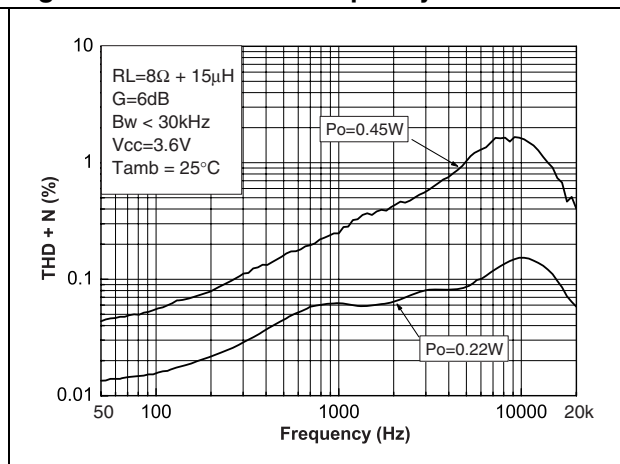


Figure 39. THD+N vs. frequency

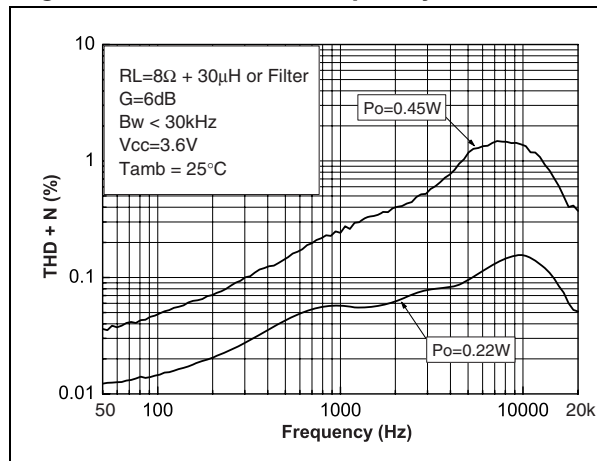


Figure 40. Gain vs. frequency

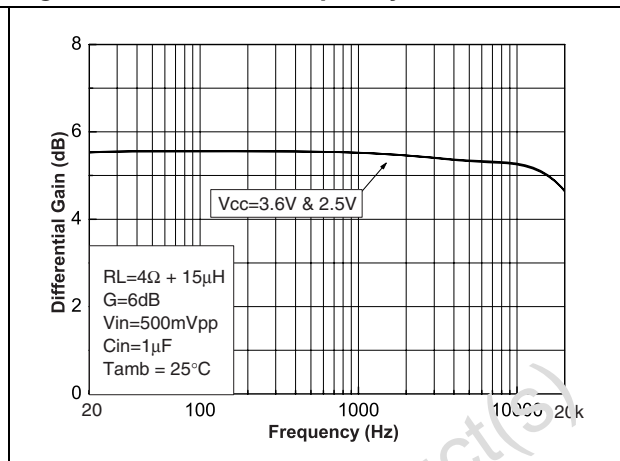


Figure 41. Gain vs. frequency

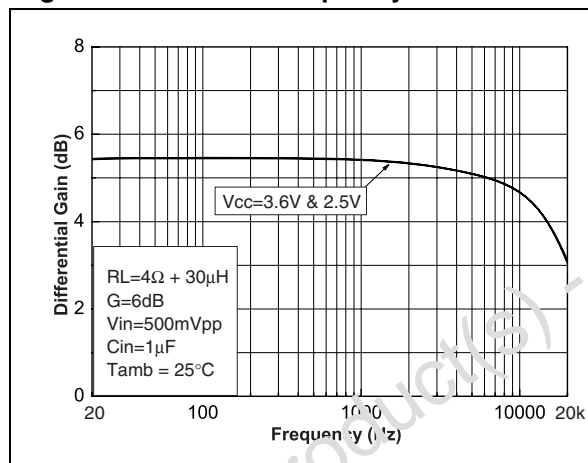


Figure 42. Gain vs. frequency

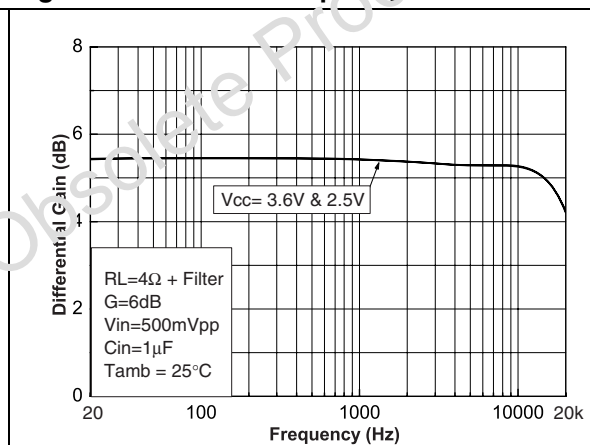


Figure 43. Gain vs. frequency

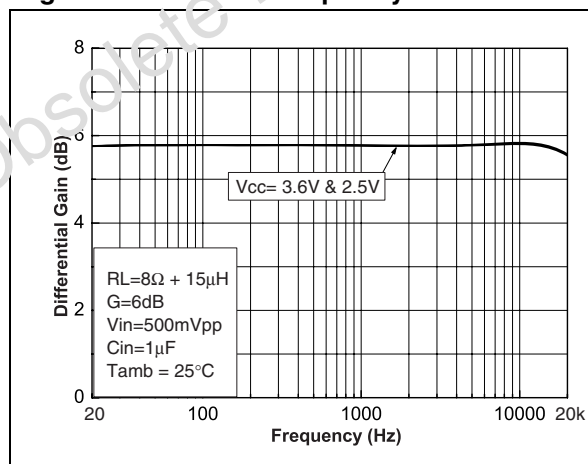


Figure 44. Gain vs. frequency

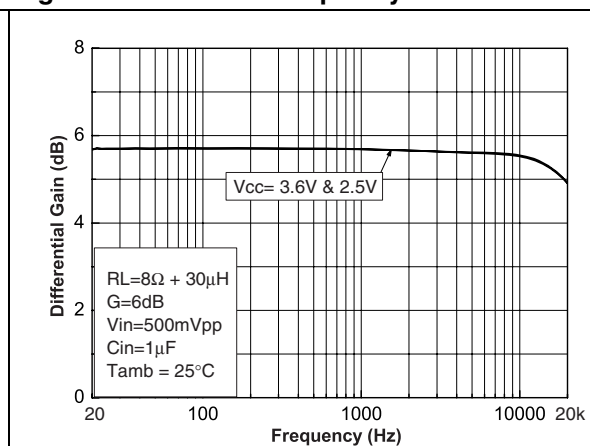


Figure 45. Gain vs. frequency

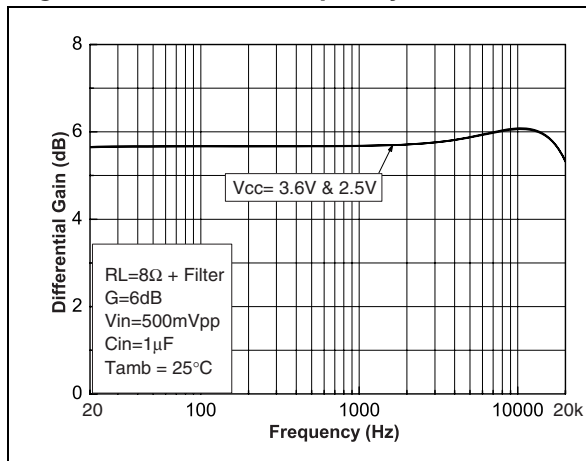


Figure 46. Gain vs. frequency

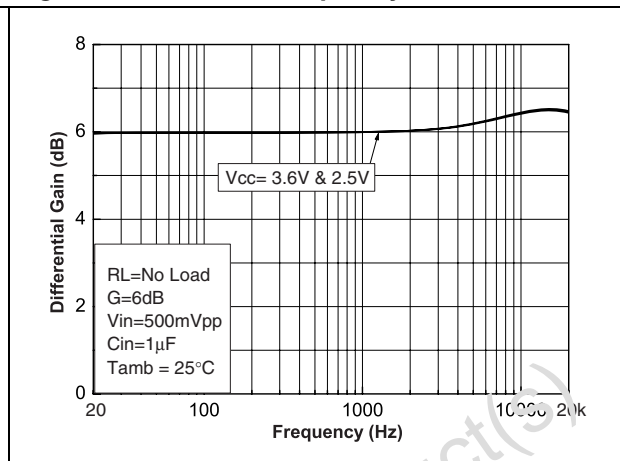


Figure 47. Startup & shutdown time $V_{CC} = 3\text{ V}$, $G = 6\text{ dB}$, $C_{in} = 1\text{ }\mu\text{F}$ (5 ms/div)

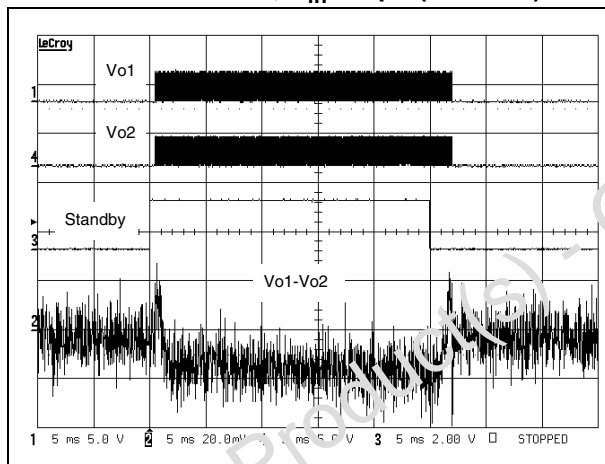


Figure 48. Startup & shutdown time $V_{CC} = 3\text{ V}$, $G = 6\text{ dB}$, $C_{in} = 100\text{ nF}$ (5 ms/div)

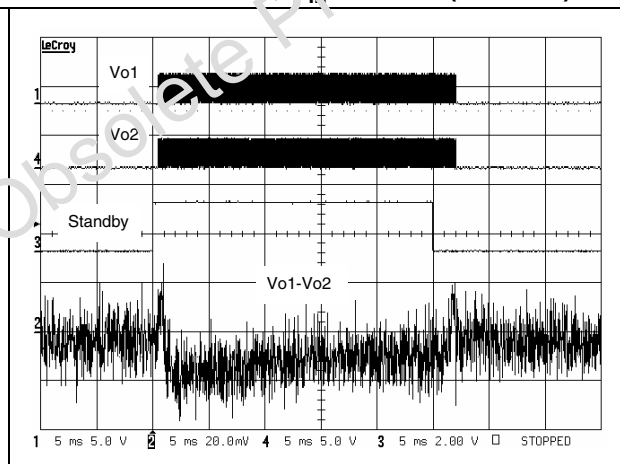
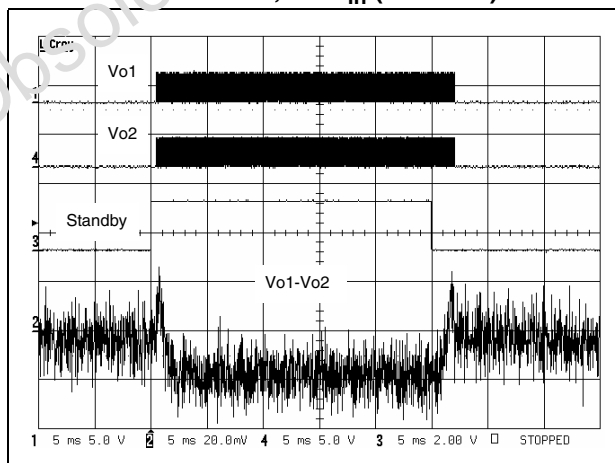


Figure 49. Startup & shutdown time $V_{CC} = 3\text{ V}$, $G = 6\text{ dB}$, no C_{in} (5 ms/div)



3.2 Analog switch section

The graphs included in this section use the following abbreviations.

- $R_L + 15\ \mu\text{H}$ or $30\ \mu\text{H}$ = pure resistor + very low series resistance inductor.
- Filter = LC output filter ($1\ \mu\text{F} + 30\ \mu\text{H}$ for $4\ \Omega$ and $0.5\ \mu\text{F} + 60\ \mu\text{H}$ for $8\ \Omega$).
- All measurements done with $C_{s1} = 1\ \mu\text{F}$ and $C_{s2} = 100\ \text{nF}$ except for PSRR where C_{s1} is removed.

Figure 50. Test diagram for switch measurements

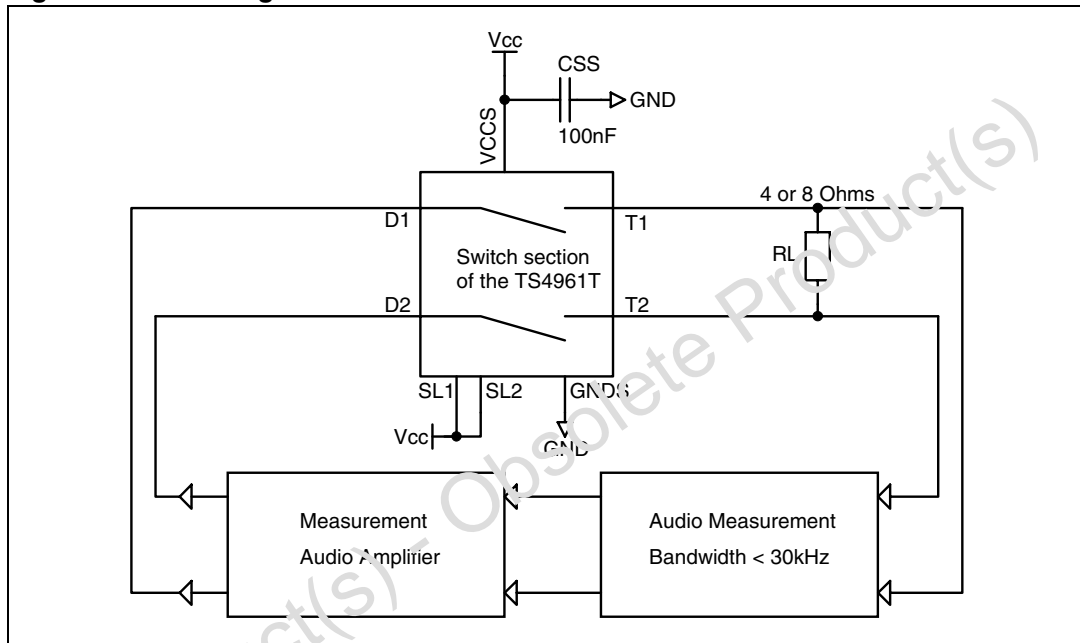


Figure 51. Test diagram for isolation switch measurements

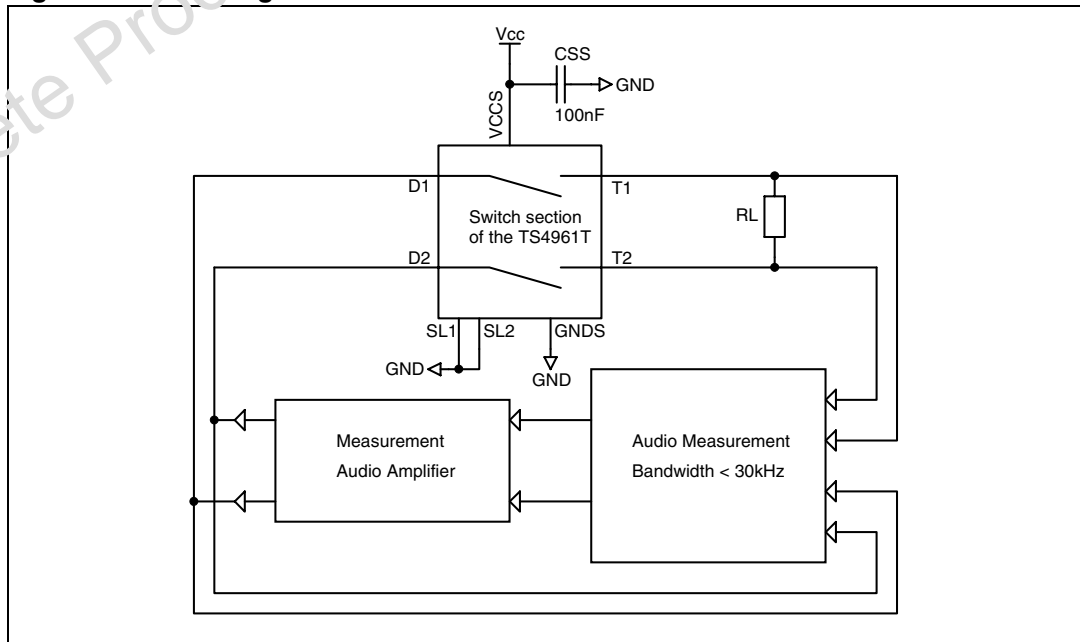


Figure 52. ON resistance

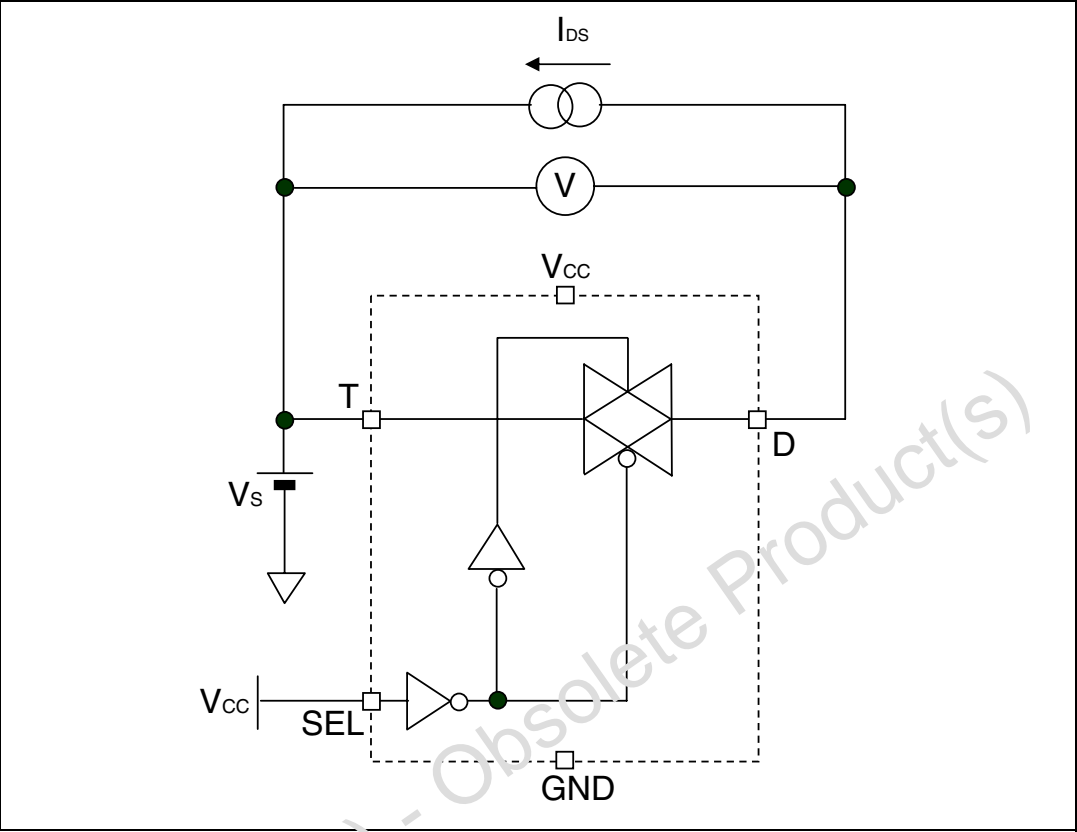


Figure 53. OFF leakage

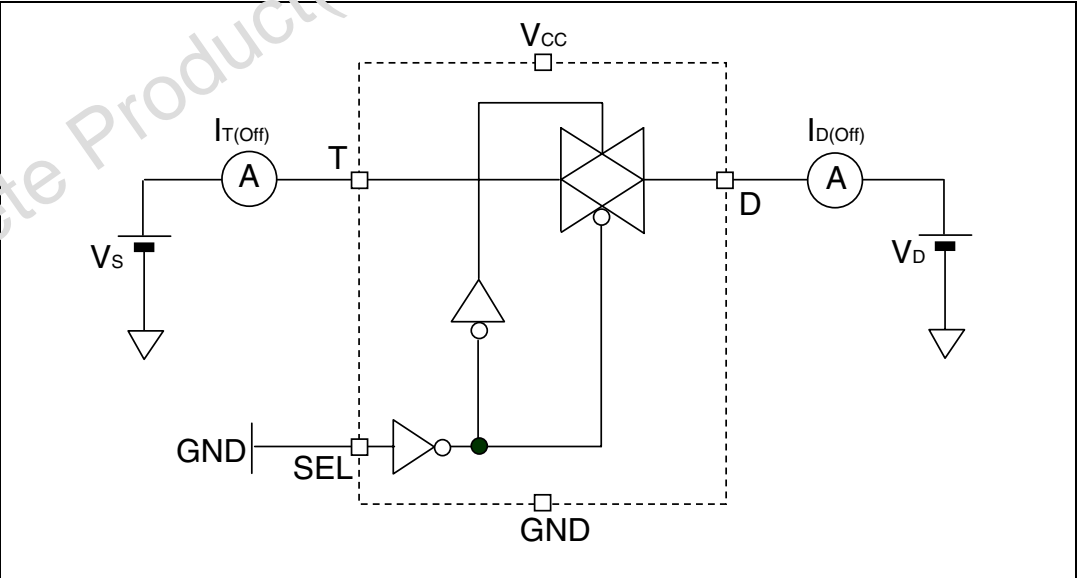


Figure 56. Switch-to-switch crosstalk

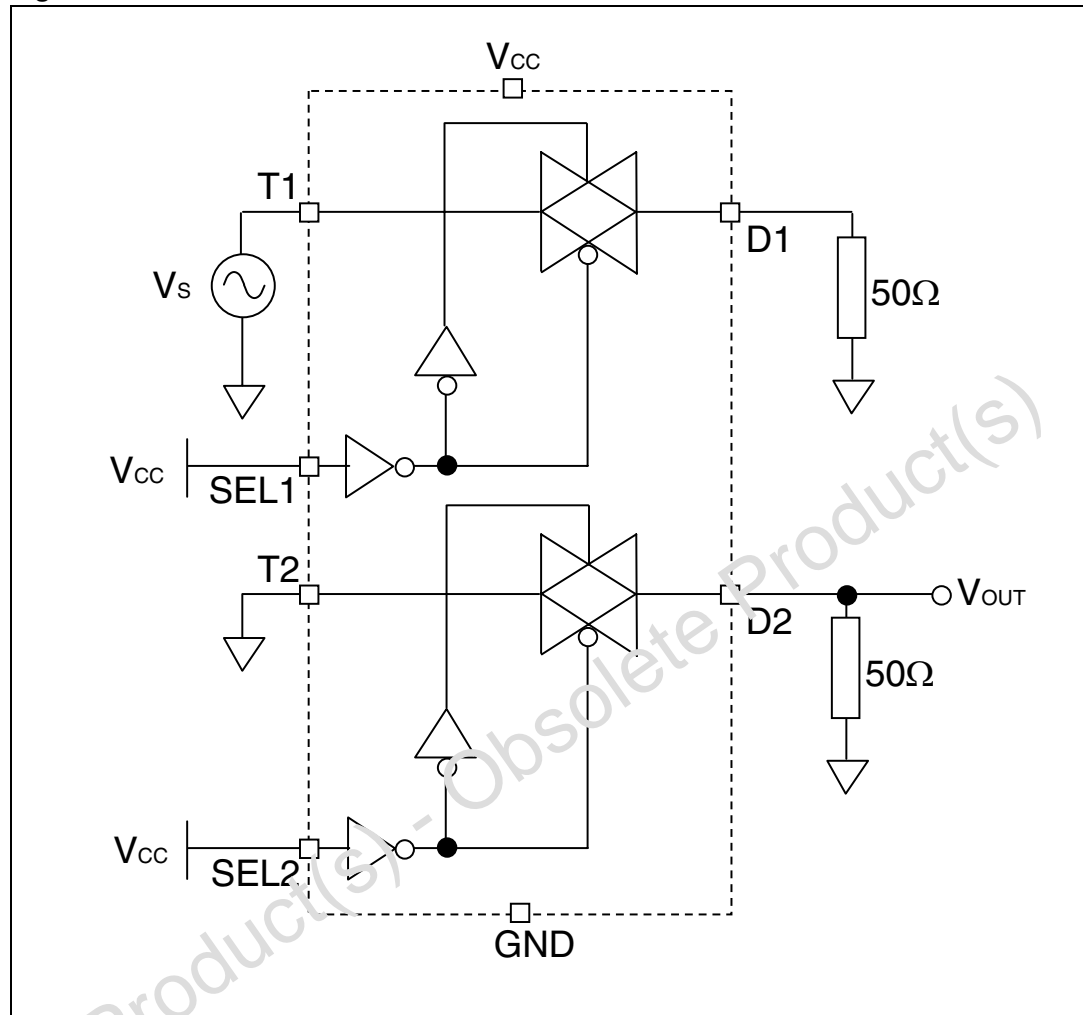
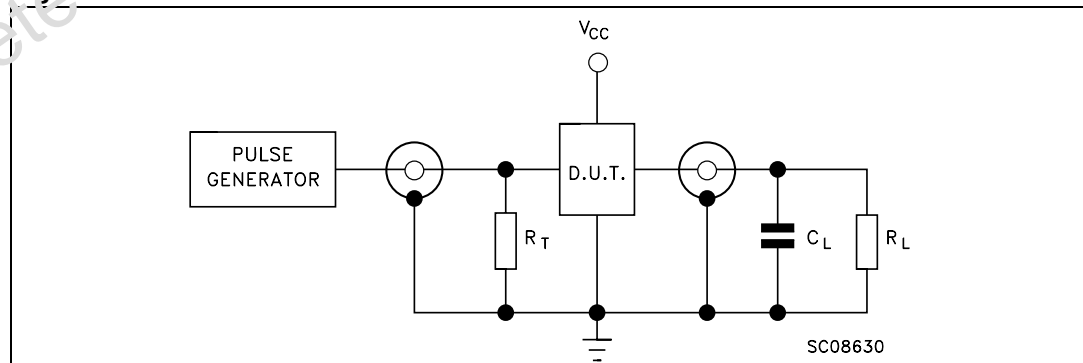


Figure 57. Test circuit



- Note:
- 1 $C_L = 5/35 \text{ pF}$ or equivalent (includes jig and probe capacitance).
 - 2 $R_L = 50 \text{ } \Omega$ or equivalent.
 - 3 $R_T = Z_{OUT}$ of pulse generator (typically $50 \text{ } \Omega$).

Figure 58. Switching time and charge injection test circuit schematics

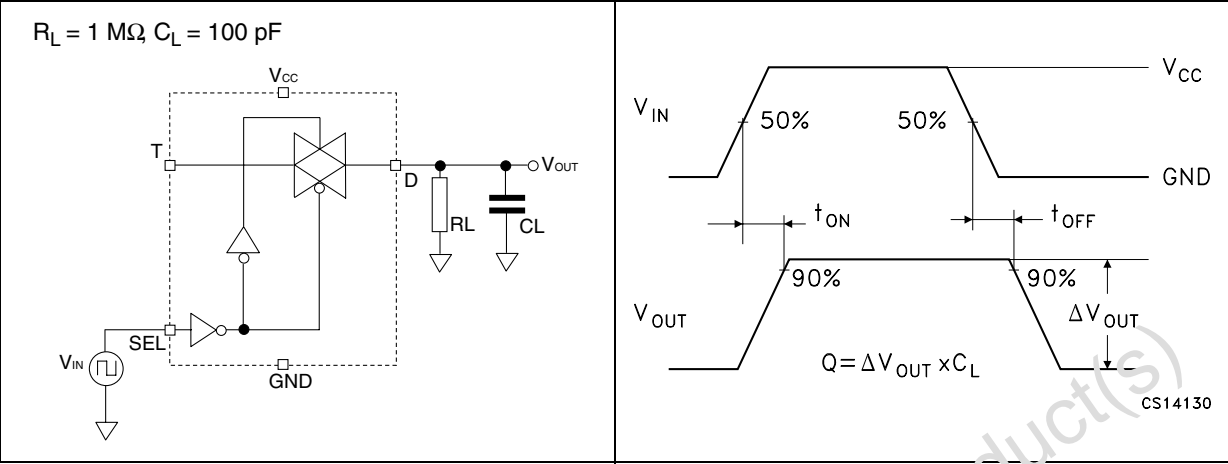


Figure 60. Turn on, turn off time test circuit schematics

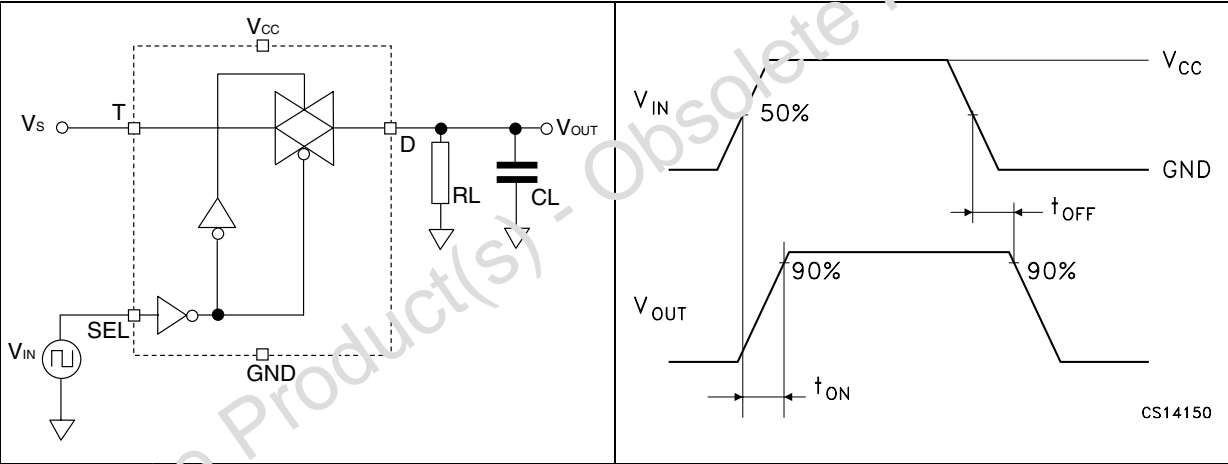


Figure 62. THD+N vs. output power

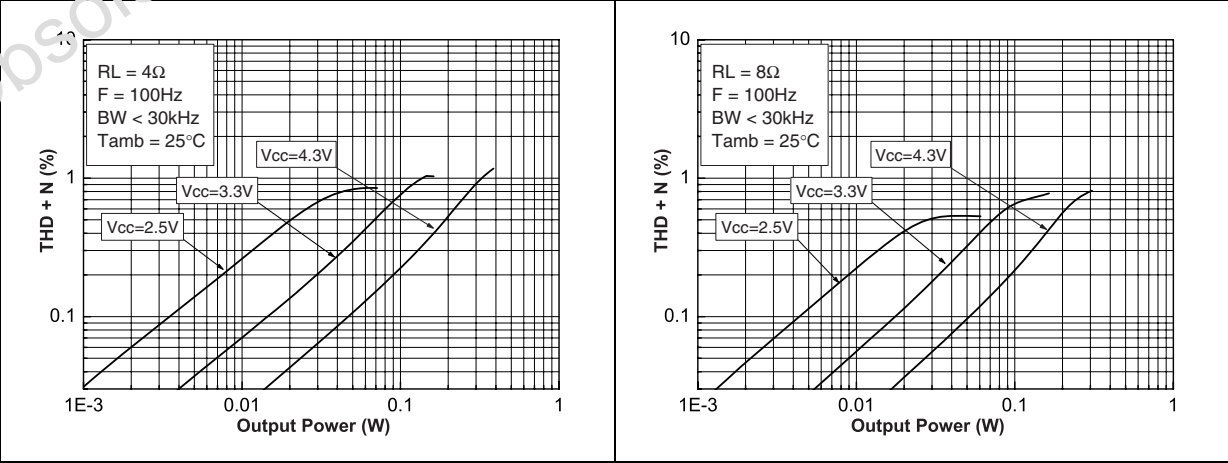


Figure 63. THD+N vs. output power

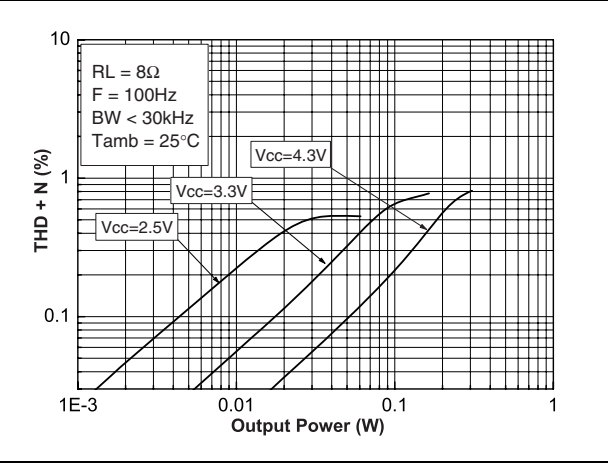


Figure 64. THD+N vs. output power

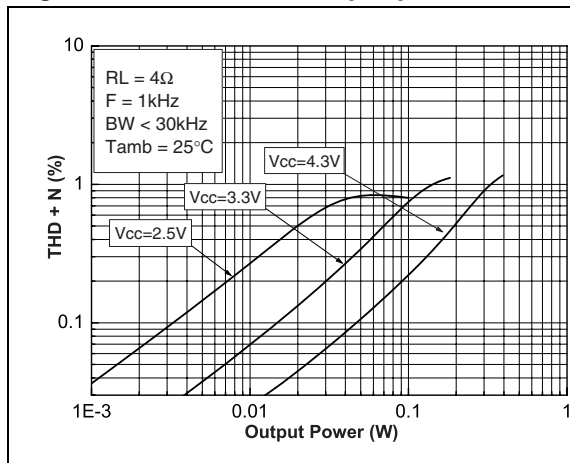


Figure 65. THD+N vs. output power

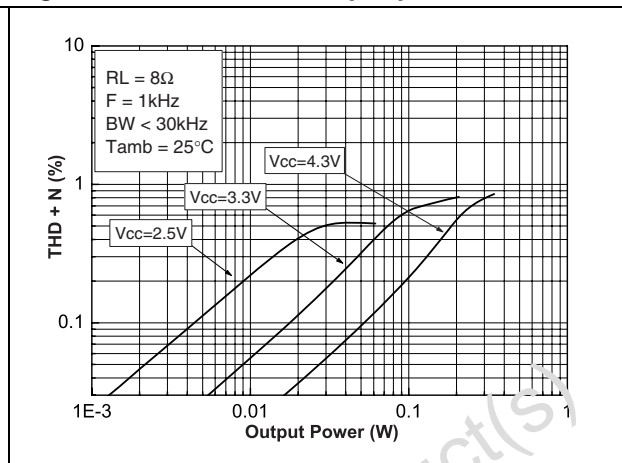


Figure 66. THD+N vs. output power

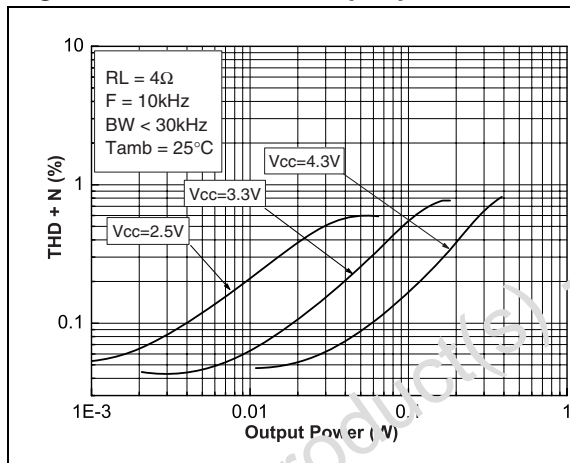


Figure 67. THD+N vs. output power

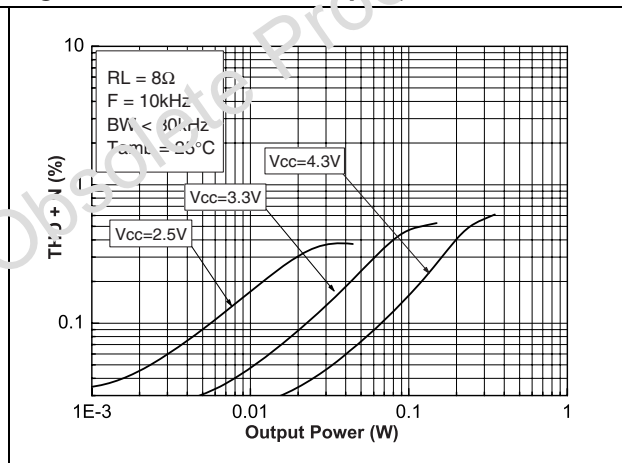


Figure 68. THD+N vs. frequency

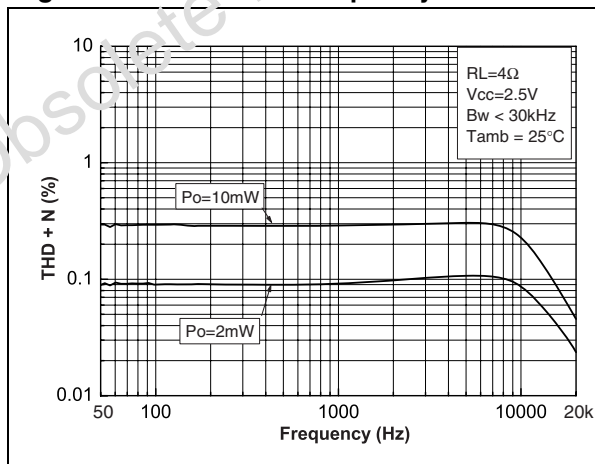


Figure 69. THD+N vs. frequency

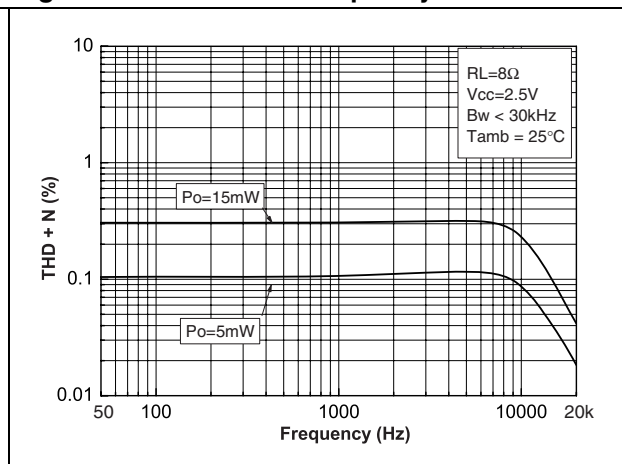


Figure 70. THD+N vs. frequency

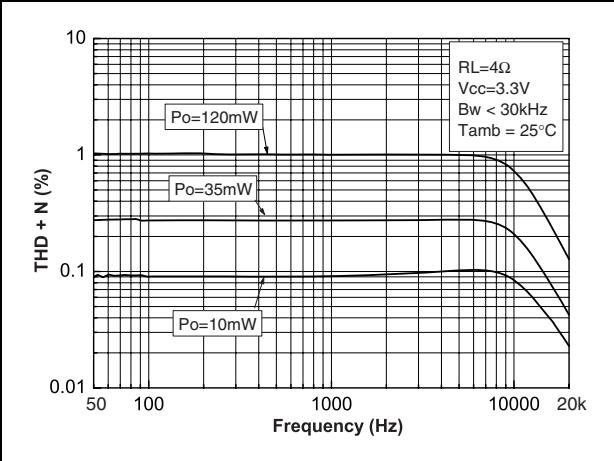


Figure 71. THD+N vs. frequency

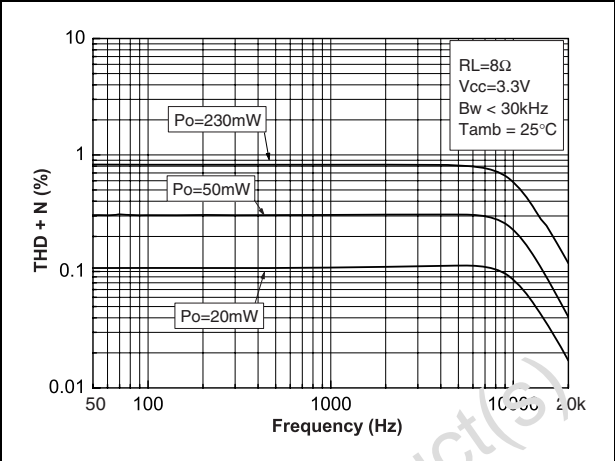


Figure 72. THD+N vs. frequency

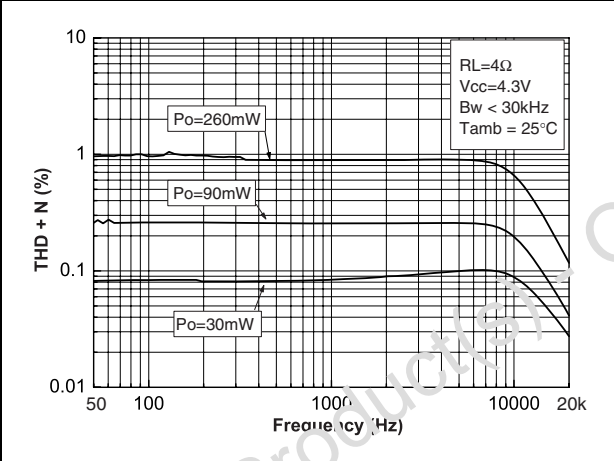


Figure 73. THD+N vs. frequency

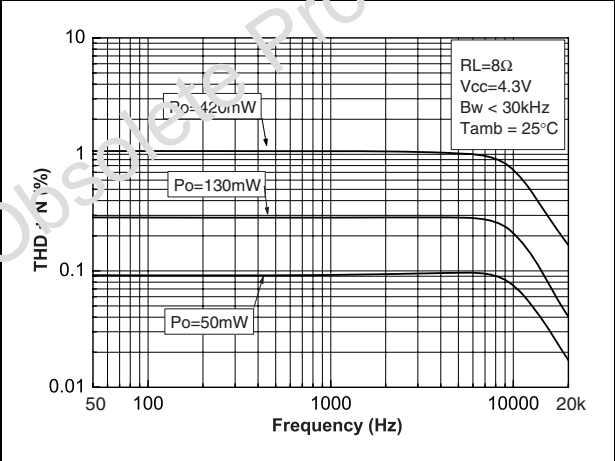
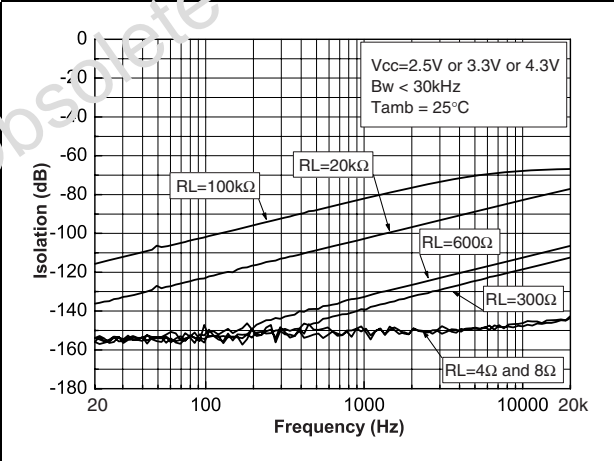


Figure 74. Isolation vs. frequency

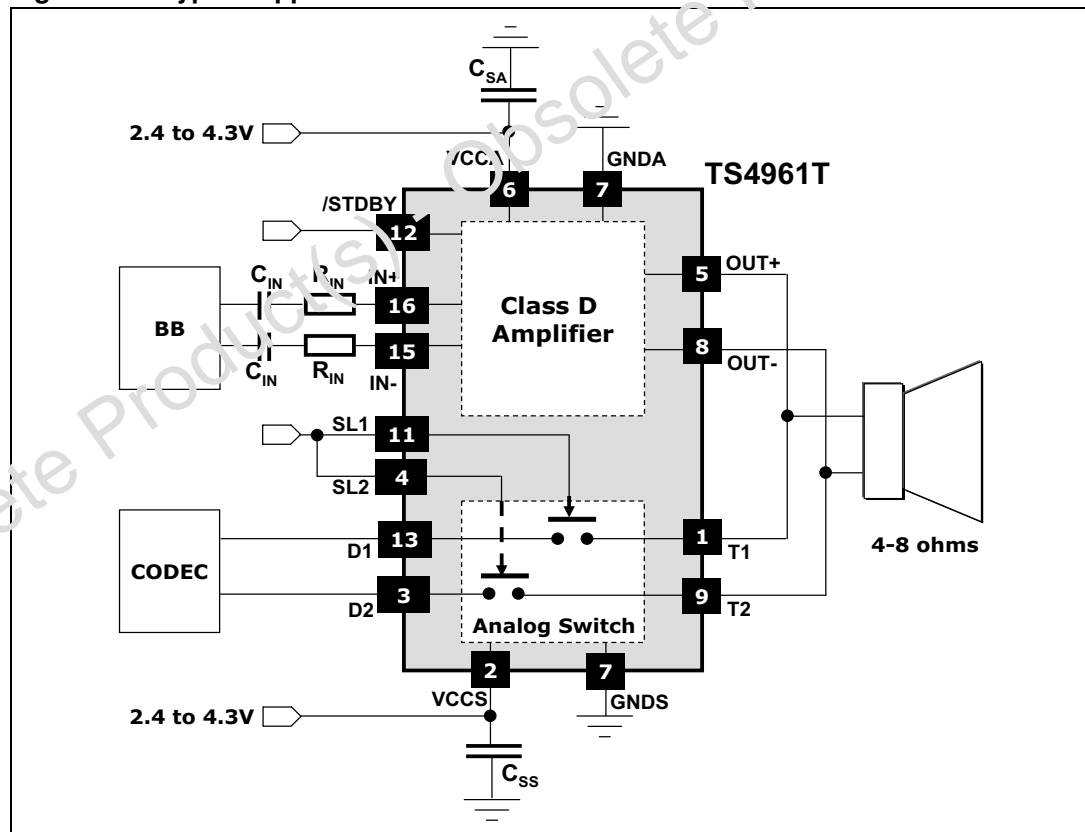


4 Application component information

Table 15. Component information

Component	Functional description
C_{SA}	Bypass supply capacitor. Install as close as possible to the VCCA pin of the TS4961T to minimize high-frequency ripple. A 1 μ F ceramic capacitor should be added to enhance power supply filtering at high frequencies (see below).
C_{SS}	Bypass supply capacitor. Install as close as possible to the VCCS pin of the TS4961T to minimize high-frequency ripple. A 100 nF ceramic capacitor should be added to enhance power supply filtering at high frequencies.
R_{IN}	Input resistor to program the TS4961T differential gain (gain = $300 \text{ k}\Omega / R_{IN}$ with R_{IN} in $\text{k}\Omega$).
C_{IN}	Because common mode feedback is implemented, these input capacitors are optional. However, they can be added to form with R_{IN} a 1st order high pass filter with a -3 dB cut-off frequency = $1/(2\pi R_{IN} C_{IN})$.

Figure 75. Typical application schematics



4.1 Common mode feedback loop limitations

The common mode feedback loop allows the output DC bias voltage to be averaged at $V_{CC}/2$ for any DC common mode bias input voltage.

However, because of the V_{icm} limitation in the input stage (see [Table 2: Operating conditions for audio amplifier section on page 3](#)), the common mode feedback loop can only fulfill its role within a defined range. This range depends upon the values of V_{CC} and R_{in} (A_v). To obtain a good estimation of the V_{icm} value, the following formula can be used (no tolerance on R_{in}):

$$V_{icm} = \frac{V_{CC} \times R_{in} + 2 \times V_{IC} \times 150k\Omega}{2 \times (R_{in} + 150k\Omega)} \quad (V)$$

with

$$V_{IC} = \frac{In^+ + In^-}{2} \quad (V)$$

and the result of the calculation must be in the range:

$$0.5V \leq V_{icm} \leq V_{CC} - 0.8V$$

Due to the +/-9% tolerance on the 150 kΩ resistor, it is also important to check V_{icm} in these conditions:

$$\frac{V_{CC} \times R_{in} + 2 \times V_{IC} \times 136.5k\Omega}{2 \times (R_{in} + 136.5k\Omega)} \leq V_{icm} \leq \frac{V_{CC} \times R_{in} + 2 \times V_{IC} \times 163.5k\Omega}{2 \times (R_{in} + 163.5k\Omega)}$$

If the result of the V_{icm} calculation is not in the previous range, input coupling capacitors must be used (with V_{CC} from 2.4 V to 2.5 V, input coupling capacitors are mandatory).

For example:

With $V_{CC} = 3$ V, $R_{in} = 150$ kΩ and $V_{IC} = 2.5$ V, we typically find $V_{icm} = 2$ V and this is lower than 3 V - 0.8 V = 2.2 V. With 136.5 kΩ we find 1.97 V, and with 163.5 kΩ we have 2.02 V. Therefore, no input coupling capacitors are required.

4.2 Low frequency response

If a low frequency bandwidth limitation is required, it is possible to use input coupling capacitors.

In the low frequency region, C_{in} (input coupling capacitor) starts to have an effect. C_{in} forms, with R_{in} , a first order high-pass filter with a -3 dB cut-off frequency:

$$F_{CL} = \frac{1}{2\pi \times R_{in} \times C_{in}} \quad (\text{Hz})$$

Therefore, for a desired cut-off frequency F_{CL} , C_{in} is calculated as follows:

$$C_{in} = \frac{1}{2\pi \times R_{in} \times F_{CL}} \quad (\text{F})$$

with R_{in} in Ω and F_{CL} in Hz.

4.3 Decoupling of the circuit

A power supply capacitor, referred to as C_S , is necessary to correctly bypass the class D part of the TS4961T.

The TS4961T has a typical switching frequency at 250 kHz and an output fall and rise time at approximately 5 ns. Because of these very fast transients, careful decoupling is mandatory.

A 1 μF ceramic capacitor is enough, but it must be located very close to the TS4961T in order to avoid any extra parasitic inductance created by a long track wire. In relation with di/dt , this parasitic inductance introduces an overvoltage that decreases the global efficiency and, if it is too high, may cause a breakdown of the device.

In addition, even if a ceramic capacitor has an adequate high frequency ESR value, its current capability is also important. A 0603 size is a good compromise, particularly when a 4 Ω load is used.

Another important parameter is the rated voltage of the capacitor. A 1 $\mu\text{F}/6.3\text{ V}$ capacitor used at 5 V, loses about 50% of its value. In fact, with a 5 V power supply voltage, the decoupling value is about 0.5 μF instead of 1 μF . Since C_S has a particular influence on the THD+N in the medium-high frequency region, this capacitor variation becomes decisive. In addition, less decoupling means higher overshoots, which can be problematic if they reach the power supply AMR value (6 V).

4.4 Wake-up time (t_{WU})

There is a wait of approximately 5 ms when standby is released to set the device ON. The TS4961T has an internal digital delay that mutes the outputs and releases them after this time in order to avoid any pop noise.

4.5 Shutdown time (t_{STBY})

When the standby command is set, the time required to put the two output stages into high impedance and to put the internal circuitry in standby mode, is about 5 ms. This time is used to decrease the gain and avoid any pop noise during shutdown.

4.6 Consumption in standby mode

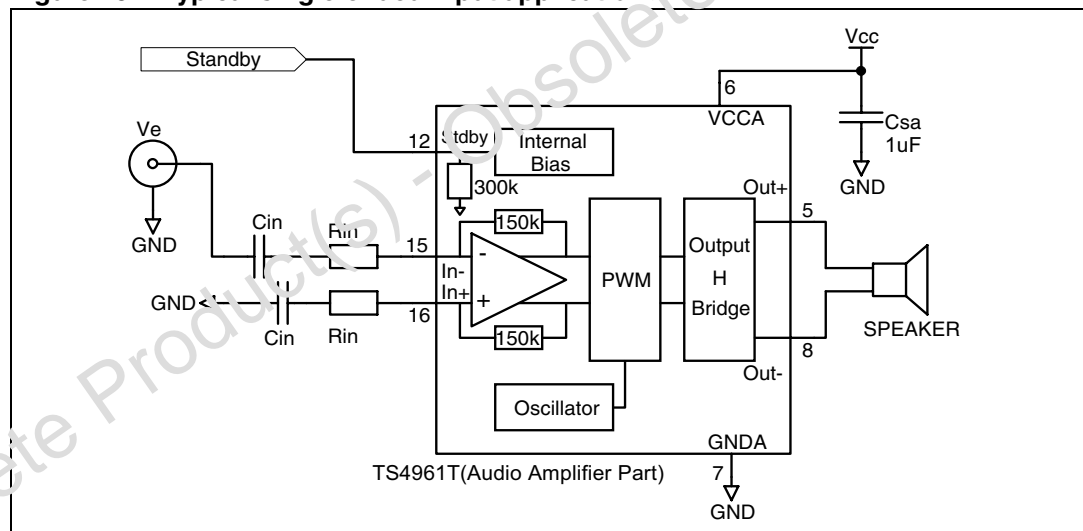
Between the shutdown pin and GND there is an internal 300 k Ω resistor. This resistor forces the TS4961T to switch to standby mode when the standby input is left floating.

However, this resistor also introduces additional power consumption if the standby pin voltage is not 0 V.

4.7 Single-ended input configuration

The TS4961T can be used in a single-ended input configuration, but in this configuration coupling capacitors are necessary. [Figure 76](#) shows a typical single-ended input application.

Figure 76. Typical single-ended input application



All formulas are identical except for the gain (with R_{in} in k Ω):

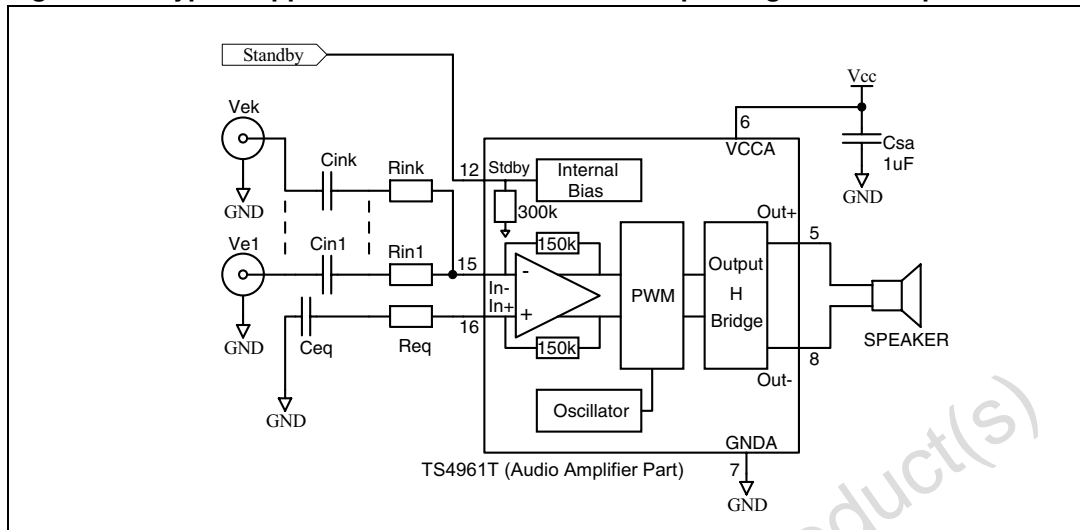
$$A_{V_{single}} = \frac{V_e}{Out^+ - Out^-} = \frac{300}{R_{in}}$$

Due to the internal resistor tolerance, $A_{V_{single}}$ is in the range of:

$$\frac{273}{R_{in}} \leq A_{V_{single}} \leq \frac{327}{R_{in}}$$

In the event that multiple single-ended inputs are summed, it is important that the impedance on both TS4961 inputs (In^- and In^+) be equal.

Figure 77. Typical application schematics with multiple single-ended inputs



We have the following equations.

$$\text{Out}^+ - \text{Out}^- = V_{e1} \times \frac{300}{R_{in1}} + \dots + V_{ek} \times \frac{300}{R_{ink}} \quad (\text{V})$$

$$C_{eq} = \sum_{j=1}^k C_{inj}$$

$$C_{inj} = \frac{1}{2 \times \pi \times R_{inj} \times F_{CLj}} \quad (\text{F})$$

$$R_{eq} = \frac{1}{\sum_{j=1}^k \frac{1}{R_{inj}}}$$

In general, for mixed situations (single-ended and differential inputs), the same rule must be used, that is, to equalize impedance on both TS4961T inputs.

4.8 Output filter considerations

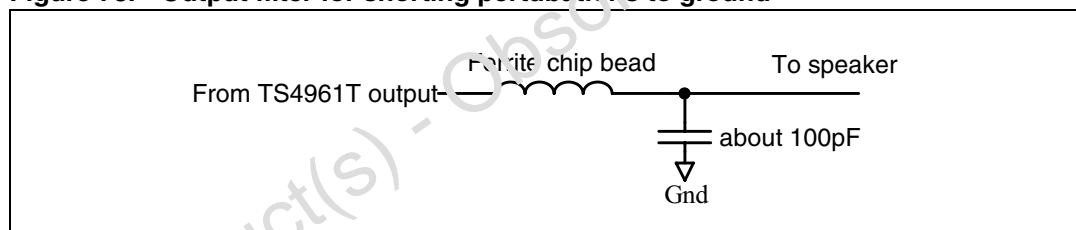
The TS4961T is designed to operate without an output filter. However, due to very sharp transients on the TS4961T output, EMI radiated emissions may cause some standard compliance issues.

These EMI standard compliance issues can appear if the distance between the TS4961T outputs and loudspeaker terminal are long (typically more than 50 mm, or 100 mm in both directions, to the speaker terminals). Since the PCB layout and internal equipment device are different for each configuration, it is difficult to provide a one-size-fits-all solution.

However, to decrease the probability of EMI issues, there are several simple rules to follow.

- Reduce, as much as possible, the distance between the TS4961T output pins and the speaker terminals.
- Use ground planes for shielding sensitive wires.
- Place, as close as possible to the TS4961T and in series with each output, a ferrite bead with a rated current of 2.5 A minimum, and impedance greater than 50 Ω at frequencies above 30 MHz. If, after testing, these ferrite beads are not necessary, replace them by a short circuit.
- Allow enough footprint to place, if necessary, a capacitor to short perturbations to ground as shown in [Figure 78](#).

Figure 78. Output filter for shorting perturbations to ground



In the case where the distance between the TS4961T outputs and speaker terminals is high, it is possible to have low frequency EMI issues due to the fact that the typical operating frequency is 250 kHz.

In this configuration, it is recommended to use an output filter. It should be placed as close as possible to the TS4961T.

4.9.1 Example 1: dual differential inputs

The diagram illustrates the internal structure of the TS4961T (Audio Amplifier Part). Key components and connections include:

- Inputs:** E2+, E1+, E1-, and E2- are connected through resistors R2 and R1 to pins 12, 15, 16, and 17 respectively. A Standby signal is connected to pin 12.
- Internal Components:** The chip contains an Internal Bias network (300k resistor), an Op-Amp (with 150k feedback resistors), a PWM block, an Oscillator, and an Output H Bridge.
- Power Supply:** VCCA (pin 6) is connected to Vcc through a 1uF capacitor (Csa). GND (pin 7) is connected to GND.
- Outputs:** The Output H Bridge drives the speaker through pins 5 (Out+) and 8 (Out-).

$$A_{V_1} = \frac{Out^+ - Out^-}{E_1^+ - E_1^-} = \frac{300}{R_1}$$

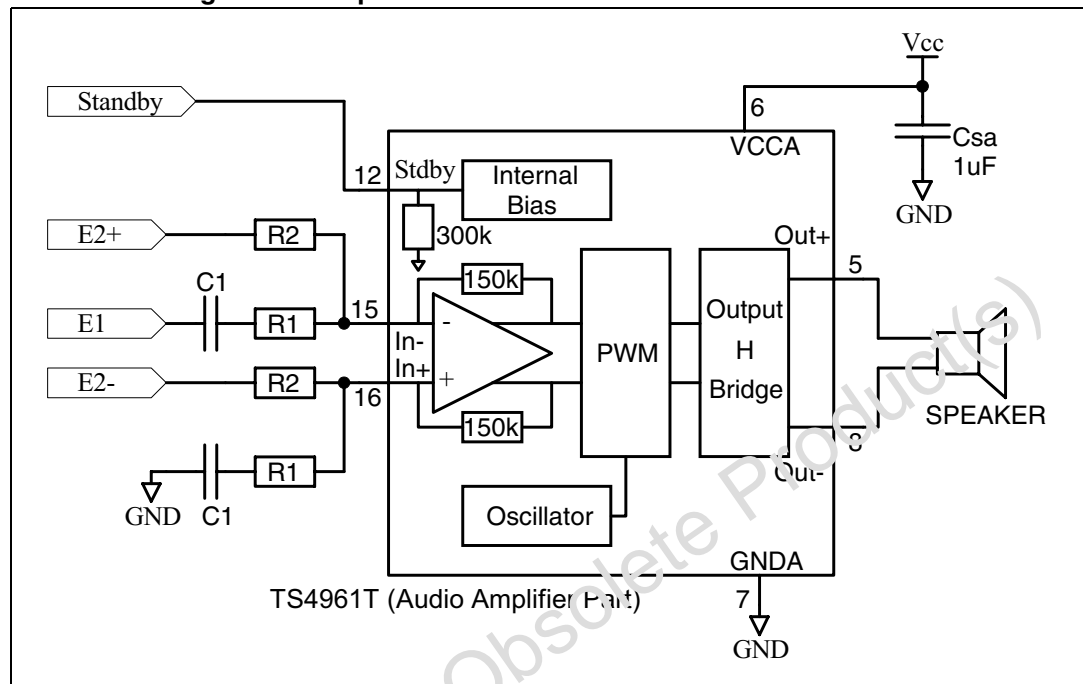
$$A_{V_2} = \frac{Out^+ - Out^-}{E_2^+ - E_2^-} = \frac{300}{R_2}$$

$$0.5V \leq \frac{V_{CC} \times R_1 \times R_2 + 300 \times (V_{IC1} \times R_2 + V_{IC2} \times R_1)}{300 \times (R_1 + R_2) + 2 \times R_1 \times R_2} \leq V_{CC} - 0.8V$$

$$V_{IC_1} = \frac{E_1^+ + E_1^-}{2} \quad \text{and} \quad V_{IC_2} = \frac{E_2^+ + E_2^-}{2}$$

4.9.2 Example 2: one differential input plus one single-ended input

Figure 80. Typical application schematics with one differential input plus one single-ended input



With (R_i in $k\Omega$):

$$A_{V_1} = \frac{Out^+ - Out^-}{E_1^+} = \frac{300}{R_1}$$

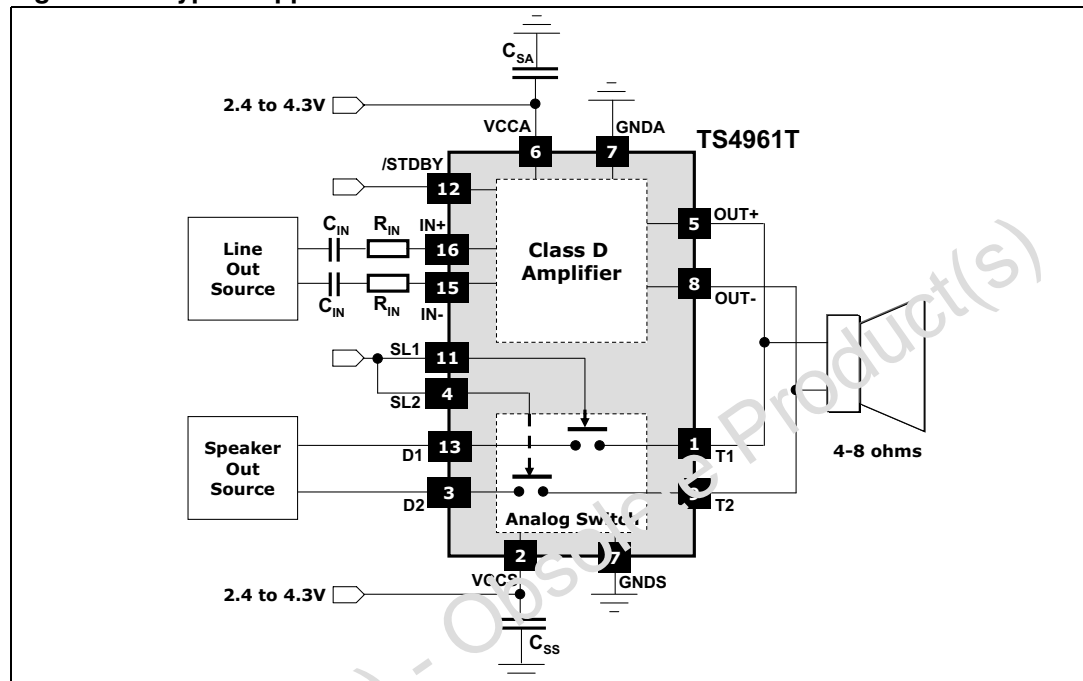
$$A_{V_2} = \frac{Out^+ - Out^-}{E_2^+ - E_2^-} = \frac{300}{R_2}$$

$$C_1 = \frac{1}{2\pi \times R_1 \times F_{CL}} \quad (F)$$

4.10 Using the audio amplifier and switch on the same speaker

The TS4961T can be used to supply a speaker with two different sources. The typical application is shown in [Figure 81](#).

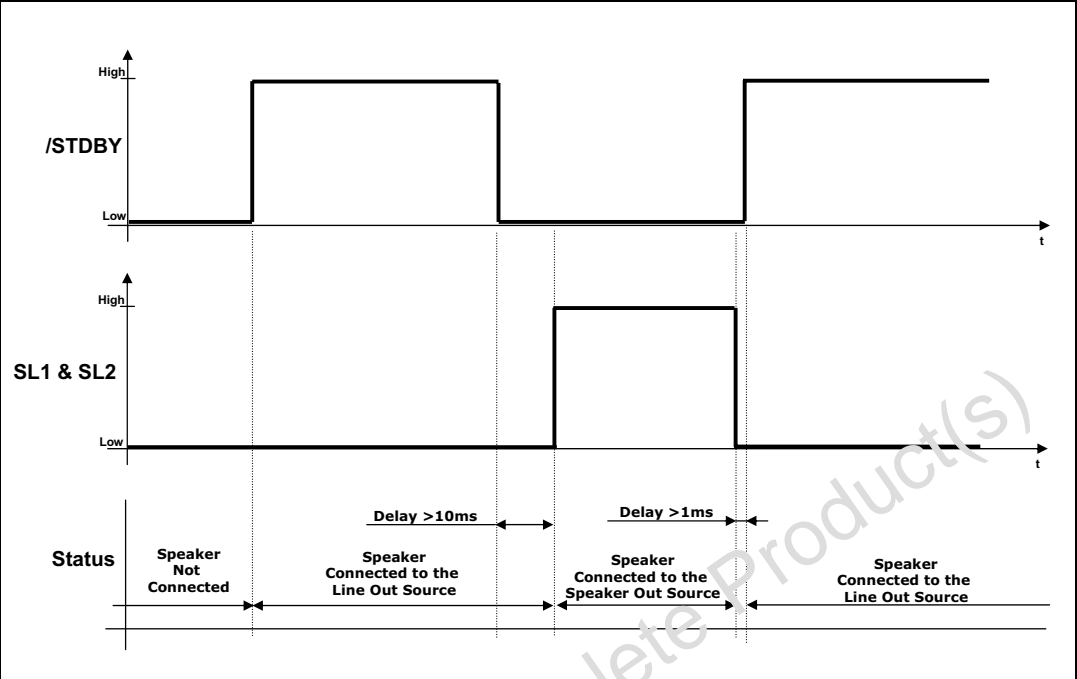
Figure 81. Typical application schematics for the TS4961T



The first source is a line-out signal provided by the baseband and the second is a speaker-out signal coming from the CODEC. Switching is done through the standby pin (/STDBY) of the audio amplifier and through the SLn pins of the switch.

Note that, as shown in [Figure 82](#), all pins should not be switched at the same time because this can cause damage to the TS4961T audio amplifier and to the external audio amplifier that provides the speaker-out signal.

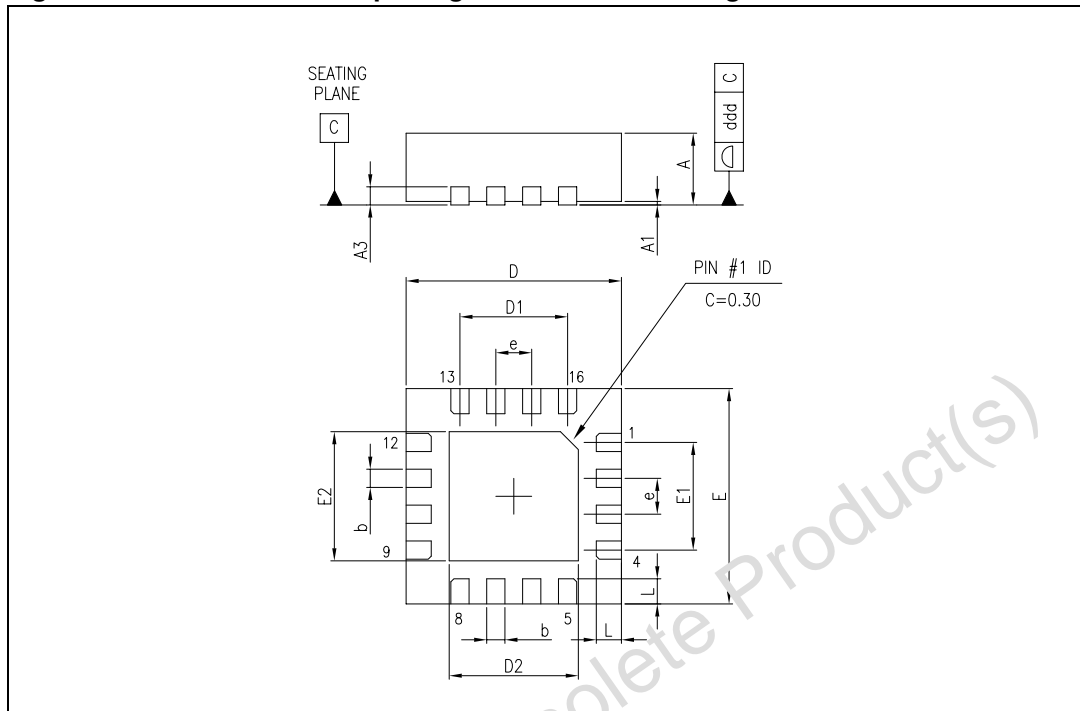
Figure 82. Timing of switching between two audio sources



5 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK[®] packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

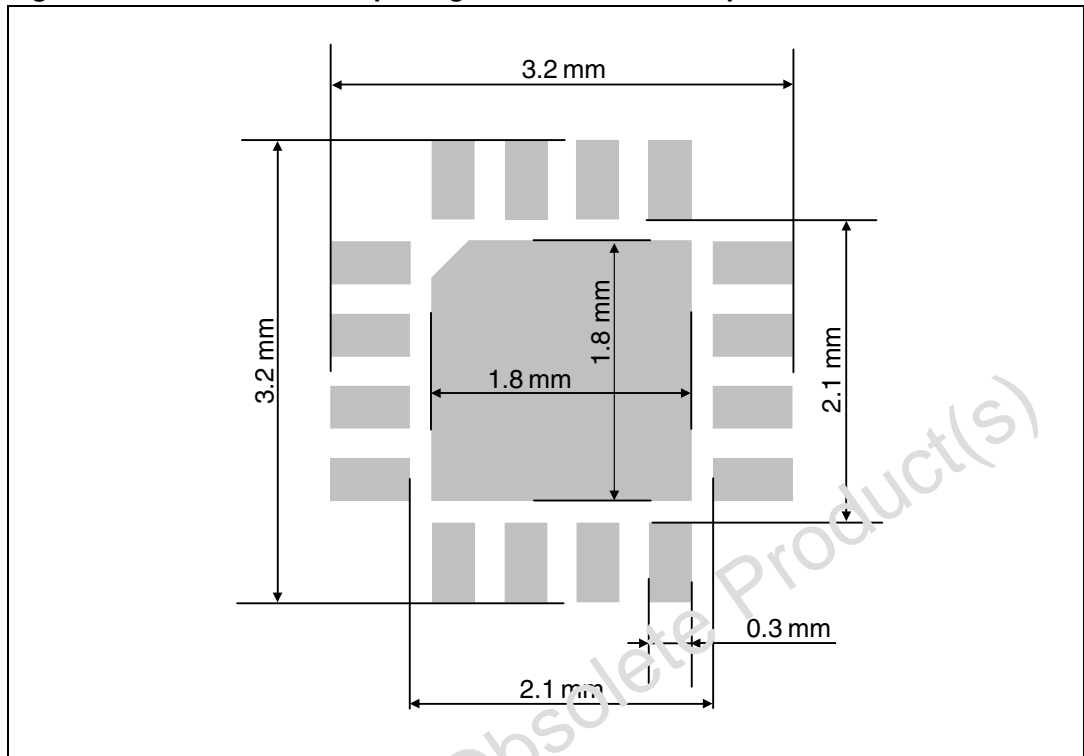
Obsolete Product(s) - Obsolete Product(s)

Figure 83. QFN16 3 x 3 mm package mechanical drawing

Note: For enhanced thermal performance the exposed pad must be soldered to a copper area on the PCB, acting as a heatsink. This copper area can be electrically connected to pins 7 and 10 or left floating.

Table 16. QFN16 3 x 3 mm package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1		0.02	0.05		0.001	0.002
A3		0.20			0.008	
b	0.18	0.25	0.30	0.007	0.01	0.012
D	2.85	3.00	3.15	0.112	0.118	0.124
D1		1.50			0.059	
D2	1.70	1.80	1.90	0.067	0.071	0.075
E	2.85	3.00	3.15	0.112	0.118	0.124
E1		1.50			0.059	
E2	1.70	1.80	1.90	0.067	0.071	0.075
e	0.45	0.50	0.55	0.018	0.020	0.022
L	0.30	0.40	0.50	0.012	0.016	0.020
ddd			0.08			0.003

Figure 84. QFN16 3 x 3 mm package recommended footprint

Note: The substrate pad should be tied to the FCB GND.

6 Ordering information

Table 17. Order codes

Order code	Temperature range	Package	Packing	Marking
TS4961TIQT	-40°C to +85°C	QFN16	Tape & reel	K61T

7 Revision history

Table 18. Document revision history

Date	Revision	Changes
16-Sep-2008	1	Initial release.

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