



ULN2064B, ULN2066B ULN2068B, ULN2074B

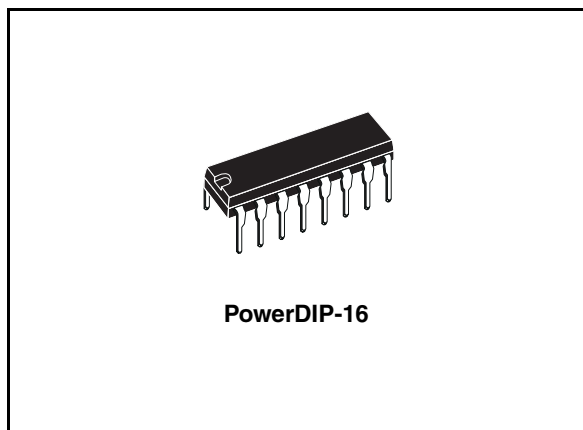
50 V - 1.5 A quad Darlington switches

Features

- Output current to 1.5 A for each Darlington
- Minimum breakdown 50 V
- Sustaining voltage at least 35 V
- Integral suppression diodes (ULN2064B, ULN2066B and ULN2068B)
- Isolated Darlington pinout (ULN2074B)
- Versions compatible with all popular logic families

Description

Designed to interface logic to a wide variety of high current, high voltage loads, these devices each contain four NPN Darlington switches delivering up to 1.5 A with a specified minimum breakdown of 50 V and a sustaining voltage of 35 V measured at 100 mA. The ULN2064B, ULN2066B and ULN2068B contain integral suppression diodes for inductive loads have common emitters. The ULN2074B feature isolated Darlington pinouts and is intended for



applications such as emitter follower configurations. Inputs of the ULN2064B, ULN2068B and ULN2074B are compatible with popular 5 V logic families and the ULN2066B are compatible with 6 - 15 V CMOS and PMOS. Type ULN2068B includes a pre-driver stage to reduce loading on the control logic.

Table 1. Device summary

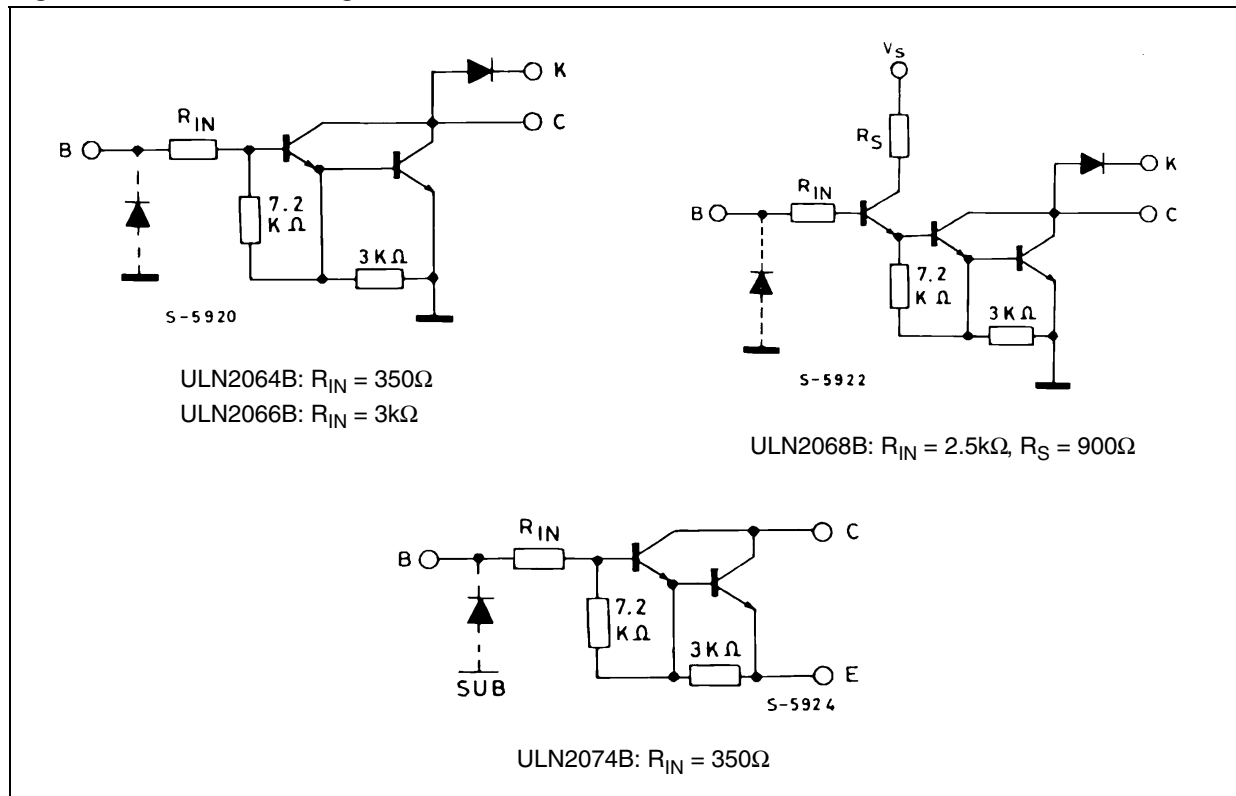
Part numbers	Package
ULN2064B	PowerDIP-16
ULN2066B	PowerDIP-16
ULN2068B	PowerDIP-16
ULN2074B	PowerDIP-16

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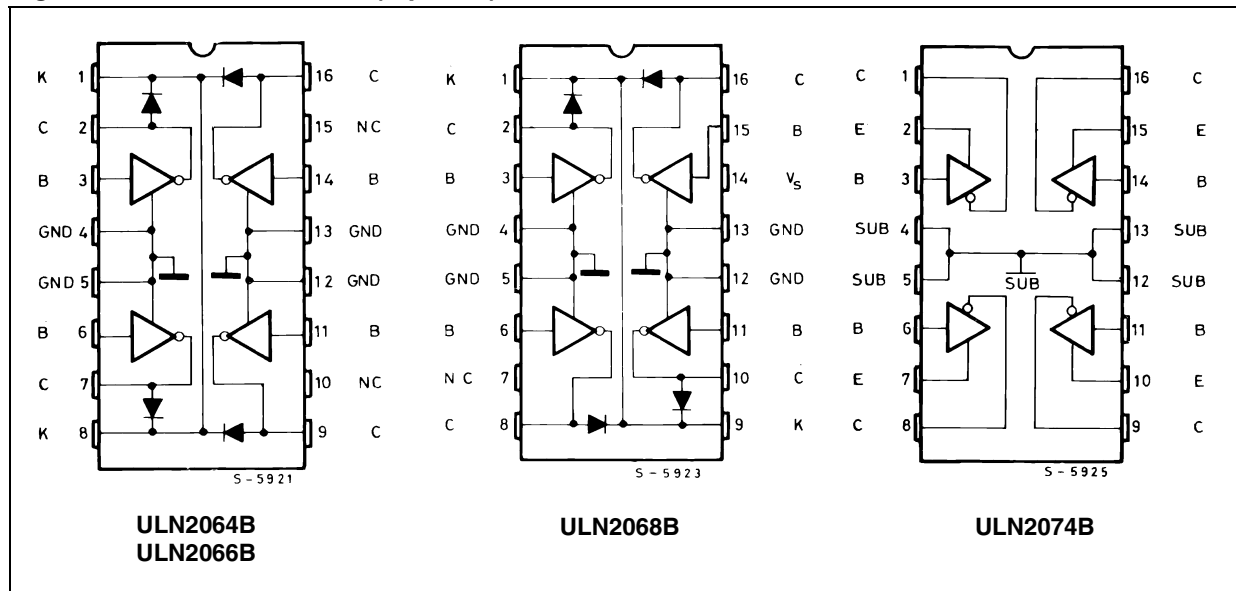
1 Diagram

Figure 1. Schematic diagrams



2 Pin configuration

Figure 2. Pin connections (top view)



3 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CEX}	Output voltage	50	V
$V_{CE(SUS)}$	Output sustaining voltage	35	V
I_O	Output current	1.75	A
V_I	Input voltage ULN2066B - 2074B	30	V
	Input voltage ULN2064B - 2068B	15	
I_I	Input current	25	mA
V_S	Supply voltage for ULN2068B	10	V
P_{TOT}	Power dissipation at $T_{PINS} = 90\text{ °C}$	4.3	W
	Power dissipation at $T_{AMB} = 70\text{ °C}$	1	
T_{AMB}	Operating ambient temperature range	- 20 to 85	°C
T_{STG}	Storage temperature	- 55 to 150	°C

4 Electrical characteristics

Table 3. Electrical characteristics ($T_A = 25^\circ\text{C}$ unless otherwise specified).

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{CEX}	Output leakage current (<i>Figure 5</i>)	$V_{CE} = 50\text{V}$, $T_A = 25^\circ\text{C}$			100	μA
		$V_{CE} = 50\text{V}$, $T_A = 70^\circ\text{C}$			500	
$V_{CE(SUS)}$	Collector-emitter sustaining voltage (<i>Figure 4</i>)	$I_C = 100\text{mA}$, $V_I = 0.4\text{V}$	35			V
$V_{CE(SAT)}$	Collector-emitter saturation voltage (<i>Figure 5</i>)	$I_C = 500\text{mA}$, $I_B = 325\mu\text{A}$			1.1	V
		$I_C = 750\text{mA}$, $I_B = 935\mu\text{A}$			1.2	
		$I_C = 1\text{A}$, $I_B = 1.25\text{mA}$			1.3	
		$I_C = 1.25\text{A}$, $I_B = 2\text{mA}$			1.4	
$I_{I(ON)}$	Input current (<i>Figure 6</i>)	for ULN2064B and ULN2074B $V_I = 2.4\text{V}$ $V_I = 3.75\text{V}$	1.4 3.3		4.3 9.6	mA
		for ULN2066B, $V_I = 5\text{V}$ $V_I = 12\text{V}$	0.6 1.7		1.8 5.2	
		for ULN2068B, $V_I = 2.75\text{V}$ $V_I = 3.75\text{V}$			0.55 1.0	
$V_{I(ON)}$	Input voltage (<i>Figure 7</i>)	$V_{CE} = 2\text{V}$, $I_C = 1\text{A}$ ULN2064B, ULN2074B, ULN2066B			2 6.5	V
		$V_{CE} = 2\text{V}$, $I_C = 1.5\text{A}$ ULN2064B, ULN2074B, ULN2066B ULN2068B			2.5 10 2.75	
I_S	Supply current (<i>Figure 10</i>)	for ULN2068B, $V_I = 2.75\text{V}$, $I_C = 500\text{mA}$			6	mA
t_{PLH}	Turn-on delay time	$0.5 V_I$ to $0.5V_O$			1	μs
t_{PHL}	Turn-off delay time	$0.5 V_I$ to $0.5V_O$			1.5	μs
I_R	Clamp diode leakage current (<i>Figure 8</i>)	For ULN2064B - ULN2066B - ULN2068B, $V_R = 50\text{V}$ $T_A = 25^\circ\text{C}$ $T_A = 70^\circ\text{C}$			50 100	μA
V_F	Clamp diode forward voltage (<i>Figure 9</i>)	For ULN2064B - ULN2066B - ULN2068B $I_F = 1\text{A}$ $I_F = 1.5\text{A}$			1.75 2	V

Note: Input voltage is with reference to the substrate (no connection to any other pins) for the ULN2074B reference is ground for all other types.

Note: 1 Input current may be limited by maximum allowable input voltage.

5 Test circuits

Figure 3. Output leakage current

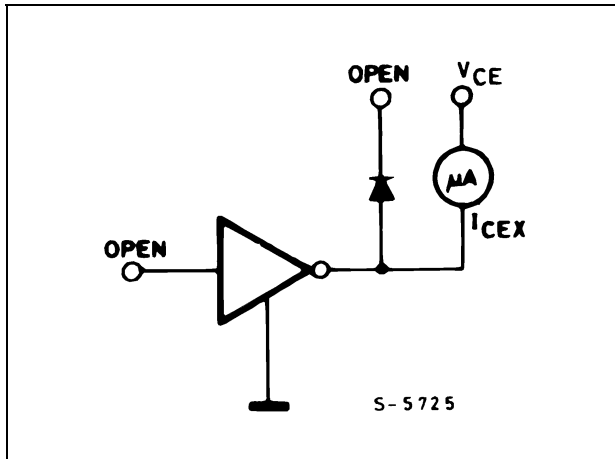


Figure 4. Collector-emitter sustaining voltage

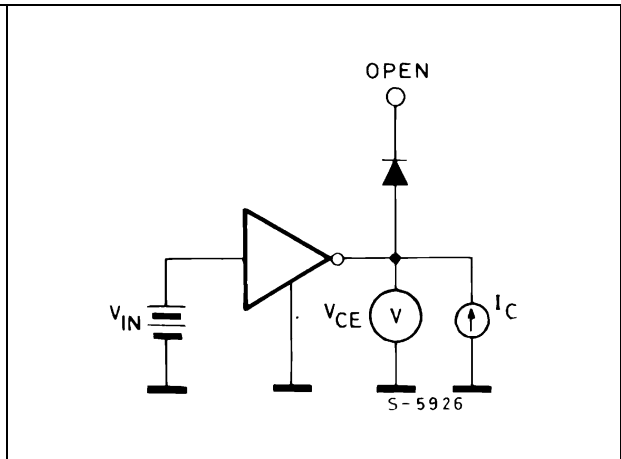


Figure 5. Collector-emitter saturation voltage Figure 6. Input current (ON)

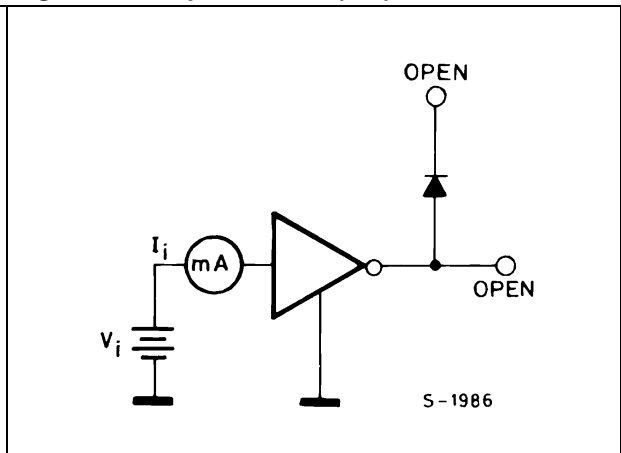
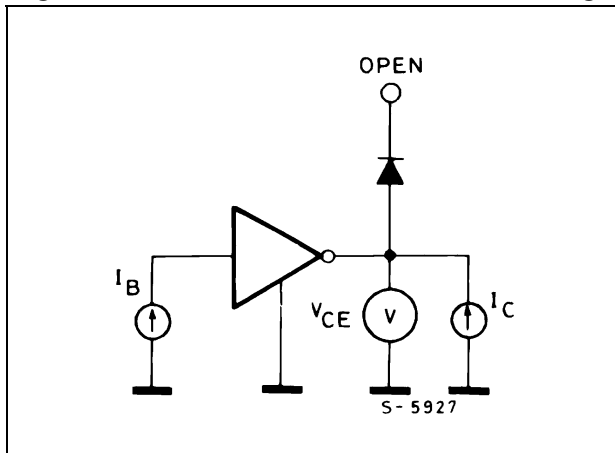


Figure 7. Input voltage

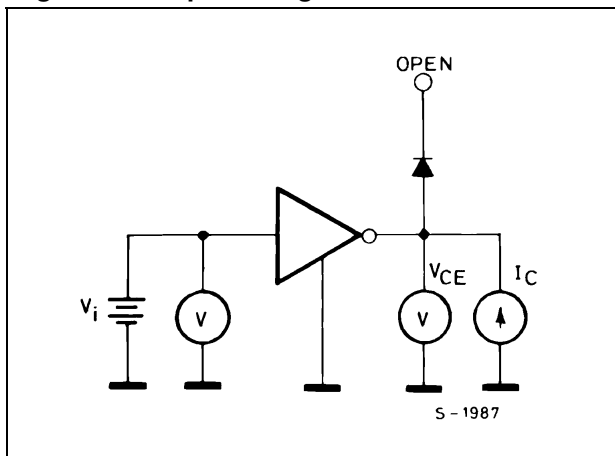


Figure 8. Clamp diode leakage current

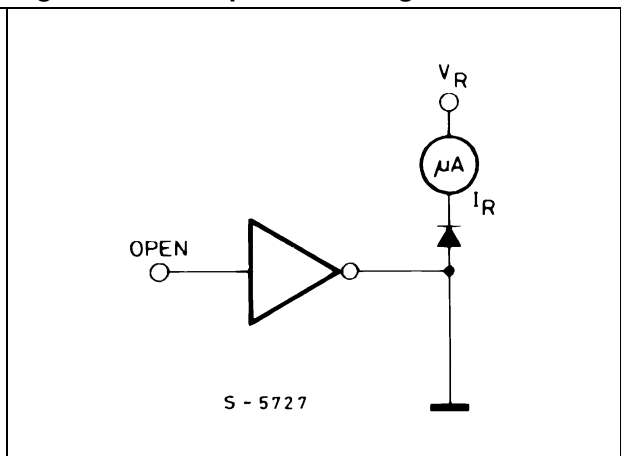


Figure 9. Clamp diode forward voltage

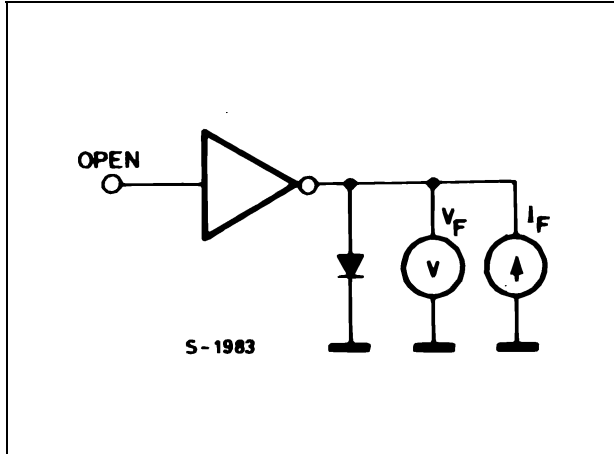


Figure 10. Supply current

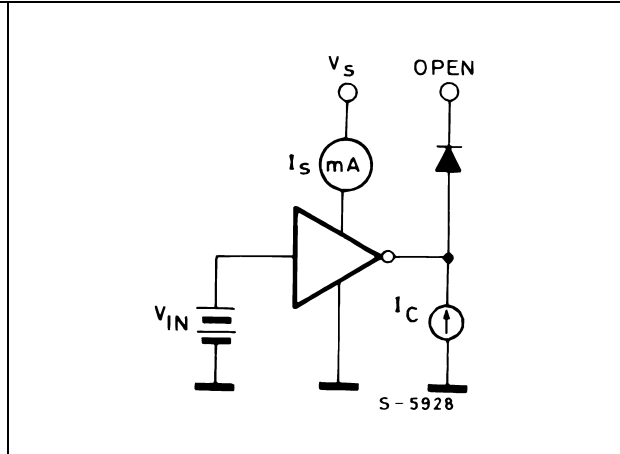


Figure 11. Input current as a function of input voltage

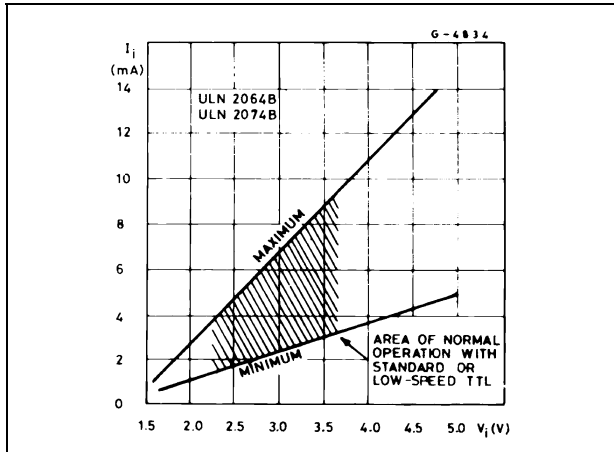


Figure 12. Input current as a function of input voltage

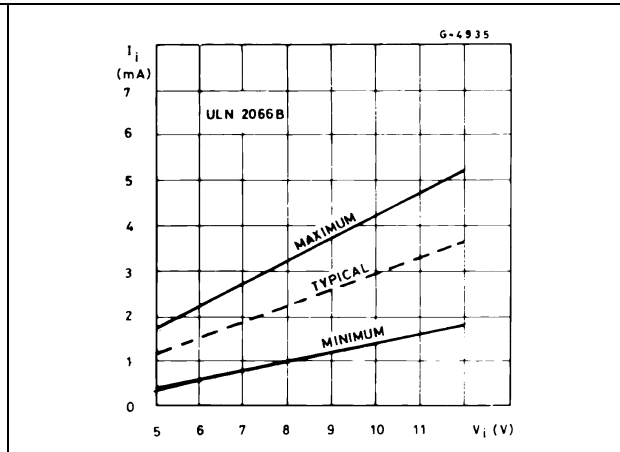
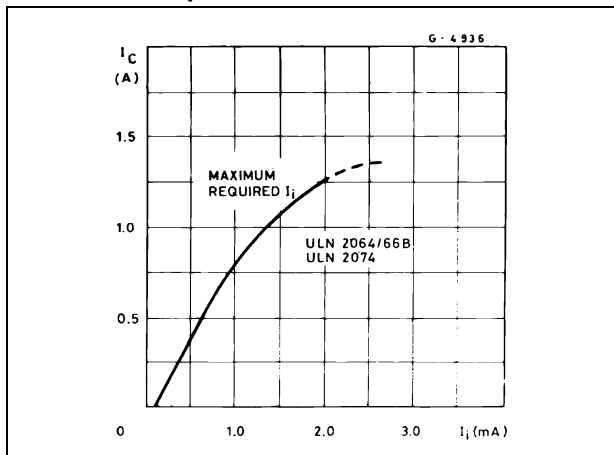


Figure 13. Collector current as a function of input current



6 Mounting instructions

The R_{thJA} can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Figure 14) or to an external heatsink (Figure 15).

The diagram of Figure 16 shows the maximum dissipated power P_{TOT} and the R_{thJA} as a function of the side "α" of two equal square copper areas having a thickness of 35 μ (1.4 mils).

During soldering the pins temperature must not exceed 260 °C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

Figure 14. Example of P.C. board area which is used as heatsink **Figure 15. External heatsink mounting example**

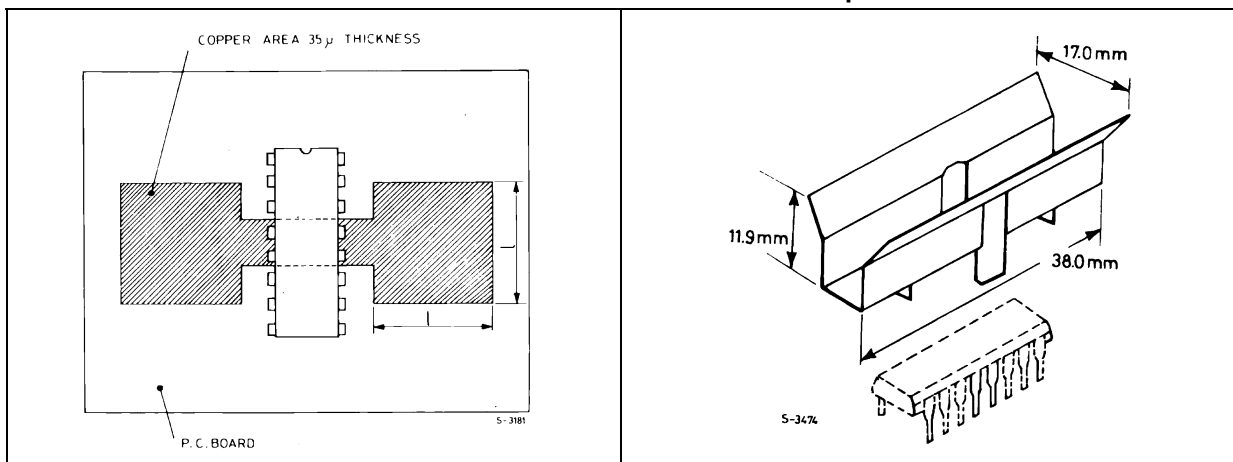


Figure 16. Maximum dissipated power and junction to ambient thermal resistance vs. side "α"

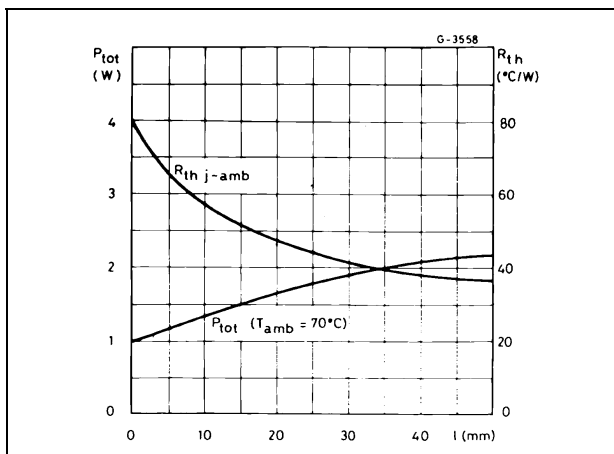
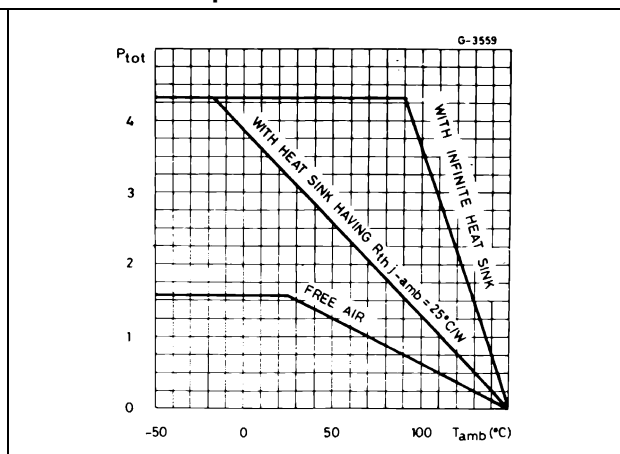


Figure 17. Maximum allowable power dissipation vs. ambient temperature



7 Typical applications

Figure 18. Common-anode LED drivers

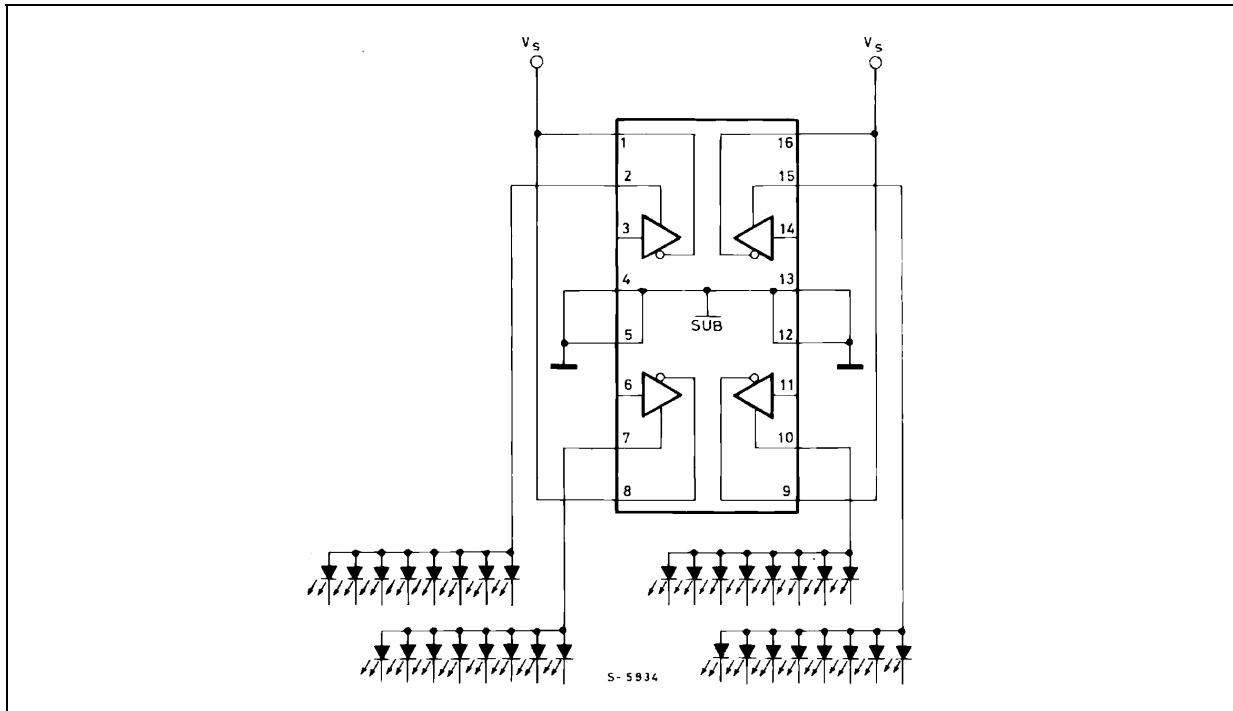
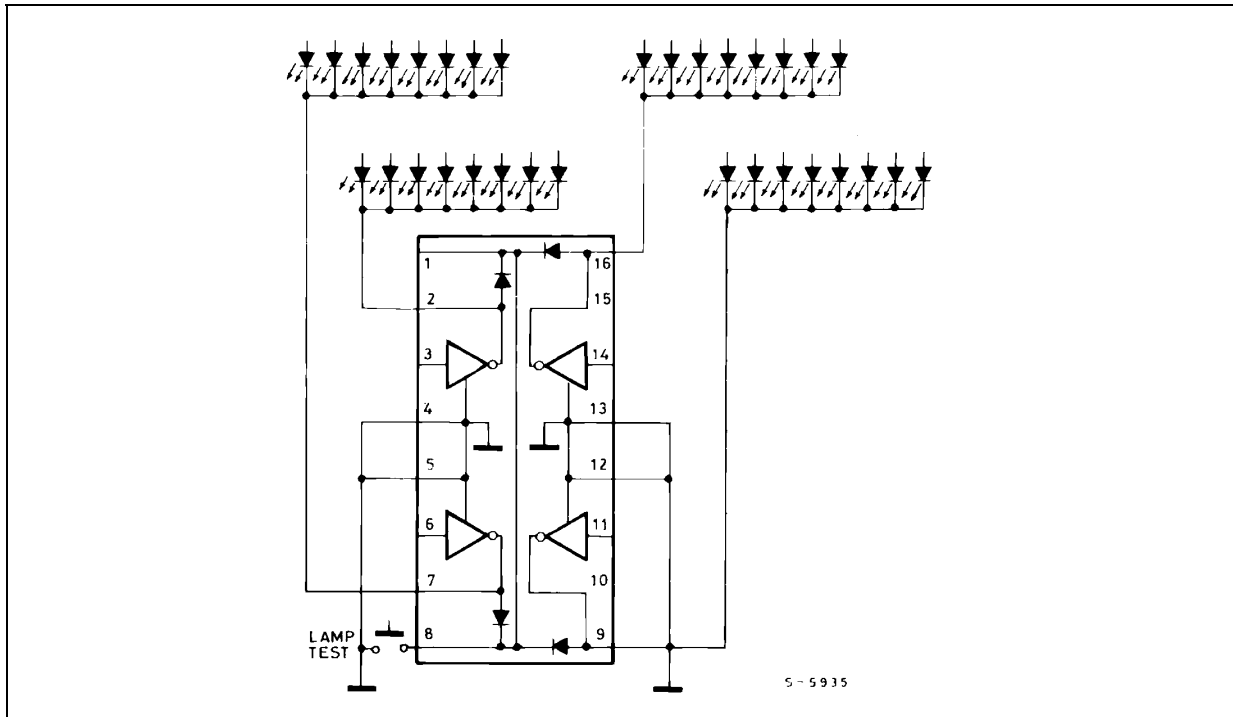


Figure 19. Common-cathode LED drivers

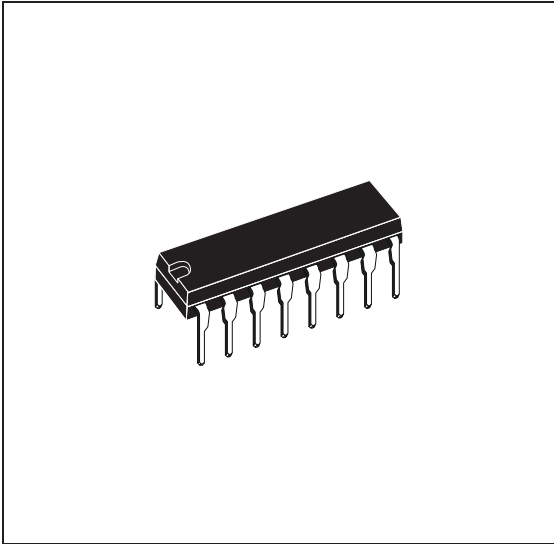


8 Package mechanical data

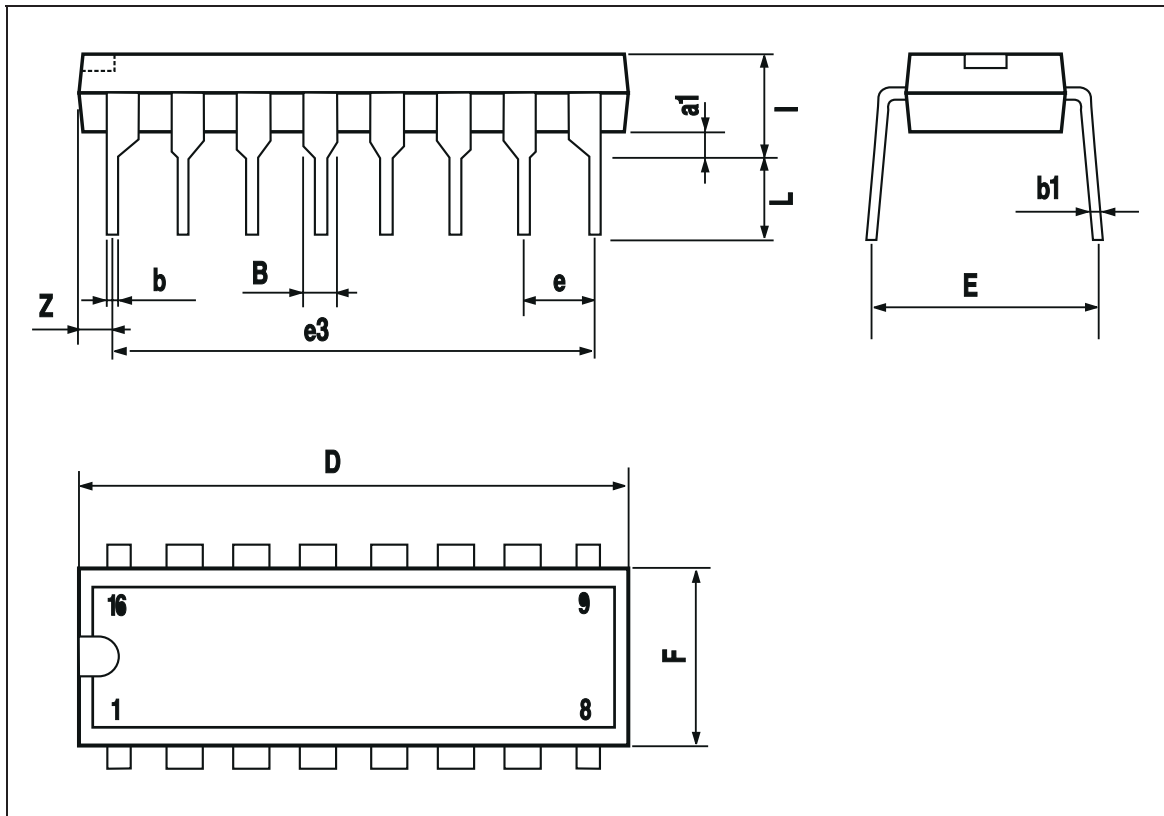
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Dim.	mm			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	0.85		1.40	0.033		0.055
b		0.50			0.020	
b1	0.38		0.50	0.015		0.020
D			20.0			0.787
E		8.80			0.346	
e		2.54			0.100	
e3		17.78			0.700	
F			7.10			0.280
I			5.10			0.201
L		3.30			0.130	
Z			1.27			0.050

OUTLINE AND MECHANICAL DATA



PowerDIP-16



9 Revision history

Table 4. Document revision history

Date	Revision	Changes
12-Sep-2003	1	First release
22-Jan-2009	2	Modified Table 1 on page 1 .

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