PEX 8606

**PCIe Gen2, 5.0 GT/s 6-lane 6-port PCI Express® Switch**

The ExpressLane™ PEX 8606 device offers PCI Express switching capability enabling users to add scalable high bandwidth non-blocking interconnection to a wide variety of applications including communications platforms, control plane applications and embedded systems. The PEX 8606 is well suited for fan-out, aggregation, peer-to-peer, and intelligent I/O module applications.

**Low Packet Latency & High Performance**

The PEX 8606 architecture supports packet cut-thru with a maximum latency of 190ns in x1 to x1 configuration. This, combined with large packet memory and non-blocking internal switch architecture, provides full line rate on all ports for low-latency applications such as communications and embedded. The low latency enables applications to achieve high throughput and performance. In addition to low latency, the device supports a max payload size of 2048 bytes, enabling the user to achieve even higher throughput.

**Data Integrity**

The PEX 8606 provides end-to-end CRC protection (ECRC) and Poison bit support to enable designs that require guaranteed error-free packets. PLX also supports data path parity and memory (RAM) error correction as packets pass through the switch.

**Dual-Host and Fail-Over Support**

The PEX 8606 supports full non-transparent bridging (NTB) functionality to allow implementation of multi-host systems and intelligent I/O modules in applications which require redundancy support such as communications, storage, and servers.

Non-transparent bridges allow systems to isolate host memory domains by presenting the processor subsystem as an endpoint rather than another memory system. Base address registers are used to translate addresses; doorbell registers are used to send interrupts between the address domains; and scratchpad registers are accessible from both address domains to allow inter-processor communication.

**Interoperability**

The PEX 8606 is designed to be fully compliant with the PCI Express Base Specification r2.0 and is backwards compatible to PCI Express Base Specification r1.1 and r1.0a. Additionally each port supports auto-negotiation, lane reversal and polarity reversal. Furthermore, the PEX 8606 is designed for Microsoft Vista compliance. All PLX switches undergo thorough interoperability testing in PLX’s Interoperability Lab and compliance testing at the PCI-SIG plug-fest to ensure compatibility with PCI Express devices in the market.

**Device Operation Configuration Flexibility**

The PEX 8606 provides several ways to configure its operations. The device can be configured through strapping pins, I²C interface, CPU configuration cycles and/or an optional serial EEPROM. This allows for easy debug during the development phase and functional monitoring during the operation phase.

Features

- **PEX 8606 General Features**
  - 6-lane PCI Express switch
  - Integrated 5.0 GT/s SerDes
  - Up to 6 configurable ports
  - 15 x 15mm², 196-ball PBGA
  - Typical Power: 1.34 Watts

- **PEX 8606 Key Features**
  - **Standards Compliant**
    - PCI Express Base Specification r2.0 (Backwards compatible with PCIe r1.0a/1.1)
    - PCI Power Management Spec r1.2
    - Microsoft Vista Compliant
    - Supports Access Control Services
    - Dynamic link-width control
    - Dynamic SerDes Speed Control
  - **High Performance**
    - Non-blocking internal architecture
    - Full line rate on all ports
    - Cut-Thru latency: 190ns
    - 2KB max payload size
    - Read Pacing
    - (intelligent bandwidth allocation)
    - Dual Cast
  - **Dual-Host & Fail-Over Support**
    - Configurable Non-Transparent port
    - Moveable upstream port
    - Crosslink port capability
  - **Flexible Configuration**
    - 6 flexible & configurable ports
      - (x1 or x2)
    - Configurable with strapping pins, EEPROM, I²C, or Host software
    - Lane and polarity reversal
  - **PCI Express Power Management**
    - Link power management states: L0, L0s, L1, L2/L3 Ready, and L3
    - Device states: D0 and D3\text{hot}
  - **Spread Spectrum Clock Isolation**
    - Two Virtual Channels (VC) per port
    - Eight Traffic Classes per port
    - Weighted Round-Robin Port & VC Arbitration
  - **Reliability, Availability, Serviceability**
    - All ports Hot-Plug capable thru I²C
      - (Hot-Plug Controller on every port)
    - ECRC & Poison bit support
    - Data path protection
    - Memory (RAM) error correction
    - Advanced Error Reporting support
    - Port Status bits and GPIO available
    - Per port error diagnostics
    - Performance monitoring
      - (per port payload & header counters)
    - JTAG AC/DC boundary scan
    - Fatal Error (FATAL_ERR#) output signal
    - INTA\# output signal
  - **Interoperability**
    - Presenting the processor subsystem as an endpoint rather than another memory system
    - Base address registers are used to translate addresses; doorbell registers are used to send interrupts between the address domains; and scratchpad registers are accessible from both address domains to allow inter-processor communication.
  - **Device Operation Configuration Flexibility**
    - The PEX 8606 provides several ways to configure its operations. The device can be configured through strapping pins, I²C interface, CPU configuration cycles and/or an optional serial EEPROM. This allows for easy debug during the development phase and functional monitoring during the operation phase.
Flexible Port Configurations
The PEX 8606 supports the port configurations as shown in figure 1 below. The figure shows a 6-port configuration and a 5-port configuration.

![Figure 1. Port Configurations](image)

Hot-Plug for High Availability
Hot-Plug capability allows users to replace hardware modules and perform maintenance without powering down the system. The PEX 8606 Hot-Plug capability feature makes it suitable for High Availability (HA) applications. If the PEX 8606 is used in an application where one or more of its downstream ports connect to PCI Express slots, each port’s Hot-Plug Controller can be used to manage the Hot-Plug event of its associated slot. Every port on the PEX 8606 is equipped with a Hot-Plug control/status register to support Hot-Plug capability through external logic via the I²C interface.

Dual Cast
The PEX 8606 supports Dual Cast, a feature which allows for the copying of data (e.g. packets) from one ingress port to two egress ports allowing for higher performance in storage, security, and mirroring applications.

Read Pacing
The Read Pacing feature allows users to throttle the amount of read requests being made by downstream devices. In the case where a downstream device requests several long reads back-to-back, the Root Complex gets tied up in serving this downstream port. If this port has a narrow link and is therefore slow in receiving these read packets from the Root Complex, then other downstream ports may become starved — thus, impacting performance. The Read Pacing feature enhances performances by allowing for the adequate servicing of all downstream devices by intelligent handling of read requests.

SerDes Power and Signal Management
The PEX 8606 provides low power capability that is fully compliant with the PCI Express power management specification. In addition, the SerDes physical links can be turned off when unused for even lower power. The PEX 8606 supports software control of the SerDes outputs to allow optimization of power and signal strength in a system. The PLX SerDes implementation supports four levels of power — off, low, typical, and high. The SerDes block also supports loop-back modes and advanced reporting of error conditions, which enables efficient debug and management of the entire system.

Port and Virtual Channel (VC) Arbitration
The PEX 8606 switch supports hardware fixed and Weighted Round-Robin (WRR) Ingress Port Arbitration. This allows fine tuning of Quality of Service and efficient use of packet buffers for better system performance. The PEX 8606 also supports WRR VC arbitration scheme between the two virtual channels.

Applications
Suitable for fan-out, control plane applications, embedded systems as well as intelligent I/O and host isolation applications, PEX 8606 can be configured for a wide variety of form factors and applications.

Fan-Out
The PEX 8606 switch, with its high port count and flexible configurations, allows user specific tuning to a variety of host-centric as well as peer-to-peer applications.

SerDes Power and Signal Management
The PEX 8606 provides low power capability that is fully compliant with the PCI Express power management specification. In addition, the SerDes physical links can be turned off when unused for even lower power. The PEX 8606 supports software control of the SerDes outputs to allow optimization of power and signal strength in a system. The PLX SerDes implementation supports four levels of power – off, low, typical, and high. The SerDes block also supports loop-back modes and advanced reporting of error conditions, which enables efficient debug and management of the entire system.

Port and Virtual Channel (VC) Arbitration
The PEX 8606 switch supports hardware fixed and Weighted Round-Robin (WRR) Ingress Port Arbitration. This allows fine tuning of Quality of Service and efficient use of packet buffers for better system performance. The PEX 8606 also supports WRR VC arbitration scheme between the two virtual channels.

Applications
Suitable for fan-out, control plane applications, embedded systems as well as intelligent I/O and host isolation applications, PEX 8606 can be configured for a wide variety of form factors and applications.

Fan-Out
The PEX 8606 switch, with its high port count and flexible configurations, allows user specific tuning to a variety of host-centric as well as peer-to-peer applications.

SerDes Power and Signal Management
The PEX 8606 provides low power capability that is fully compliant with the PCI Express power management specification. In addition, the SerDes physical links can be turned off when unused for even lower power. The PEX 8606 supports software control of the SerDes outputs to allow optimization of power and signal strength in a system. The PLX SerDes implementation supports four levels of power – off, low, typical, and high. The SerDes block also supports loop-back modes and advanced reporting of error conditions, which enables efficient debug and management of the entire system.

Port and Virtual Channel (VC) Arbitration
The PEX 8606 switch supports hardware fixed and Weighted Round-Robin (WRR) Ingress Port Arbitration. This allows fine tuning of Quality of Service and efficient use of packet buffers for better system performance. The PEX 8606 also supports WRR VC arbitration scheme between the two virtual channels.

Applications
Suitable for fan-out, control plane applications, embedded systems as well as intelligent I/O and host isolation applications, PEX 8606 can be configured for a wide variety of form factors and applications.

Fan-Out
The PEX 8606 switch, with its high port count and flexible configurations, allows user specific tuning to a variety of host-centric as well as peer-to-peer applications.
Docking Station Application
The PEX 8606 is ideal for IO expansion applications. The support for SSC isolation as well as its low power consumption makes it an ideal candidate for peripheral expansion. Figure 3 below shows a block diagram for a docking station. With PCI Express slots, the IO subsystem can be expanded in order to extend the peripheral capabilities of a notebook PC.

![Figure 3. Docking Station](image)

Control Planes for Large Systems
Control for larger systems can be accomplished with a bigger switch. However, in many cases where multiple PCIe ports are available on the CPU, multiple switches can be used in order to balance the traffic as shown in Figure 4.

![Figure 4. Control Planes for Large Systems](image)

Embedded Control Planes
The PEX 8606 is well suited for embedded control plane applications. An example of such application is a packet processing module, as shown in Figure 5. In this example, the FPGAs and ASICs implement an x1 PCI Express Interface. With its high port count, the PEX 8606 can provide connectivity to a high number of FPGAs and ASICs for a robust packet processing communications sub-system.

![Figure 5. Packet Processing Module](image)

Intelligent Adapter Card
The PEX 8606 supports the non-transparency feature. Figure 6 illustrates a host system using an intelligent adapter card.

![Figure 6. Intelligent Adapter Usage](image)

Active-Standby Failover Model
The PEX 8606 supports applications requiring dual host, host failover applications through the non-transparency feature. Figure 7 illustrates a dual host system with an active and standby processor configuration.

The redundancy of the host and the fabric can be achieved through many possible configurations using NTB function of PEX 8606. In the configuration shown below Processor A is the primary active host of the PCI Express system. Processor B acts as the backup Host. In the case of a failure on Processor A, application software is instructed to migrate the PCI Express system to Processor B. Consequently, Processor B becomes the active host and Processor A can be replaced as the backup Host.

![Figure 7. Active-Standby Host Mode](image)
Software Usage Model
From a system model viewpoint, each PCI Express port is a virtual PCI to PCI bridge device and has its own set of PCI Express configuration registers. It is through the upstream port that the BIOS or host can configure the other ports using standard PCI enumeration. The virtual PCI-to-PCI bridges within the PEX 8606 are compliant to the PCI and PCI Express system models. The Configuration Space Registers (CSRs) in a virtual primary/secondary PCI-to-PCI bridge are accessible by type 0 configuration cycles through the virtual primary bus interface (matching bus number, device number, and function number).

Development Tools
PLX offers hardware and software tools to enable rapid customer design activity. These tools consist of a PEX 8606 Rapid Development Kit (RDK), hardware documentation, and a Software Development Kit (also available at www.plxtech.com/sdk).

Interrupt Sources/Events
The PEX 8606 supports the INTx interrupt message type (compatible with PCI 2.3 Interrupt signals) or Message Signaled Interrupts (MSI) when enabled. Interrupts/messages are generated by PEX 8606 for Hot-Plug events, doorbell interrupts, baseline error reporting, and advanced error reporting.

RDK
The PEX 8606RDK is a hardware module containing the PEX 8606 which plugs right into your system (Figure 8). The PEX 8606RDK hardware module can be installed in a motherboard, used as a riser card, or configured as a bench-top board. The PEX 8606RDK can be used to test and validate customer software. Additionally, it can be used as an evaluation vehicle for PEX 8606 features and benefits.

SDK
The SDK tool set includes:
- Linux & Windows drivers
- C/C++ Source code, Objects, libraries
- User’s Guides & Application examples

Figure 8. PEX 8606RDK

Product Ordering Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PEX8606-BA50BC</td>
<td>6 Lane, 6 Port PCIe Switch, 196-ball PBGA 15x15mm² pkg</td>
</tr>
<tr>
<td>PEX8606-BA50BC G</td>
<td>6 Lane, 6 Port PCIe Switch, 196-ball PBGA 15x15mm² pkg, Pb-free</td>
</tr>
<tr>
<td>PEX8606-BA50BI G</td>
<td>6 Lane, 6 Port PCIe Switch, 196-ball PBGA 15x15mm² pkg, Pb-free Industrial Temperature</td>
</tr>
<tr>
<td>PEX 8606bA-AIC1U1D RDK</td>
<td>PEX 8606 Rapid Development Kit</td>
</tr>
</tbody>
</table>

Please visit the PLX Web site at http://www.plxtech.com or contact PLX sales at 408-774-9060 for sampling.
Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Avago Technologies:
PEX8606-BA50BIG  PEX8606BA-AIC1U1DRDK  PEX 8606-BA50BC  PEX 8606-BA50BC G  PEX 8606BA-AIC1U1D RDK  PEX8606-BA50BC  PEX8606-BA50BC G  PEX8606-BA50BI G