


**SANYO Semiconductors**

# DATA SHEET

## LB11851TT — Monolithic Digital IC Microprocessor Fan Motor Interface Driver

### Overview

The LB11851TT provides an interface between a microcontroller motor control signal and external MOS transistors. This device can implement a microprocessor fan driver with a minimal number of external components. The LB11851TT is optimal for server and personal computer microprocessor fan drive in response to temperature or other external signals when high precision and high air flow are required.

### Features

- Fan motor interface driver function (FGIN)  
⇒ This IC accepts a signal from a microcontroller and interfaces to external power transistors (PMOS and NMOS) to provide high-efficiency low-power single-phase full-wave drive.
- Variable speed input pin (PWMIN)  
⇒ PMOS side PWM control  
NMOS side current regeneration using slow decay is used to achieve quite high-speed control.
- Built-in kickback absorption circuit (OUT1P/2P)  
⇒ This circuit absorbs the kickback current that is generated at phase switching or power on/off to achieve smooth current regeneration and protect the external transistors against destruction or degradation.
- Built-in current limiter circuit (SENSE)  
⇒ This circuit implements a chopper-type current limiting control that operates at startup and during lock protection mode.  
The current detection voltage is set to a fixed 0.2V internally.
- Built-in microcontroller power supply (5VREG)

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## Specifications

### Allowable Operating Ranges at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC}$ max		18	V
OUTN pin maximum output current	IOUTN max		20	mA
OUTP pin maximum output current	IOUTP max		20	mA
OUT pin voltage handling capacity	VOUT max		18	V
5VREG maximum output current	I5VREG max		20	mA
Allowable power dissipation	$P_d$ max	When mounted on the specified circuit board *1	400	mW
Operating temperature	$T_{opr}$	*2	-40 to +90	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-55 to +150	$^\circ\text{C}$

\*1 Specified substrate :20.0mm x10.0mm x0.8mm, Paper phenol board.

\*2 Do not exceed  $T_j$  max =  $150^\circ\text{C}$

### Recommended Operating Ranges at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage - $V_{CC}$	$V_{CC}$		6 to 16	V
PWM high-level input voltage range	VPWMINH		2.1 to 5.0	V
PWM low-level input voltage range	VPWMINL		0 to 0.4	V
FGIN high-level input voltage range	VFGINH		2.1 to 5.0	V
FGIN low-level input voltage range	VFGINL		0 to 0.3	V
SENSE input voltage range	VSENop		0 to 5.0	V

### Electrical Characteristics at $T_a = 25^\circ\text{C}$ , $V_{DD} = 12\text{V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Circuit current	$I_{CC1}$	With no load	3.5	5	6.5	mA
5VREG voltage	5VREG	5VREG = 10mA	4.8	5	5.2	V
SENSE pin detection voltage	VSENth		0.15	0.19	0.23	V
FGIN high-level input current	FGIhi	$V_{IN} = 3\text{V}$	60	80	100	$\mu\text{A}$
FGIN low-level input current	FGIlow	$V_{IN} = 0\text{V}$	-27	-21	-15	$\mu\text{A}$
PWMIN high-level current	PWMIhi	$V_{IN} = 3\text{V}$	35	45	55	$\mu\text{A}$
PWMIN low-level current	PWMIlow	$V_{IN} = 0\text{V}$	-27	-21	-14	$\mu\text{A}$
OUT1P, OUT2P high-level output voltage	$V_{O12PH}$	$I_O = 10\text{mA} \times 2$	10	11	11.9	V
		$I_O = 1\text{mA} \times 2$	11	11.3		V
OUT1P, OUT2P low-level output voltage	$V_{O12PL}$	$I_O = 10\text{mA} \times 2$	3	4	5	V
		$I_O = 1\text{mA} \times 2$		1.2	1.5	V
OUT1N, OUT2N high-level output voltage	$V_{O12NH}$	$I_O = 10\text{mA} \times 1$	9	10	11.9	V
		$I_O = 1\text{mA} \times 1$	10.8	11.1		V
OUT1N, OUT2N low-level output voltage	$V_{O12NL}$	$I_O = 10\text{mA} \times 1$	0.1	1	2	V
		$I_O = 1\text{mA} \times 1$		0.7	1	V

\*1 : There is a built-in 100 $\Omega$  gate protection resistor.

\*2 : There is a built-in 300 $\Omega$  gate protection resistor.

## Truth Table

FGIN	PWMIN	SENSE	OUT1P	OUT1N	OUT2P	OUT2N	Mode
L	L	L	L	L	H	H	OUT1 $\rightarrow$ 2 drive
H			H	H	L	L	OUT2 $\rightarrow$ 1 drive
L	H	L	H	L	H	H	Regeneration mode (low side regeneration)
H			H	H	H	L	
L	L	H	H	L	H	H	Current limiter (low side regeneration)
H			H	H	H	L	

Note 1 : For the SENSE pin, the "H" state is 0.2V or higher.

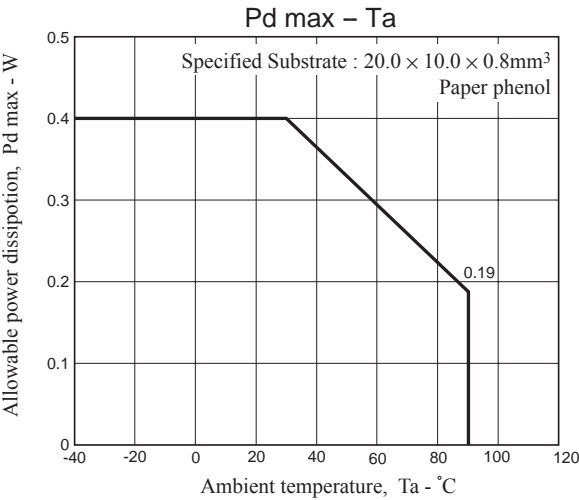
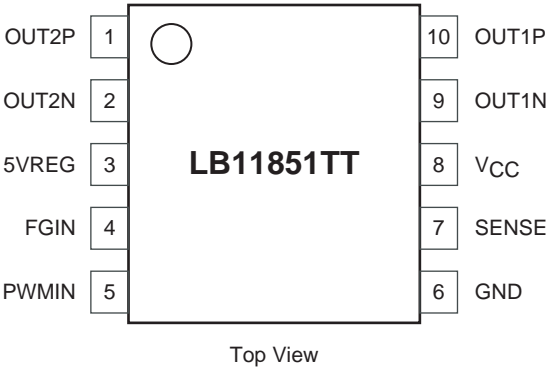
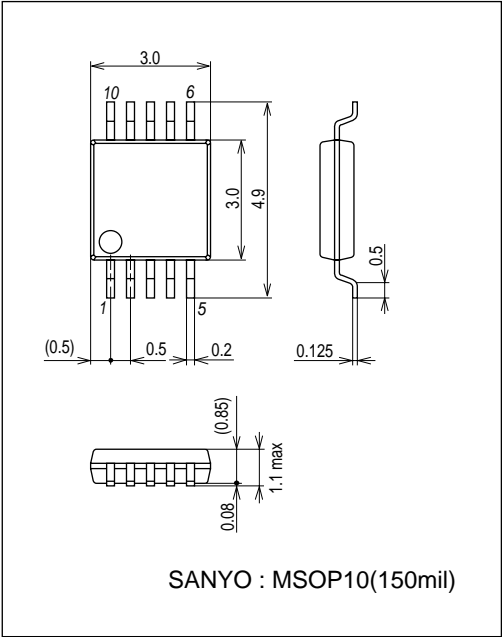
Note 2 : The IC goes to regeneration mode (no motor drive applied) when the microcontroller is reset (the output high-impedance state).

## Package Dimensions

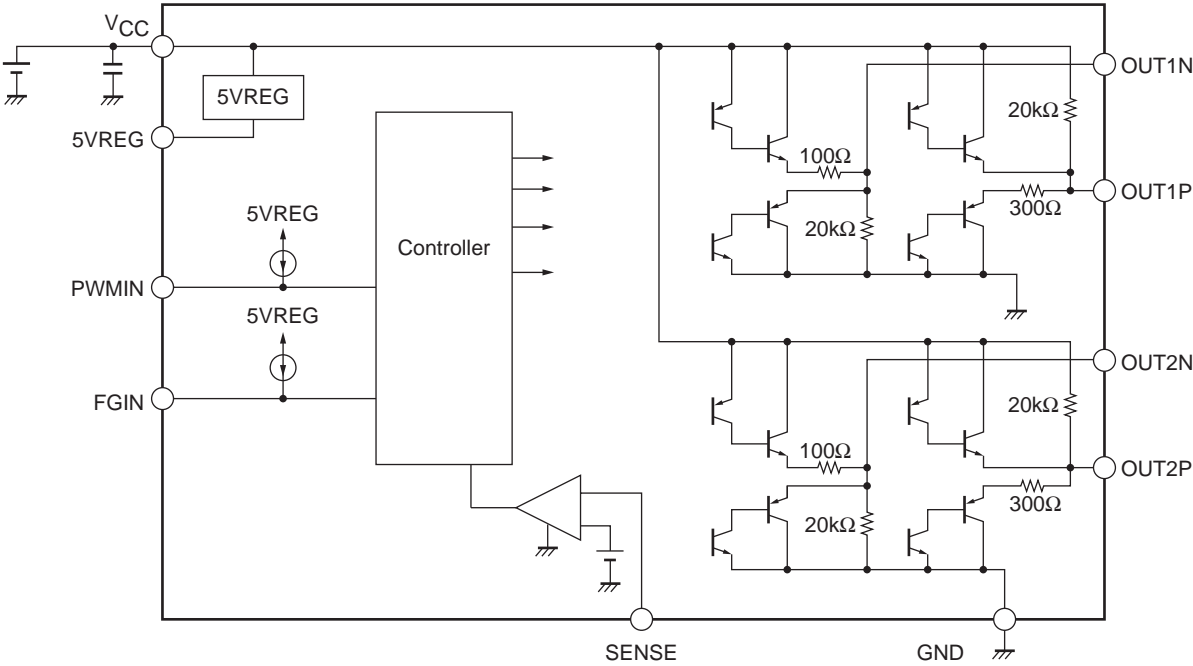
## Pin Assignment

LB11851TT

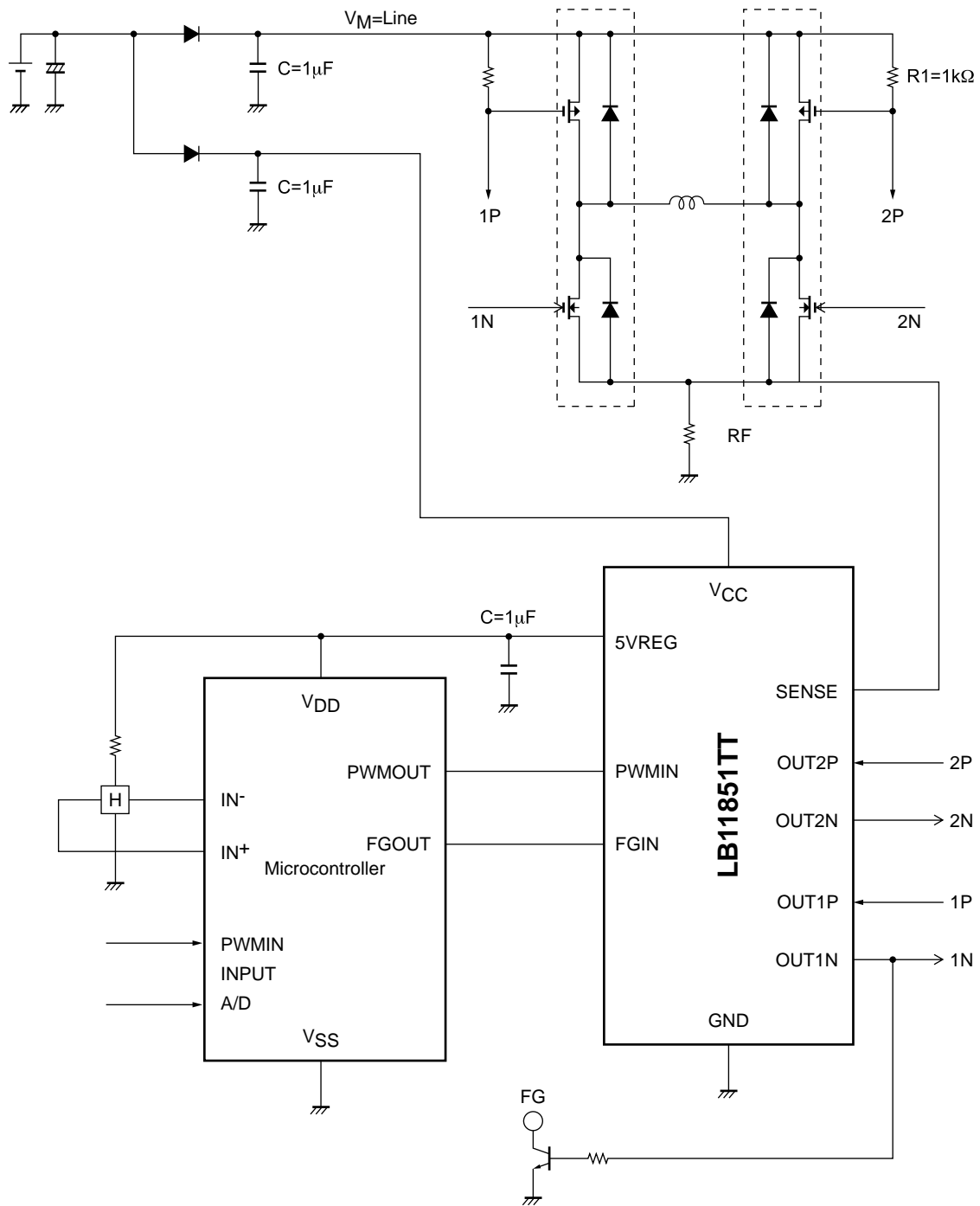
unit : mm (typ)  
3297



Block Diagram



## Application Circuit Example (12V)



## 1. Power supply ( $V_{CC}$ and $V_M$ ) and ground

The wiring is separated into the control IC side ( $V_{CC}$  line) and the motor output side ( $V_M$  line) by the diode DI, which protects the IC from destruction on reverse connection. The application circuit uses  $1\mu\text{F}$  capacitors to prevent line oscillation when kickback occurs. Similarly,  $1\mu\text{F}$  capacitors are also used on the  $V_{CC}$  line for power supply line stabilization.

## 2. PWMIN

The LB11851M accepts an open-drain output signal from the microcontroller with this pin and controls the on/off states of the PMOS transistor (OUT1P and OUT2P) outputs accordingly. A constant-current bias is provided from 5VREG internally to the IC.

## 3. FGIN

The LB11851M accepts a CMOS output from the microcontroller with this pin and determines the drive phase output (OUT1P, OUT2P, OUT1N, or OUT2N).

## 4. 5VREG

This is the power supply for the microcontroller, Hall effect sensors, and other circuits. A capacitor with a value of  $1\mu\text{F}$  is used for output stabilization. This pin has an output current capacity of 20mA.

## 5. SENSE

A sensing resistor is used for current detection. If the SENSE pin voltage exceeds 0.2V, the PMOS transistors are turned off and only low side regeneration is performed.

\*<OUT1, 2P output H voltage / OUT1, 2N output L voltage>

Output L voltage of OUT1 and 2 sticks in GND when FET is put up outside like the example of applied circuit by internal pull-down resistor ( $20\text{k}\Omega$ ), and there is no what turns on FET.

Output H voltage of OUT1 and 2 sticks in VCC with internal pull-up resistor ( $20\text{k}\Omega$ ) as the Pch side is also similar.

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