

PSMN4R4-80PS

N-channel 80 V, 4.1 mΩ standard level FET

Rev. 01 — 18 June 2009

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Suitable for standard level gate drive sources

1.3 Applications

- DC - DC converters
- Motor control
- Load switch
- Server power supplies

1.4 Quick reference data

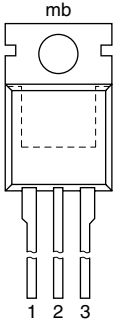
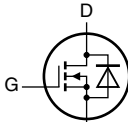
Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1 ; see Figure 3	-	-	100	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	306	W
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}$; $I_D = 80\text{ A}$; $V_{DS} = 40\text{ V}$; see Figure 14 ; see Figure 15	-	25	-	nC
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 15\text{ A}$; $T_j = 25\text{ °C}$; see Figure 6 ; see Figure 13	[1]	-	3.3	4.1 mΩ

[1] Measured 3 mm from package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	drain		

SOT78
(TO-220AB; SC-46)

3. Ordering information

Table 3. Ordering information

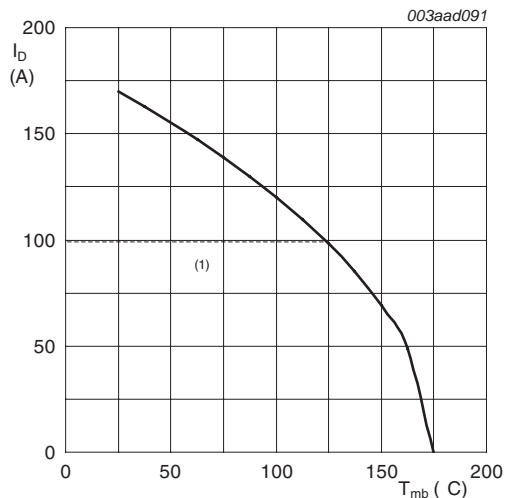
Type number	Package		Version
	Name	Description	
PSMN4R4-80PS	TO-220AB; SC-46	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78

4. Limiting values

Table 4. Limiting values

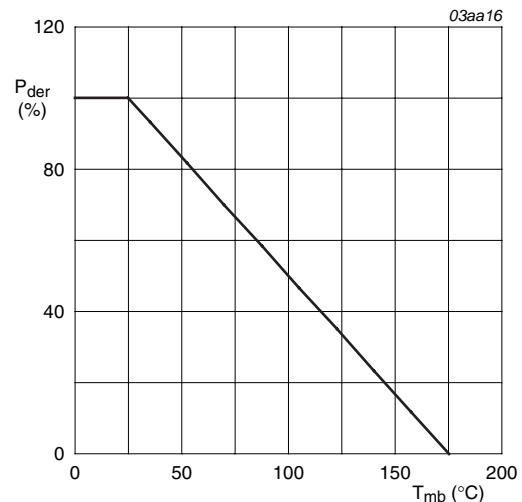
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	80	V
V _{DGR}	drain-gate voltage	T _j ≥ 25 °C; T _j ≤ 175 °C; R _{GS} = 20 kΩ	-	80	V
V _{GS}	gate-source voltage		-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 100 °C; see Figure 1 ; see Figure 3	-	100	A
		V _{GS} = 10 V; T _{mb} = 25 °C; see Figure 1 ; see Figure 3	-	100	A
I _{DM}	peak drain current	t _p ≤ 10 μs; pulsed; T _{mb} = 25 °C; see Figure 3	-	680	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	306	W
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
Source-drain diode					
I _S	source current	T _{mb} = 25 °C	-	100	A
I _{SM}	peak source current	t _p ≤ 10 μs; pulsed; T _{mb} = 25 °C	-	680	A
Avalanche ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 100 A; V _{sup} ≤ 80 V; R _{GS} = 50 Ω; unclamped	-	591	mJ



$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature

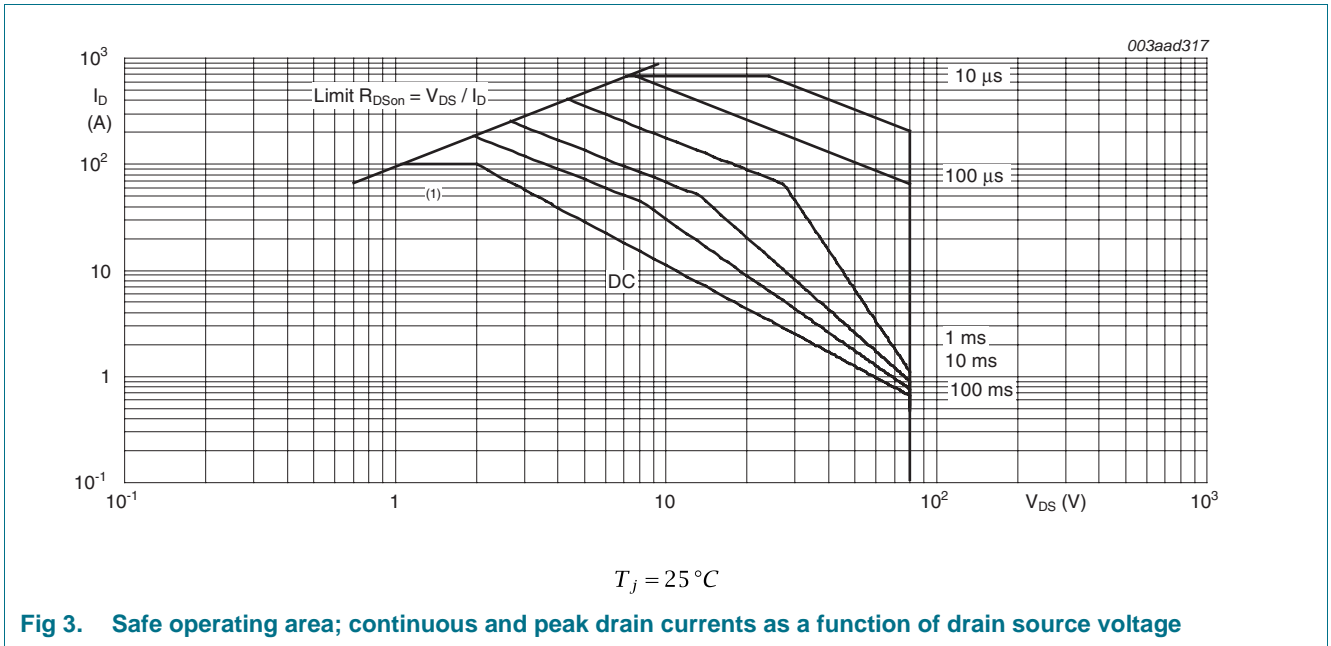


Fig 3. Safe operating area; continuous and peak drain currents as a function of drain source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	0.23	0.49	K/W

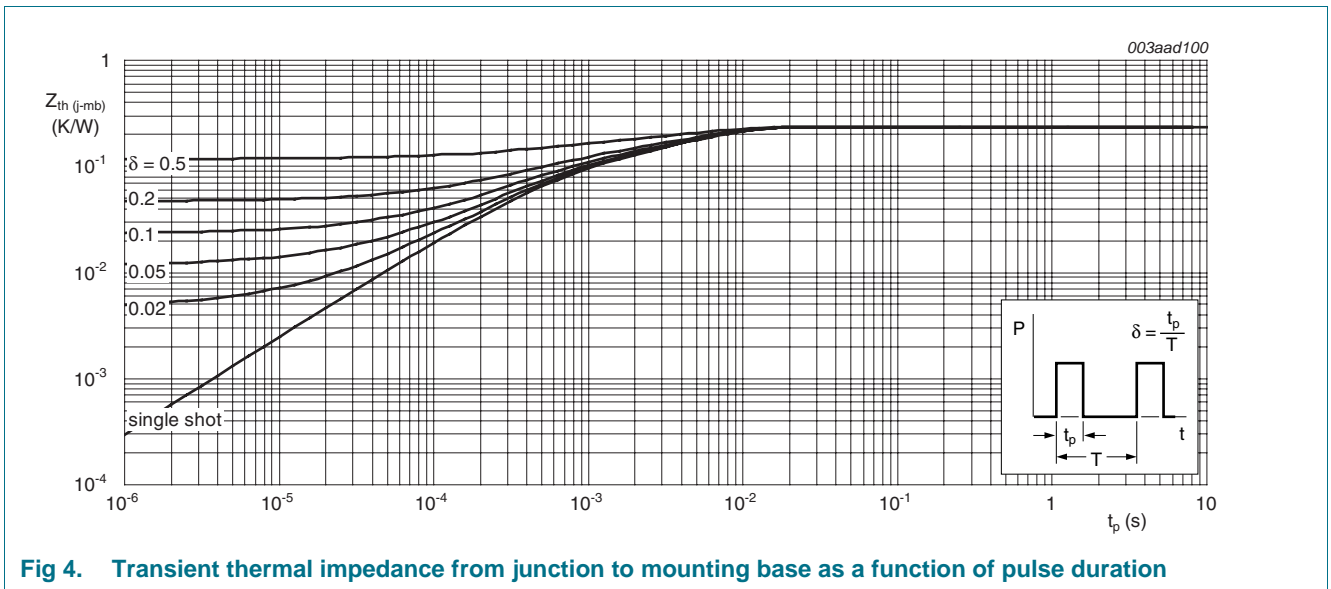


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	73	-	-	V	
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	80	-	-	V	
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ see Figure 11	1	-	-	V	
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see Figure 11	-	-	4.6	V	
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 11 ; see Figure 12	2	3	4	V	
I_{DSS}	drain leakage current	$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	10	μA	
		$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ\text{C}$	-	-	200	μA	
I_{GSS}	gate leakage current	$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA	
		$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA	
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ see Figure 13	[2]	-	7.6	9.47	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 100 \text{ }^\circ\text{C};$ see Figure 13	-	5.5	6.8	mΩ	
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 6 ; see Figure 13	[2]	-	3.3	4.1	mΩ
R_G	internal gate resistance (AC)	$f = 1 \text{ MHz}$	-	1	-	Ω	
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	112	-	nC	
		$I_D = 80 \text{ A}; V_{DS} = 40 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 14 ; see Figure 15	-	125	-	nC	
Q_{GS}	gate-source charge	$I_D = 80 \text{ A}; V_{DS} = 40 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 14 ; see Figure 15	-	39	-	nC	
$Q_{GS(th)}$	pre-threshold gate-source charge		-	24	-	nC	
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	15	-	nC	
Q_{GD}	gate-drain charge		-	25	-	nC	
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}; V_{DS} = 40 \text{ V};$ see Figure 14 ; see Figure 15	-	4.65	-	V	
C_{iss}	input capacitance	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see Figure 16	-	8400	-	pF	
C_{oss}	output capacitance		-	700	-	pF	
C_{rss}	reverse transfer capacitance		-	336	-	pF	
$t_{d(on)}$	turn-on delay time	$V_{DS} = 40 \text{ V}; R_L = 0.5 \text{ } \Omega; V_{GS} = 10 \text{ V};$ $R_{G(ext)} = 1.5 \text{ } \Omega$	-	34.7	-	ns	
t_r	rise time		-	38.1	-	ns	
$t_{d(off)}$	turn-off delay time		-	66	-	ns	
t_f	fall time		-	18.4	-	ns	

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; see Figure 17	-	0.8	1.2	V
t_{rr}	reverse recovery time	$I_S = 25\text{ A}$; $di_S/dt = 100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$;	-	59	-	ns
Q_r	recovered charge	$V_{DS} = 20\text{ V}$	-	130	-	nC

- [1] Tested to JEDEC standards where applicable.
- [2] Measured 3 mm from package.

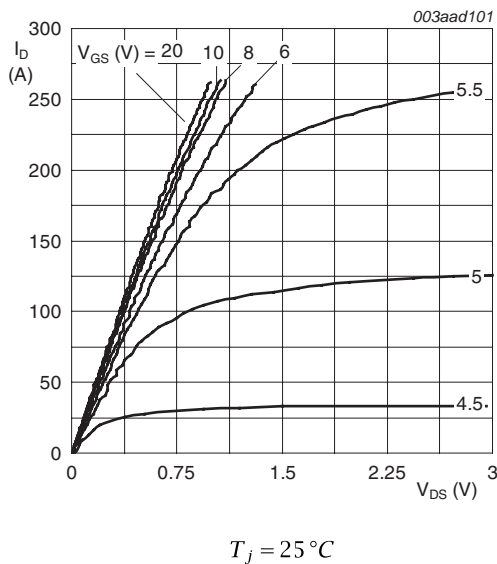


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

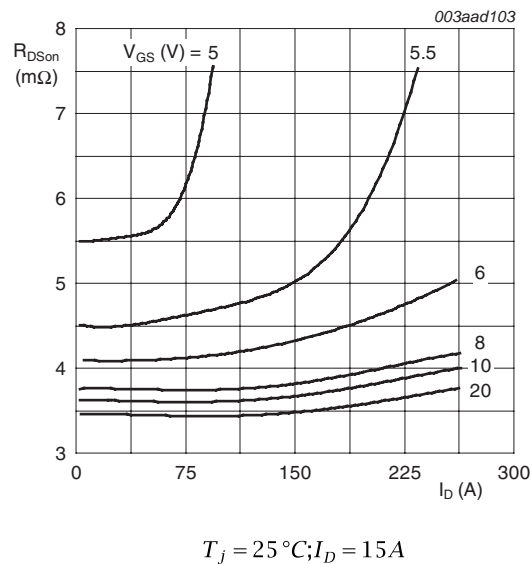


Fig 6. Drain-source on-state resistance as a function of drain current; typical values

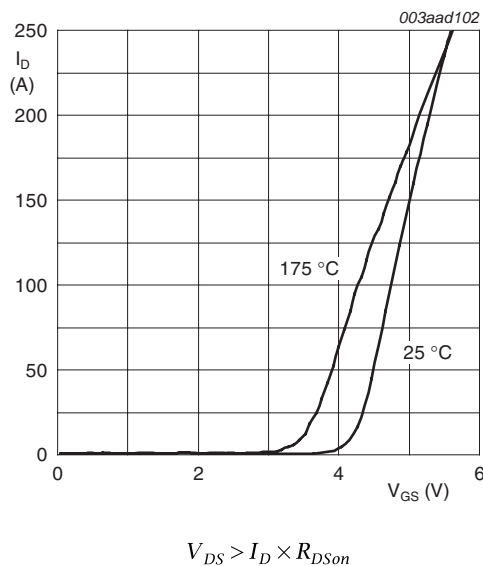


Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values

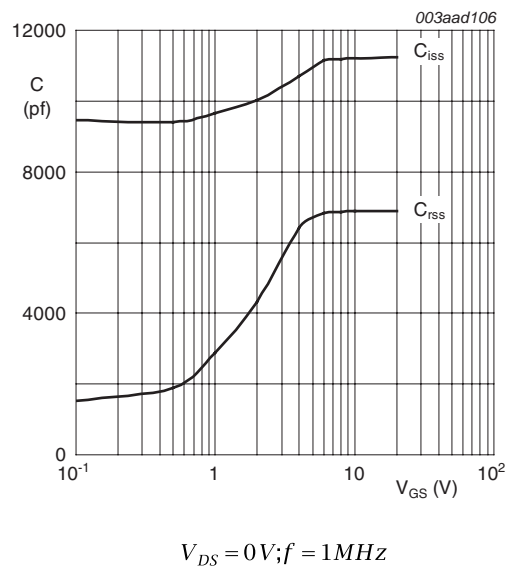
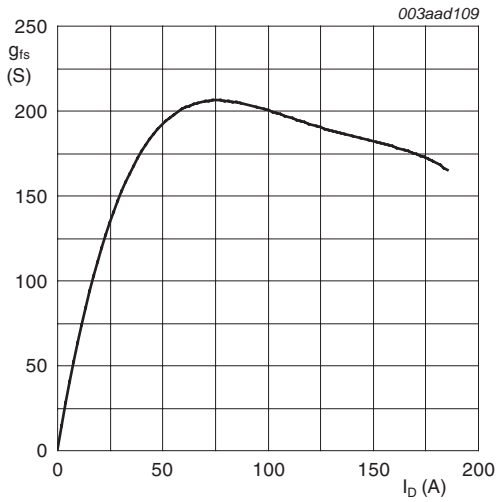
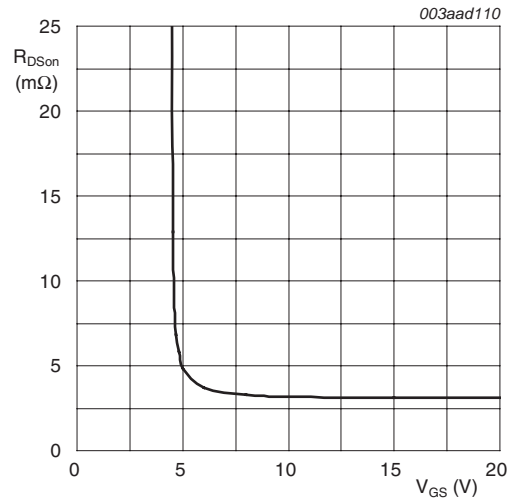


Fig 8. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



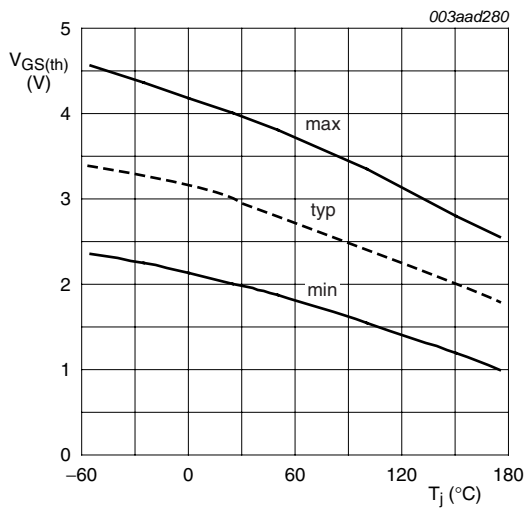
$T_j = 25^\circ\text{C}; V_{DS} = 25\text{V}$

Fig 9. Forward transconductance as a function of drain current; typical values



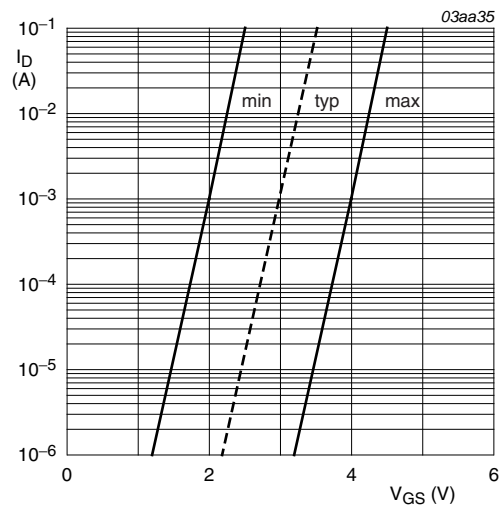
$T_j = 25^\circ\text{C}; I_D = 15\text{A}$

Fig 10. Drain-source on-state resistance as a function of gate-source voltage; typical values



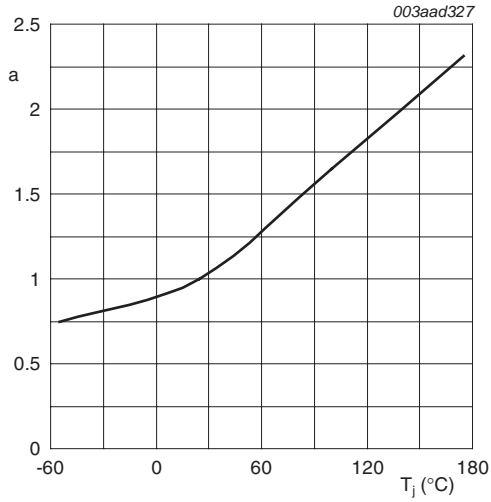
$I_D = 1\text{mA}; V_{DS} = V_{GS}$

Fig 11. Gate-source threshold voltage as a function of junction temperature



$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$

Fig 12. Sub-threshold drain current as a function of gate-source voltage



$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

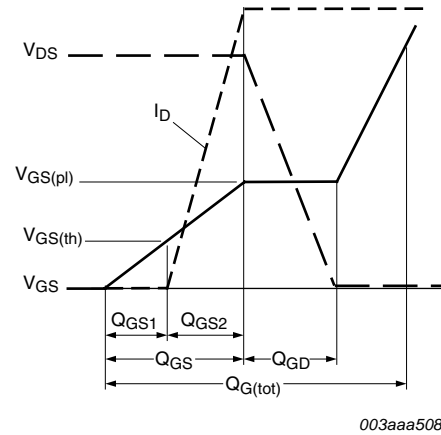
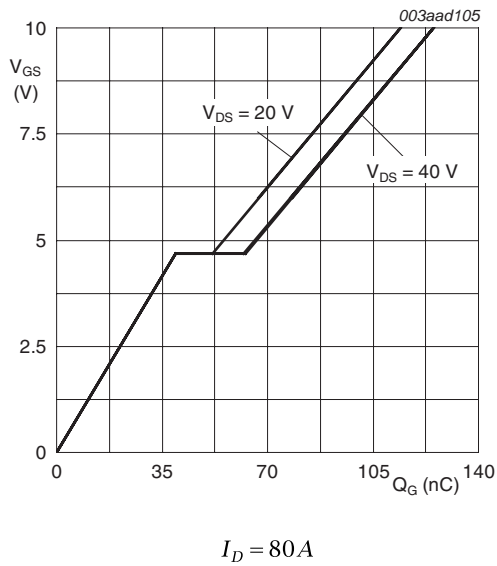
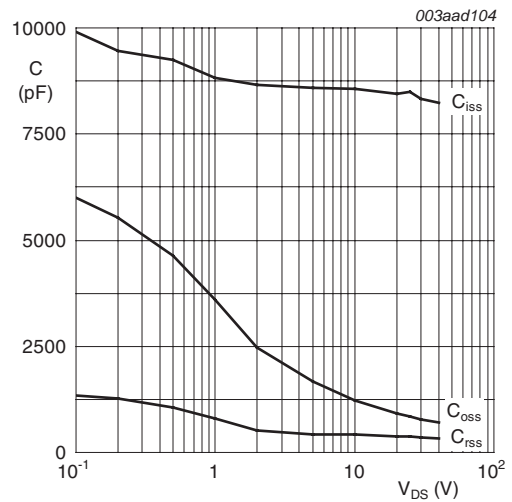


Fig 14. Gate charge waveform definitions



$I_D = 80 A$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0 V; f = 1 MHz$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

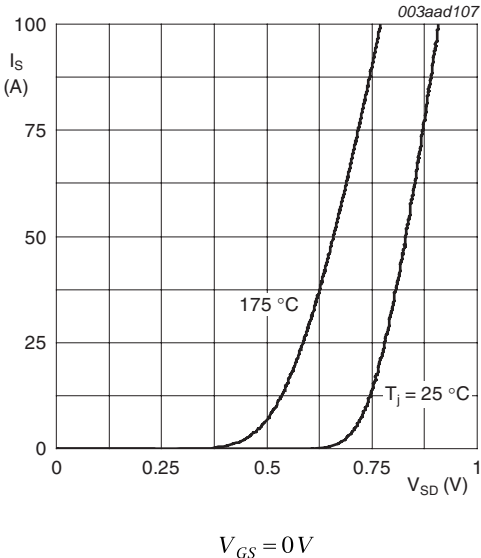


Fig 17. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78

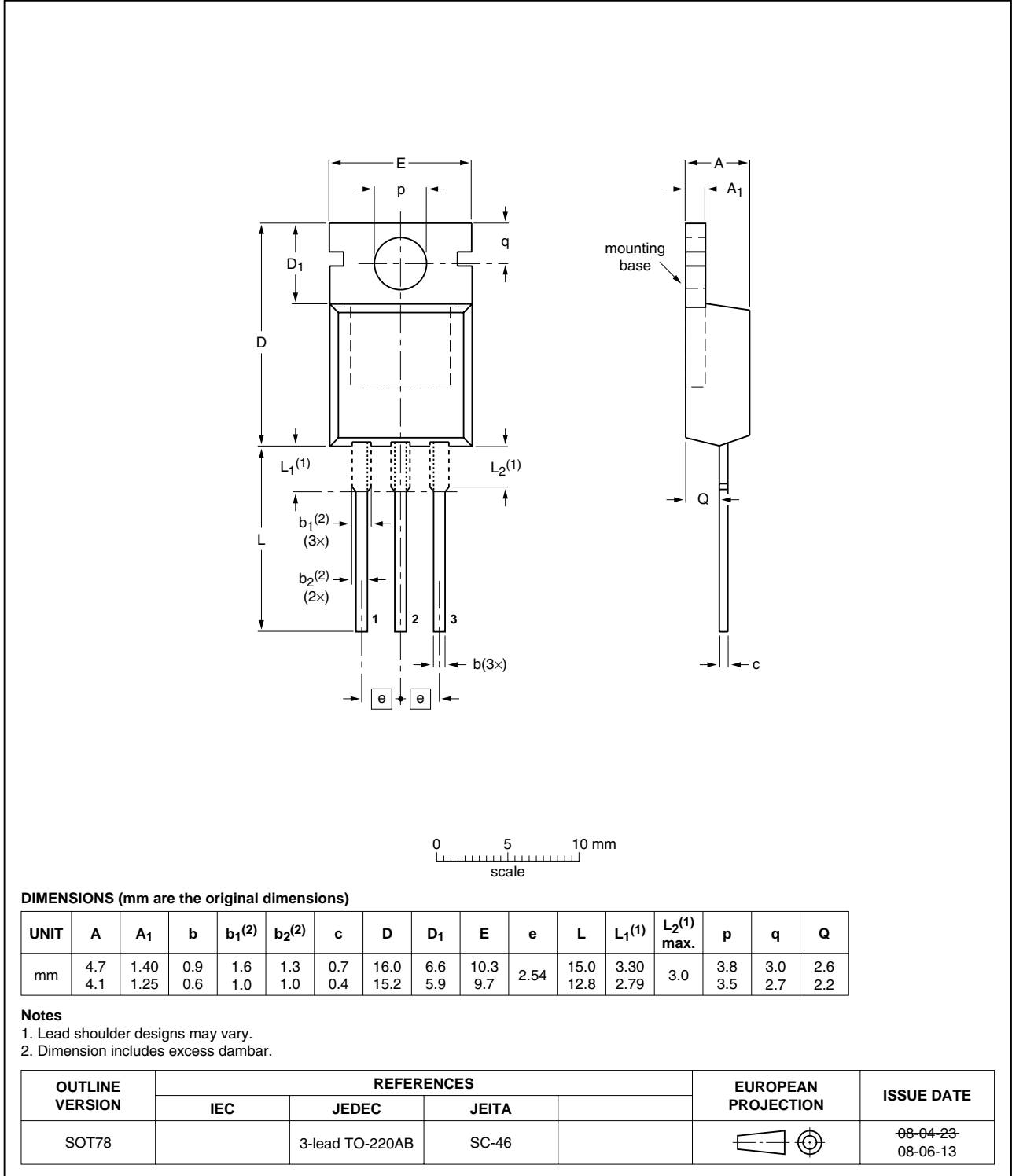


Fig 18. Package outline SOT78 (TO-220AB)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN4R4-80PS_1	20090618	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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