Document Number: AFT09H310–03S
Rev. 1, 9/2013

RoHS

RF Power LDMOS Transistors

N–Channel Enhancement–Mode Lateral MOSFETs

These 56 watt asymmetrical Doherty RF power LDMOS transistors are designed for cellular base station applications covering the frequency range of 920 to 960 MHz.

- Typical Doherty Single–Carrier W–CDMA Performance: V_{DD} = 28 Volts, I_{DQA} = 680 mA, V_{GSB} = 0.4 Vdc, P_{out} = 56 Watts Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

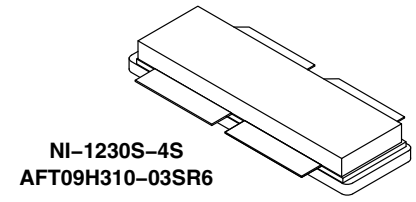
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
920 MHz	17.9	47.4	8.2	–28.5
940 MHz	18.0	48.5	8.1	–31.2
960 MHz	18.2	47.3	7.9	–35.0

Features

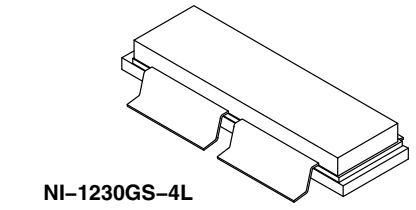
- Advanced High Performance In–Package Doherty
- Greater Negative Gate–Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- In Tape and Reel. R6 Suffix = 150 Units, 56 mm Tape Width, 13–inch Reel.

AFT09H310–03SR6
AFT09H310–04GSR6

920–960 MHz, 56 W AVG., 28 V
AIRFAST RF POWER LDMOS TRANSISTORS



NI–1230S–4S
AFT09H310–03SR6



NI–1230GS–4L
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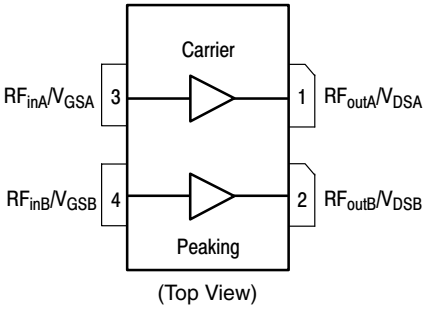


(Top View)

Figure 1. Pin Connections

freescale Airfast

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	–0.5, +70	Vdc
Gate–Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	–40 to +225	°C
CW Operation @ T_C = 25°C Derate above 25°C	CW	256 0.9	W W/°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 75°C, 56 W W–CDMA, 28 Vdc, I_{DQA} = 680 mA, V_{GSB} = 0.4 Vdc, 940 MHz	$R_{\theta JC}$	0.41	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22–A114)	2
Machine Model (per EIA/JESD22–A115)	B
Charge Device Model (per JESD22–C101)	IV

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (4)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics – Side A (4) (Carrier)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 242 μAdc)	$V_{GS(th)}$	0.9	1.5	1.9	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DA} = 680 mAdc, Measured in Functional Test)	$V_{GSA(Q)}$	1.7	2.1	2.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1.0 Adc)	$V_{DS(on)}$	0.05	0.2	0.4	Vdc
On Characteristics – Side B (4) (Peaking)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 310 μAdc)	$V_{GS(th)}$	0.9	1.5	1.9	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1.0 Adc)	$V_{DS(on)}$	0.05	0.2	0.4	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes – AN1955.
4. Each side of device measured separately.

(continued)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1,2,3) (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 680 mA, V_{GSB} = 0.4 Vdc, P_{out} = 56 W Avg., f = 920 MHz, Single–Carrier W–CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	17.7	17.9	20.7	dB
Drain Efficiency	η_D	45.3	47.4	—	%
Output Peak–to–Average Ratio @ 0.01% Probability on CCDF	PAR	7.6	8.2	—	dB
Adjacent Channel Power Ratio	ACPR	—	–28.5	–27.3	dBc
Load Mismatch (In Freescale Test Fixture, 50 ohm system) I_{DQA} = 680 mA, f = 940 MHz					
VSWR 10:1 at 32 Vdc, 280 W CW(4) Output Power (3 dB Input Overdrive from 180 W CW Rated Power)	No Device Degradation				
Typical Performances (2) (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 680 mA, V_{GSB} = 0.4 Vdc, 920–960 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	180	—	W
P_{out} @ 3 dB Compression Point (5)	P3dB	—	390	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 920 to 960 MHz frequency range)	Φ	—	31.7	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	45	—	MHz
Gain Flatness in 40 MHz Bandwidth @ P_{out} = 56 W Avg.	G_F	—	0.3	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.015	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C)	ΔP1dB	—	0.035	—	dB/°C

1. Part internally matched both on input and output.
2. Measurements made with device in an asymmetrical Doherty configuration.
3. Measurements made with device in straight lead configuration before any lead forming operation is applied. Lead forming is used for gull wing (GS) parts.
4. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.
5. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W–CDMA single–carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.

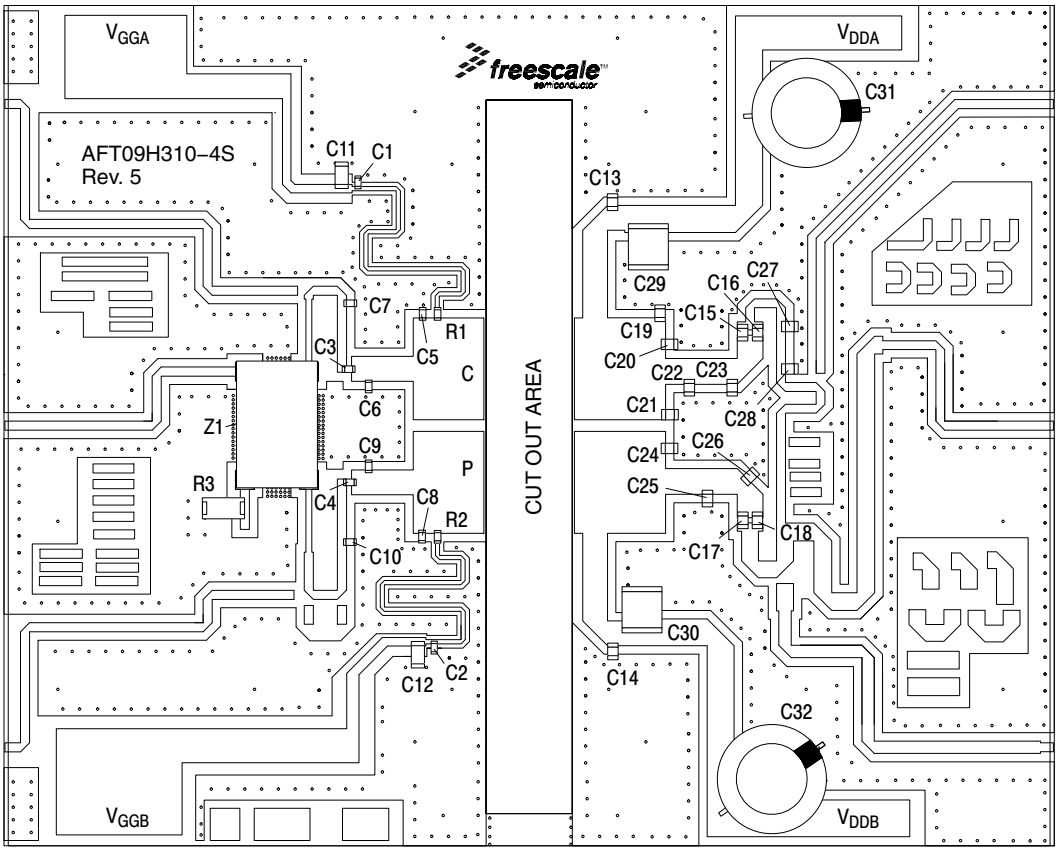


Figure 2. AFT09H310–03SR6 Test Circuit Component Layout — 920–960 MHz

Table 5. AFT09H310–03SR6 Test Circuit Component Designations and Values — 920–960 MHz

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4	47 pF Chip Capacitors	GQM1875C2E470JB15	Muruta
C5, C6	8.2 pF Chip Capacitors	GQM1875C2E8R2CB12D	Muruta
C7, C10	1.2 pF Chip Capacitors	GQM1875C2E1R2BB15	Muruta
C8, C9	6.8 pF Chip Capacitors	GQM1875C2E6R8BB15	Muruta
C11, C12	10 μF Chip Capacitors	GQM1875C2E6R8CB12D	Muruta
C13, C14, C15, C16, C17, C18	68 pF Chip Capacitors	GQM2195C2E680GB15	Muruta
C19, C20, C21	6.8 pF Chip Capacitors	GQM2195C2E6R8BB15	Muruta
C22	3.3 pF Chip Capacitor	GQM2195C2E3R3BB15	Muruta
C23, C24	3.9 pF Chip Capacitors	GQM2195C2E3R9BB15	Muruta
C25, C26	4.7 pF Chip Capacitors	GQM2195C2E4R7BB15	Muruta
C27, C28	1.8 pF Chip Capacitors	GQM2195C2E1R8BB15	Muruta
C29, C30	10 μF Chip Capacitors	C5750X7S2A106M230K	TDK
C31, C32	470 μF, 63 V Chip Capacitors	MCGPR100V477M16X32-RH	Multicomp
R1, R2	5.1 Ω, 1/10 W Chip Resistors	CRCW06035R10FKEA	Vishay
R3	50 Ω, 10 W Termination	06012A25X50–2	Anaren
Z1	800–1000 MHz, 5 dB, Directional Coupler	XC0900A-05S	Anaren
PCB	0.020″, ε_r = 3.5	RO4350	Rogers

TYPICAL CHARACTERISTICS

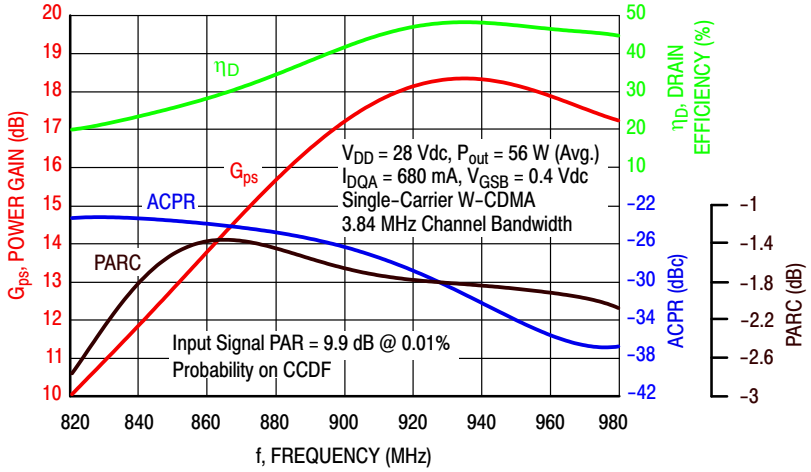


Figure 3. Single–Carrier Output Peak–to–Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 56 Watts Avg.

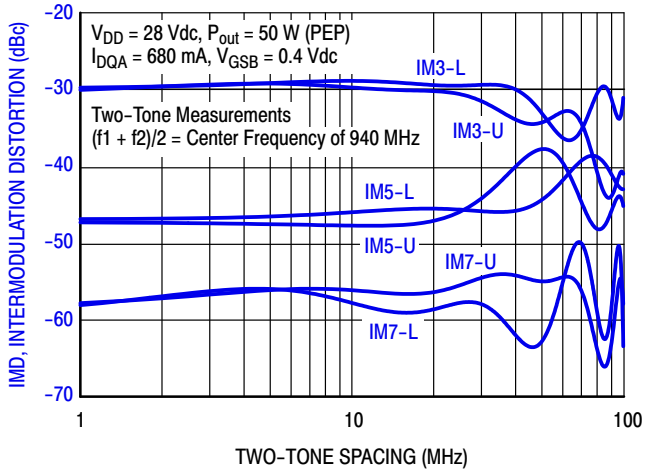


Figure 4. Intermodulation Distortion Products versus Two–Tone Spacing

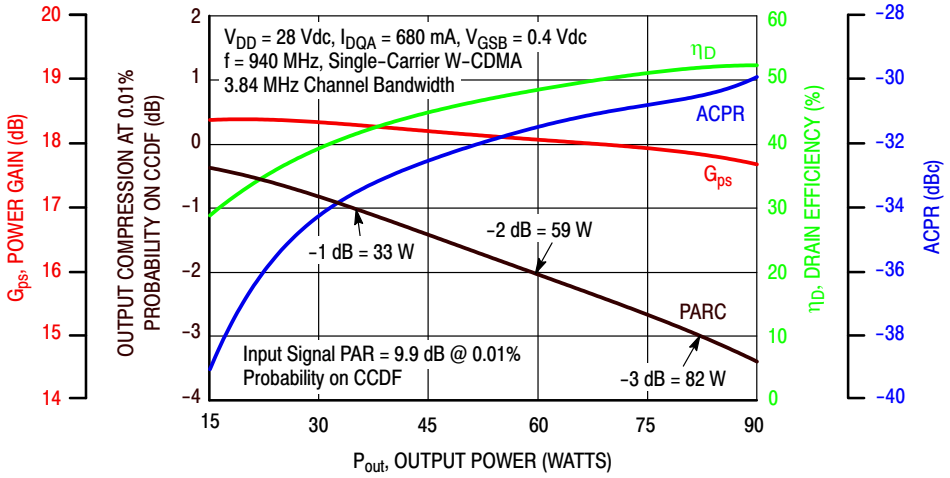


Figure 5. Output Peak–to–Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

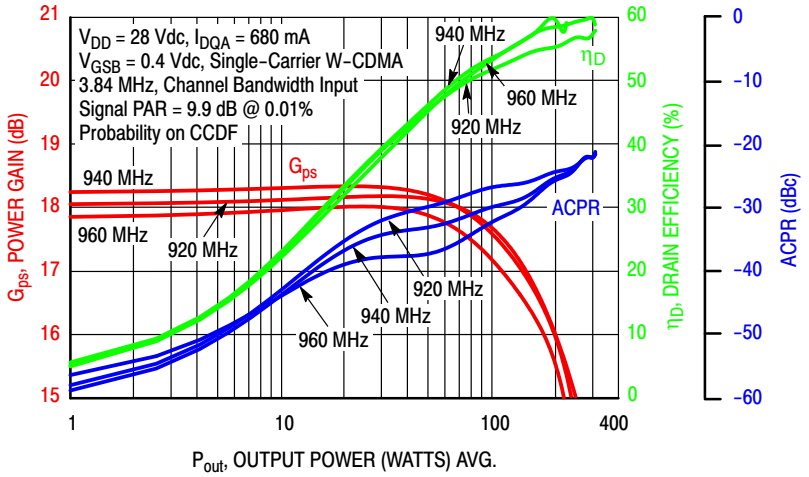


Figure 6. Single−Carrier W−CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

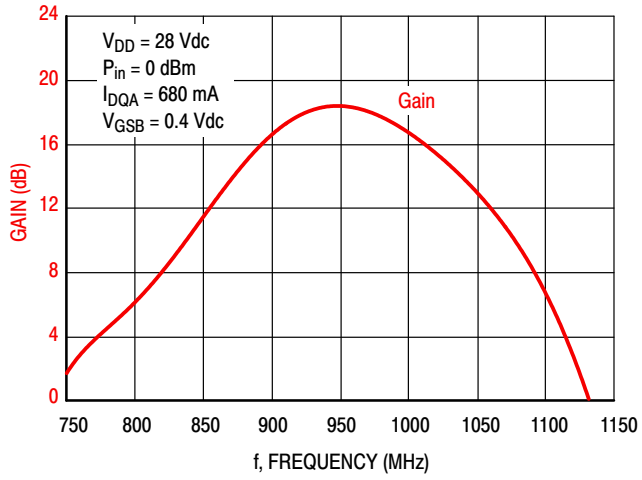


Figure 7. Broadband Frequency Response

V_{DD} = 28 Vdc, I_{DQA} = 694 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	1.16 - j2.31	1.24 + j2.27	3.28 - j1.37	20.3	52.8	190	54.5	-8.1
940	1.35 - j2.39	1.40 + j2.40	3.44 - j1.49	20.2	52.9	193	55.0	-7.5
960	1.63 - j2.70	1.64 + j2.55	3.64 - j1.33	20.1	53.0	200	55.7	-8.2

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	1.16 - j2.31	1.26 + j2.47	4.06 - j1.21	17.9	53.9	244	56.5	-13
940	1.35 - j2.39	1.44 + j2.60	4.14 - j1.14	18.0	53.9	247	57.5	-12
960	1.63 - j2.70	1.72 + j2.76	4.29 - j0.91	17.8	54.0	252	58.0	-13

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 8. Carrier Side Load Pull Performance — Maximum Power Tuning

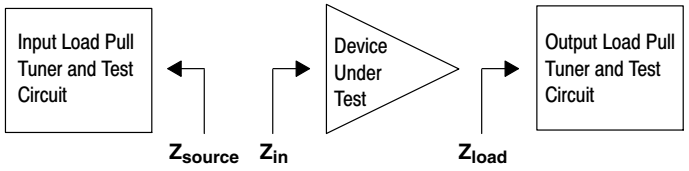
V_{DD} = 28 Vdc, I_{DQA} = 694 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	1.16 - j2.31	0.81 + j1.89	0.96 - j0.03	24.8	49.9	99	68.9	-21
940	1.35 - j2.39	0.94 + j1.98	0.95 - j0.14	24.9	49.9	98	69.9	-21
960	1.63 - j2.70	1.07 + j2.08	0.86 - j0.21	25.0	49.6	92	71.0	-24

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	1.16 - j2.31	0.89 + j2.16	1.06 + j0.03	22.8	50.8	121	70.9	-29
940	1.35 - j2.39	1.06 + j2.28	1.10 - j0.07	22.8	50.9	124	72.0	-27
960	1.63 - j2.70	1.39 + j2.49	1.40 - j0.21	21.7	51.8	153	71.6	-23

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 9. Carrier Side Load Pull Performance — Maximum Drain Efficiency Tuning



V_{DD} = 28 Vdc, V_{GSB} = 0.4 Vdc, Pulsed CW, 10 µsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	1.72 - j3.65	1.84 + j3.30	4.60 - j2.13	13.7	53.8	241	55.6	-8.3
940	2.37 - j3.46	2.28 + j3.50	5.46 - j2.55	13.3	53.9	245	53.1	-7.3
960	2.89 - j3.77	2.85 + j3.70	5.68 - j2.16	13.3	54.0	250	54.1	-7.9

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	1.72 - j3.65	1.99 + j3.42	5.63 - j2.02	11.2	54.9	312	56.1	-11
940	2.37 - j3.46	2.43 + j3.61	6.13 - j1.80	11.1	55.0	313	55.8	-10
960	2.89 - j3.77	3.06 + j3.78	6.35 - j1.22	11.1	55.0	318	56.3	-10

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 10. Peaking Side Load Pull Performance — Maximum Power Tuning

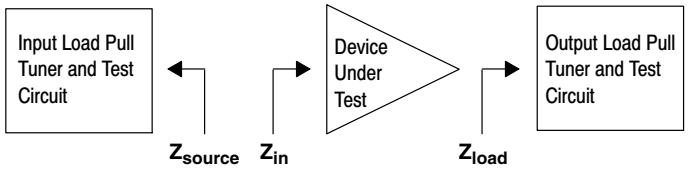
V_{DD} = 28 Vdc, V_{GSB} = 0.4 Vdc, Pulsed CW, 10 µsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	1.72 - j3.65	1.63 + j3.16	1.40 - j0.57	14.9	51.3	135	70.4	-15
940	2.37 - j3.46	1.95 + j3.29	0.95 - j0.75	14.8	50.1	102	72.3	-17
960	2.89 - j3.77	2.52 + j3.52	1.33 - j0.87	14.8	51.1	130	72.7	-16

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	1.72 - j3.65	1.74 + j3.32	1.57 - j0.45	12.9	52.2	167	71.4	-19
940	2.37 - j3.46	2.16 + j3.51	1.67 - j0.54	12.8	52.3	171	72.1	-18
960	2.89 - j3.77	2.71 + j3.69	1.55 - j0.69	12.8	52.2	164	73.2	-20

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 11. Peaking Side Load Pull Performance — Maximum Drain Efficiency Tuning



P1dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 940 MHz

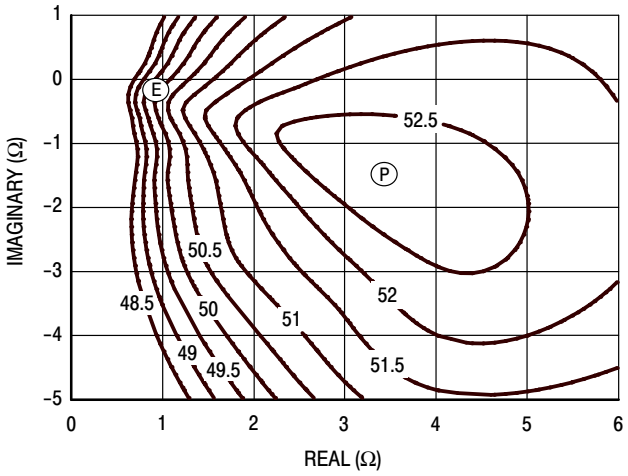


Figure 12. P1dB Load Pull Output Power Contours (dBm)

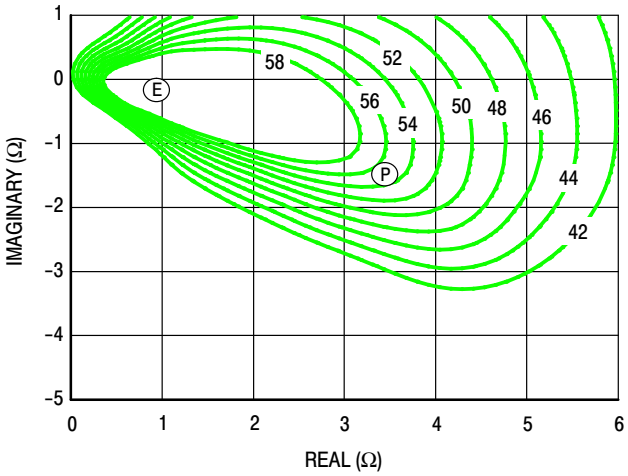


Figure 13. P1dB Load Pull Efficiency Contours (%)

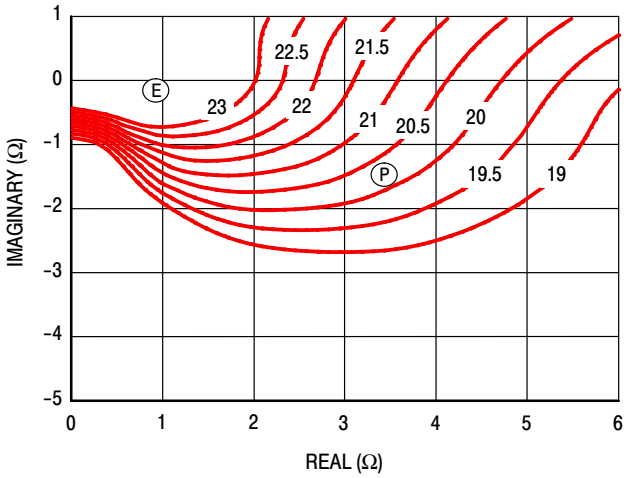


Figure 14. P1dB Load Pull Gain Contours (dB)

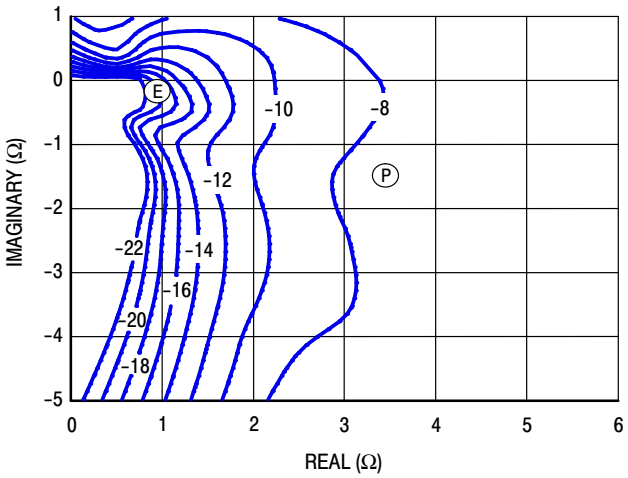


Figure 15. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 940 MHz

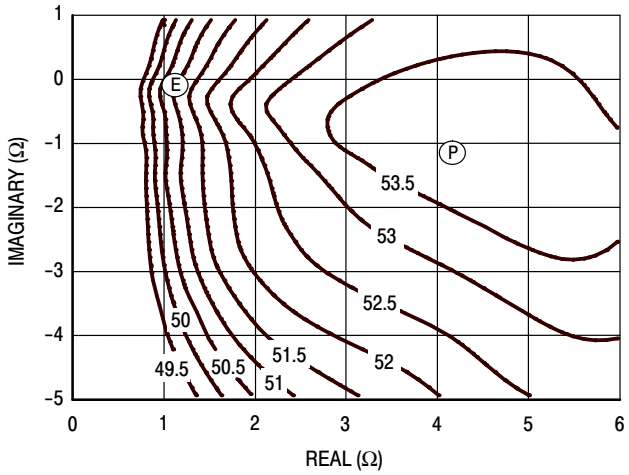


Figure 16. P3dB Load Pull Output Power Contours (dBm)

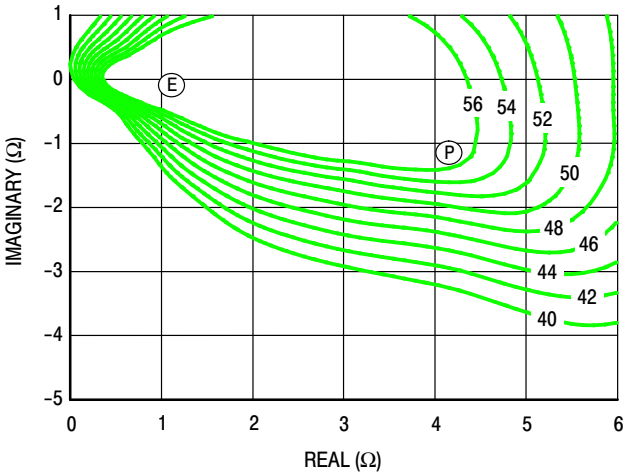


Figure 17. P3dB Load Pull Efficiency Contours (%)

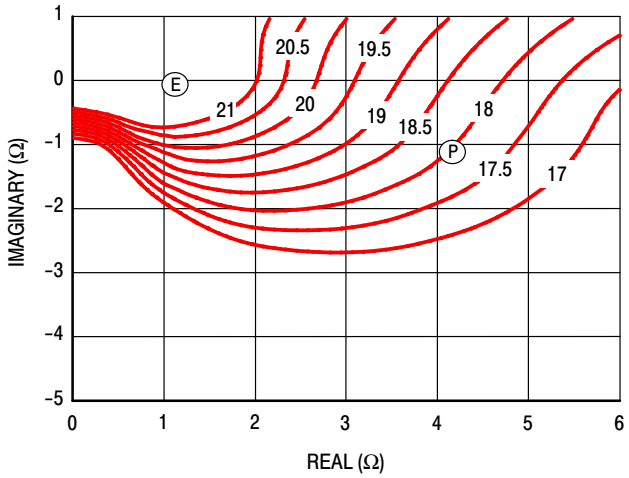


Figure 18. P3dB Load Pull Gain Contours (dB)

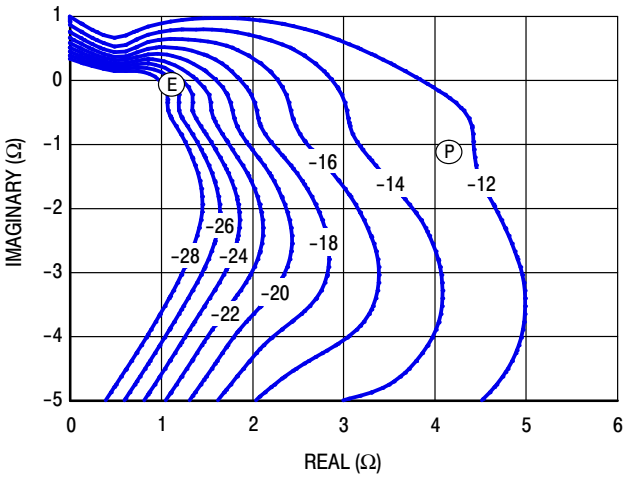


Figure 19. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P1dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 940 MHz

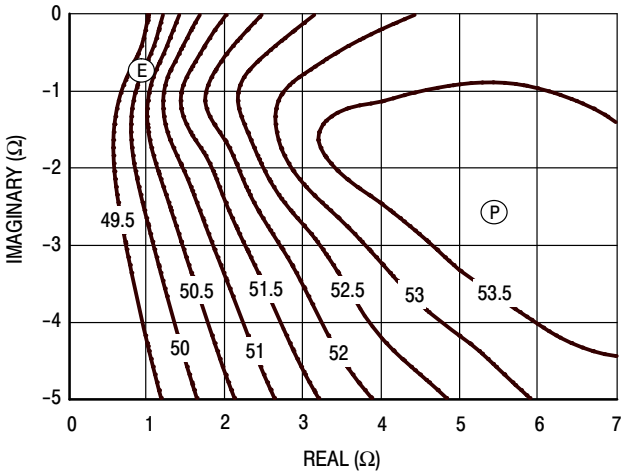


Figure 20. P1dB Load Pull Output Power Contours (dBm)

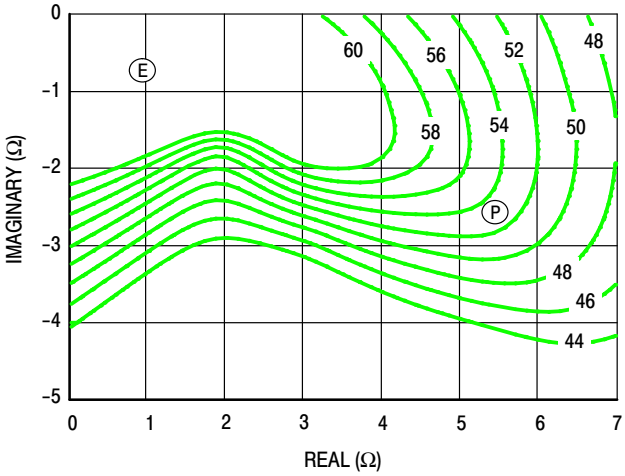


Figure 21. P1dB Load Pull Efficiency Contours (%)

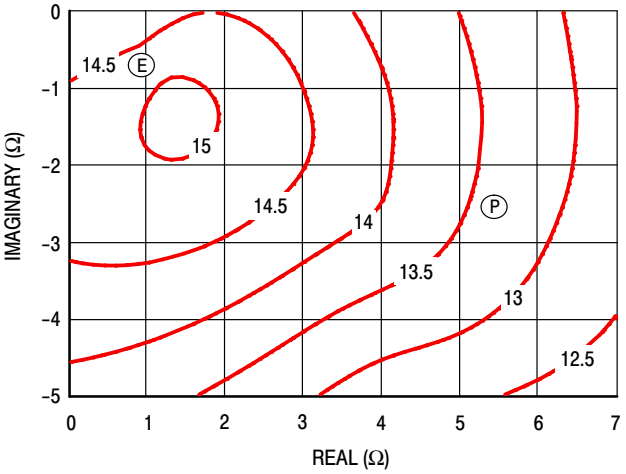


Figure 22. P1dB Load Pull Gain Contours (dB)

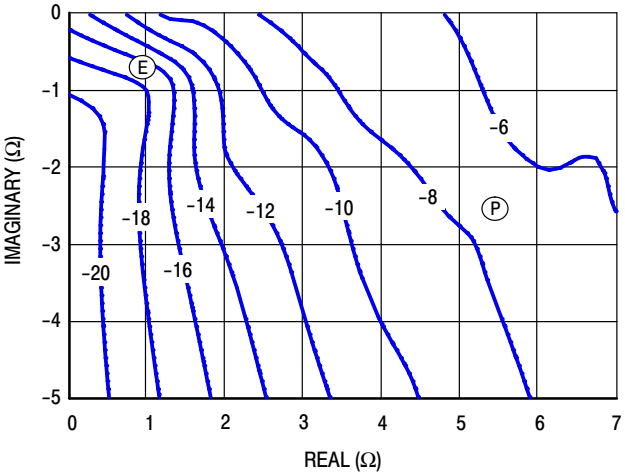


Figure 23. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 940 MHz

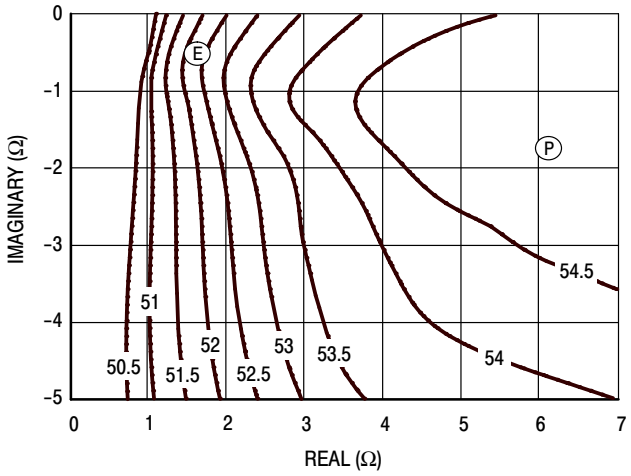


Figure 24. P3dB Load Pull Output Power Contours (dBm)

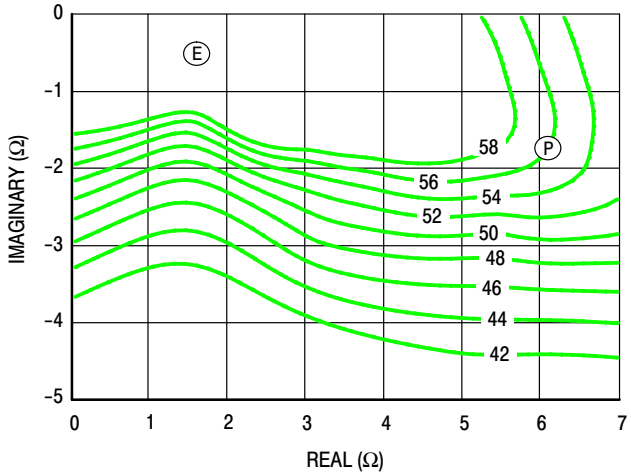


Figure 25. P3dB Load Pull Efficiency Contours (%)

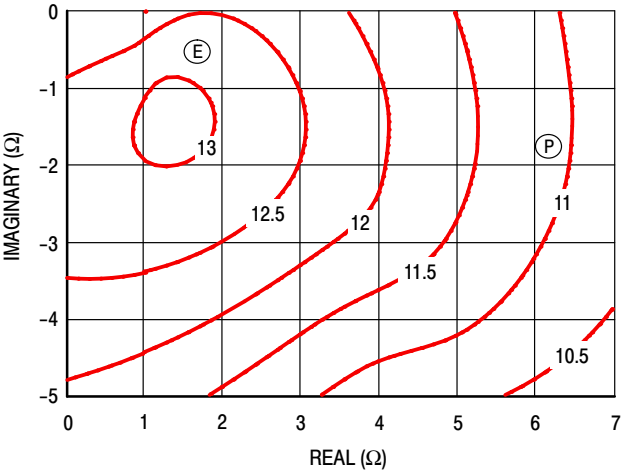


Figure 26. P3dB Load Pull Gain Contours (dB)

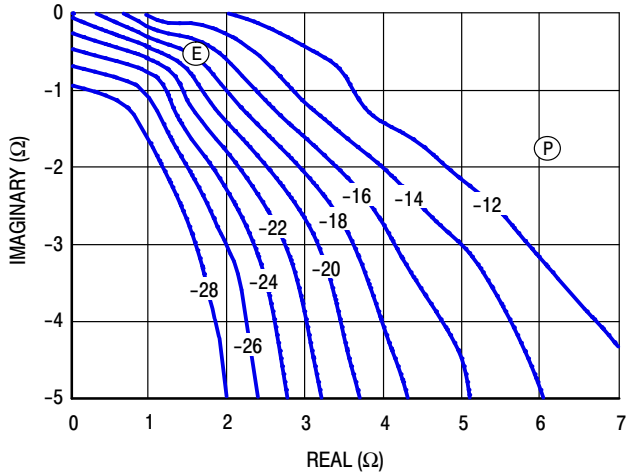


Figure 27. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

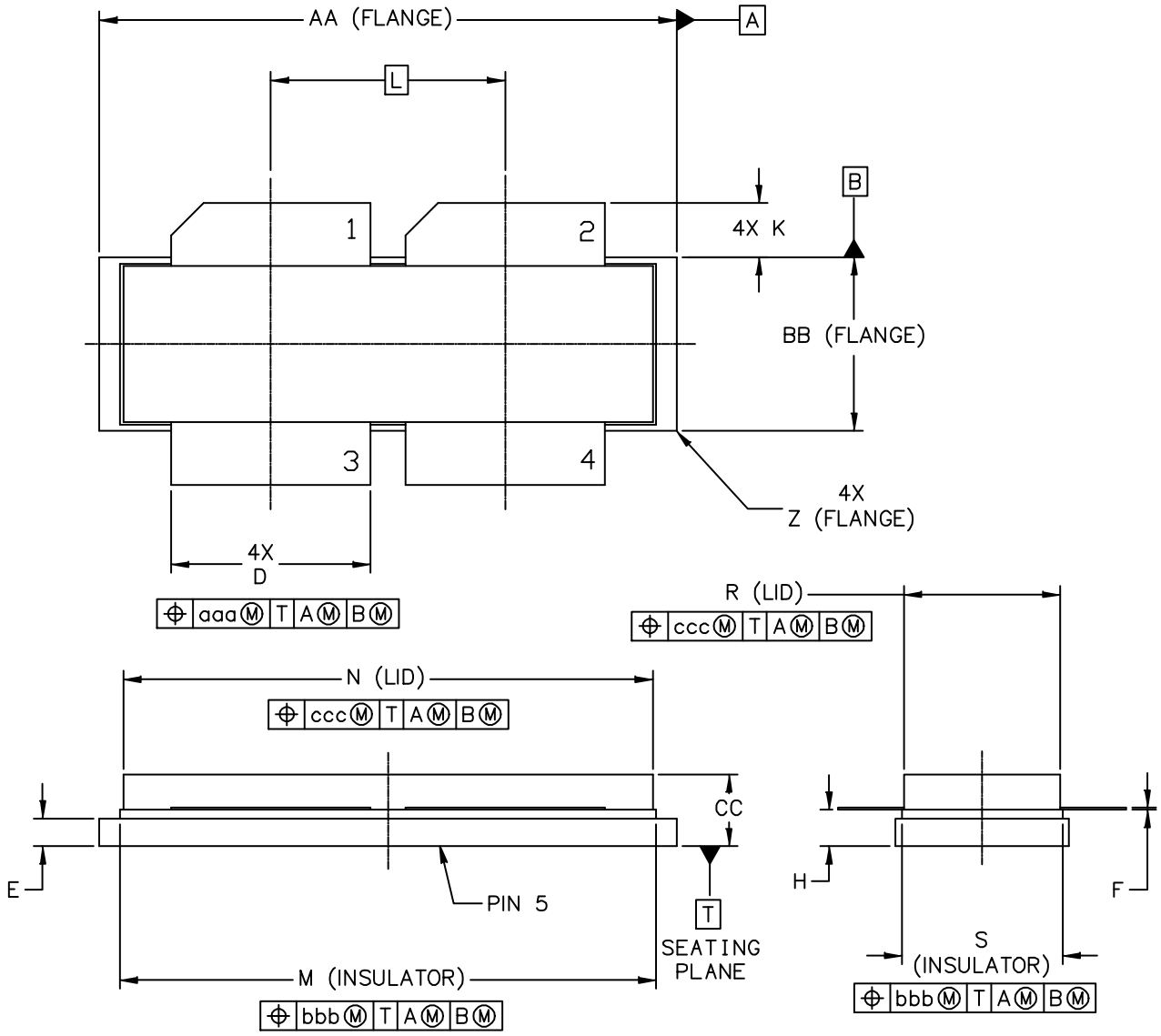
Gain

Drain Efficiency

Linearity

Output Power

PACKAGE DIMENSIONS



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NOTES:

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH
3. DIMENSION H IS MEASURED .030 INCH (0.762 MM) AWAY FROM PACKAGE BODY

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
AA	1.265	1.275	32.13	32.39	R	.355	.365	9.02	9.27
BB	.395	.405	10.03	10.29	S	.365	.375	9.27	9.53
CC	.170	.190	4.32	4.83	Z	R.000	R.040	R0.00	R1.02
D	.455	.465	11.56	11.81					
E	.062	.066	1.57	1.68	aaa	.013		0.33	
F	.004	.007	0.10	0.18	bbb	.010		0.25	
H	.082	.090	2.08	2.29	ccc	.020		0.51	
K	.117	.137	2.97	3.48					
L	.540 BSC		13.72 BSC						
M	1.219	1.241	30.96	31.52					
N	1.218	1.242	30.94	31.55					

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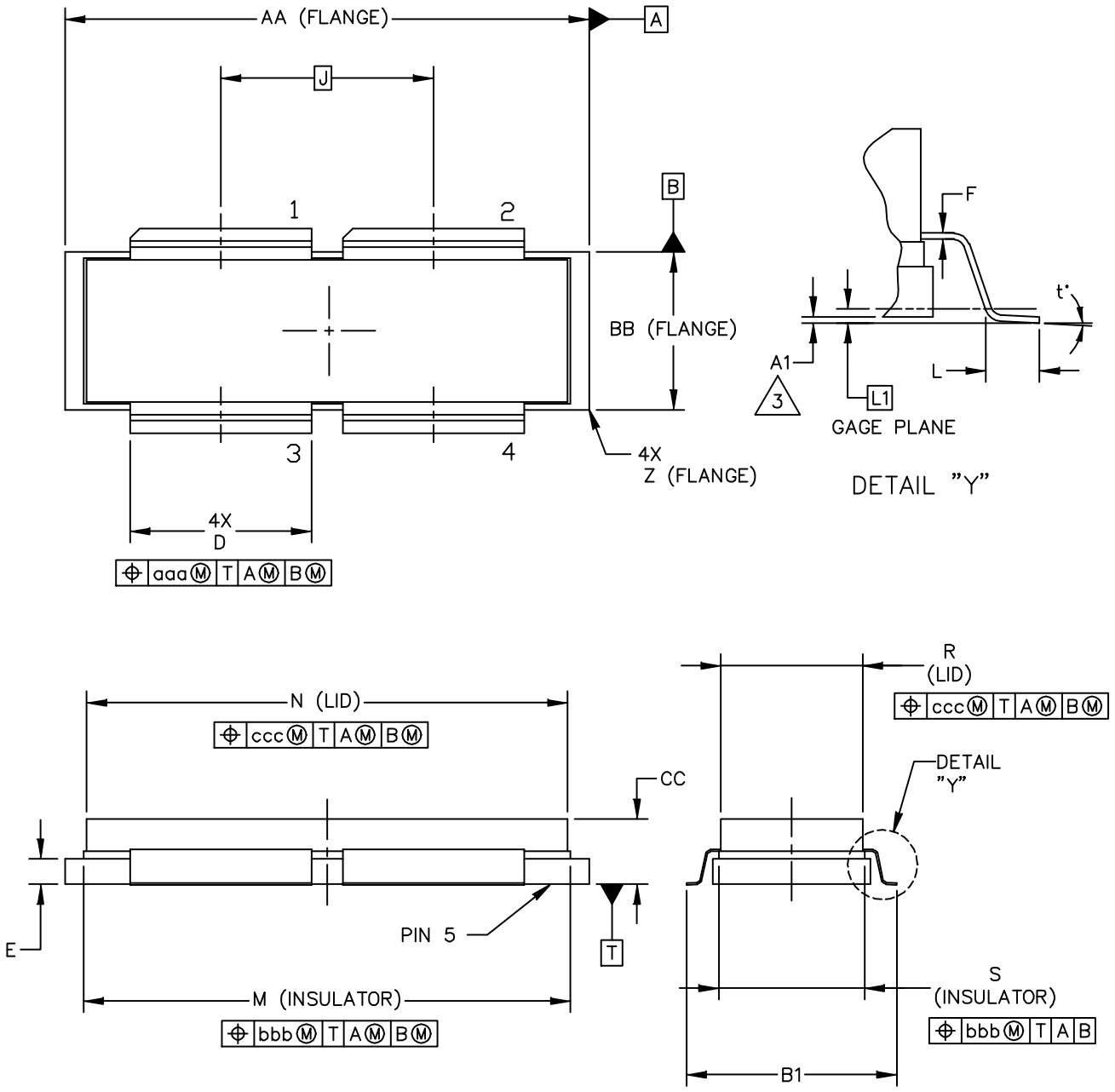

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NOTES:

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M−1994.

2. CONTROLLING DIMENSION: INCH

3. DIMENSION A1 IS MEASURED WITH REFERENCE TO DATUM T. THE POSITIVE VALUE IMPLIES THAT THE PACKAGE BOTTOM IS HIGHER THAN THE LEAD BOTTOM.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
AA	1.265	1.275	32.13	32.39	R	.355	.365	9.02	9.27
A1	−.001	.011	−0.03	0.28	S	.365	.375	9.27	9.53
BB	.395	.405	10.03	10.29	Z	R.000	R.040	R0.00	R1.02
B1	.564	.574	14.32	14.58	t°	0°	8°	0°	8°
CC	.170	.190	4.32	4.83					
D	.455	.465	11.56	11.81	aaa	.013		0.33	
E	.062	.066	1.57	1.68	bbb	.010		0.25	
F	.004	.007	0.10	0.18	ccc	.020		0.51	
J	.540 BSC		13.72 BSC						
L	.038	.046	0.97	1.17					
L1	.01 BSC		0.25 BSC						
M	1.219	1.241	30.96	31.52					
N	1.218	1.242	30.94	31.55					

MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following documents, software and tools to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	July 2013	• Initial Release of Data Sheet
1	Sept. 2013	• On Characteristics table, Side B (Peaking): corrected $V_{GS(th)}$ Typ value from 2.0 to 1.5 Vdc, p. 2

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