LMH6586 32x16 Video Crosspoint Switch

Check for Samples: LMH6586

FEATURES

- **32 inputs and 16 outputs**
- **AC-coupled inputs with integrated DC restore clamp**
- **Individually addressable outputs**
- **Pin-selectable output buffer gain (1 V/V or 2 V/V)**
- **–3 dB bandwidth = 66 MHz**
- **DG = 0.05%, DP = 0.05° @ R_L = 150Ω, A_V = 2V/V**
- **−70 dB off-isolation @ 6 MHz**
- **Individual input and output shutdown modes**
- **Device power down mode**
- **Video detection with programmable threshold (8 levels)**
- **Sync detection with pin-configurable threshold**
- **100 kHz I^2C interface with 2-bit configurable slave address**
- **Single 5V supply operation**
- **Extra video output (VOUT_16) for external video sync separator**

APPLICATIONS

- **CCTV security and surveillance systems**
- **Analog video routing**

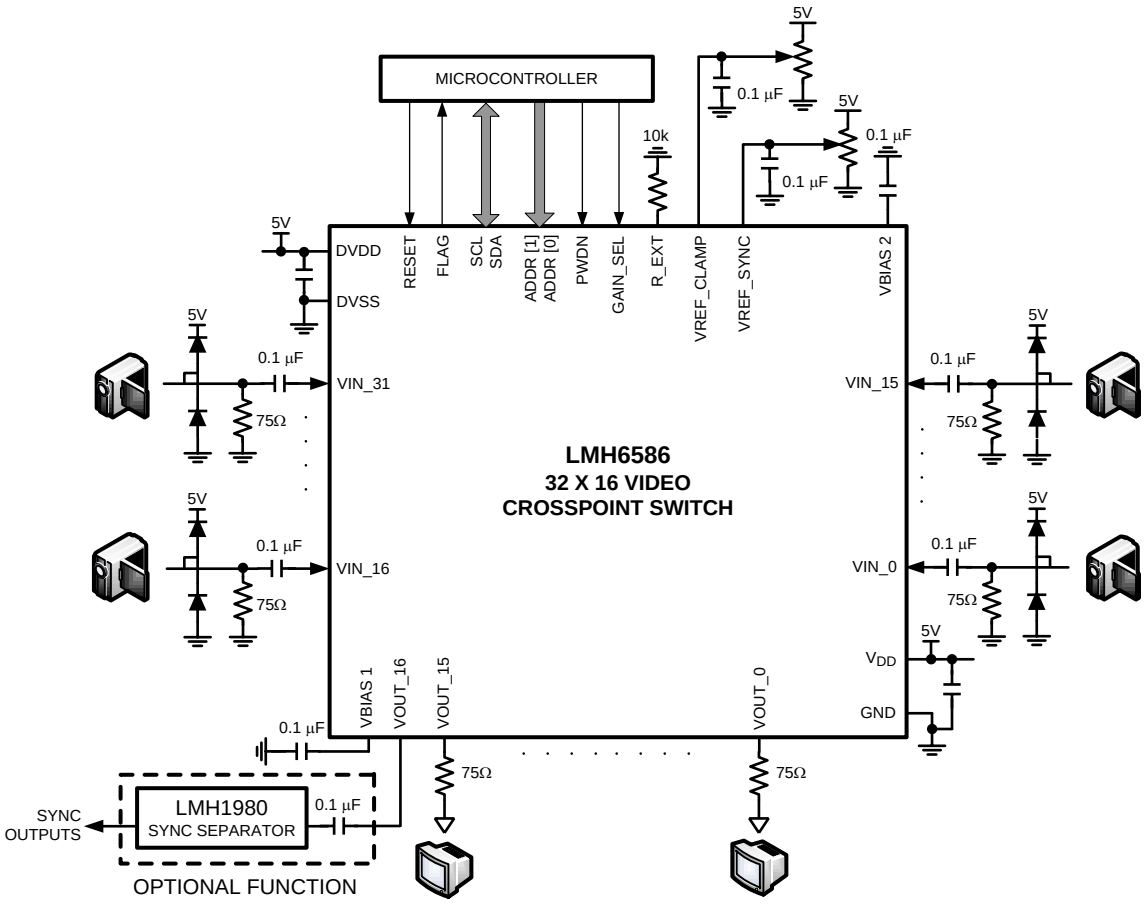
DESCRIPTION

The LMH6586 is a non-blocking analog video crosspoint switch designed for routing standard NTSC or PAL composite video signals. The non-blocking architecture allows any of the 32 inputs to be connected to any of the 16 outputs, including any input that is already connected. Each input has an integrated DC restore clamp for biasing of the AC-coupled video signal. The output buffers have a common selectable gain setting of 1X or 2X and can drive loads of 150Ω.

The LMH6586 features two types of input signal detection for convenient monitoring of activity on any input channel. Video detection can be configured to indicate when either “presence of video” or “loss of video” is detected across the video threshold level controlled by a programmable register. Additionally, sync detection can be configured to indicate when “loss of sync” is detected across the sync threshold level controlled by a DC voltage input.

The switch configuration and other parameters are programmable via the I^2C bus interface. The slave device address is configurable via two external pins allowing up to four LMH6586 devices, each with a unique address, on a common I^2C bus. This helps facilitate expansion of the crosspoint matrix array size (e.g. 64 x 16). The LMH6586 operates from a common single 5V supply for its analog sections as well as its control logic and I^2C interface. The LMH6586 is offered in a space-saving 80-pin TQFP.

Application Diagram



Functional Diagram

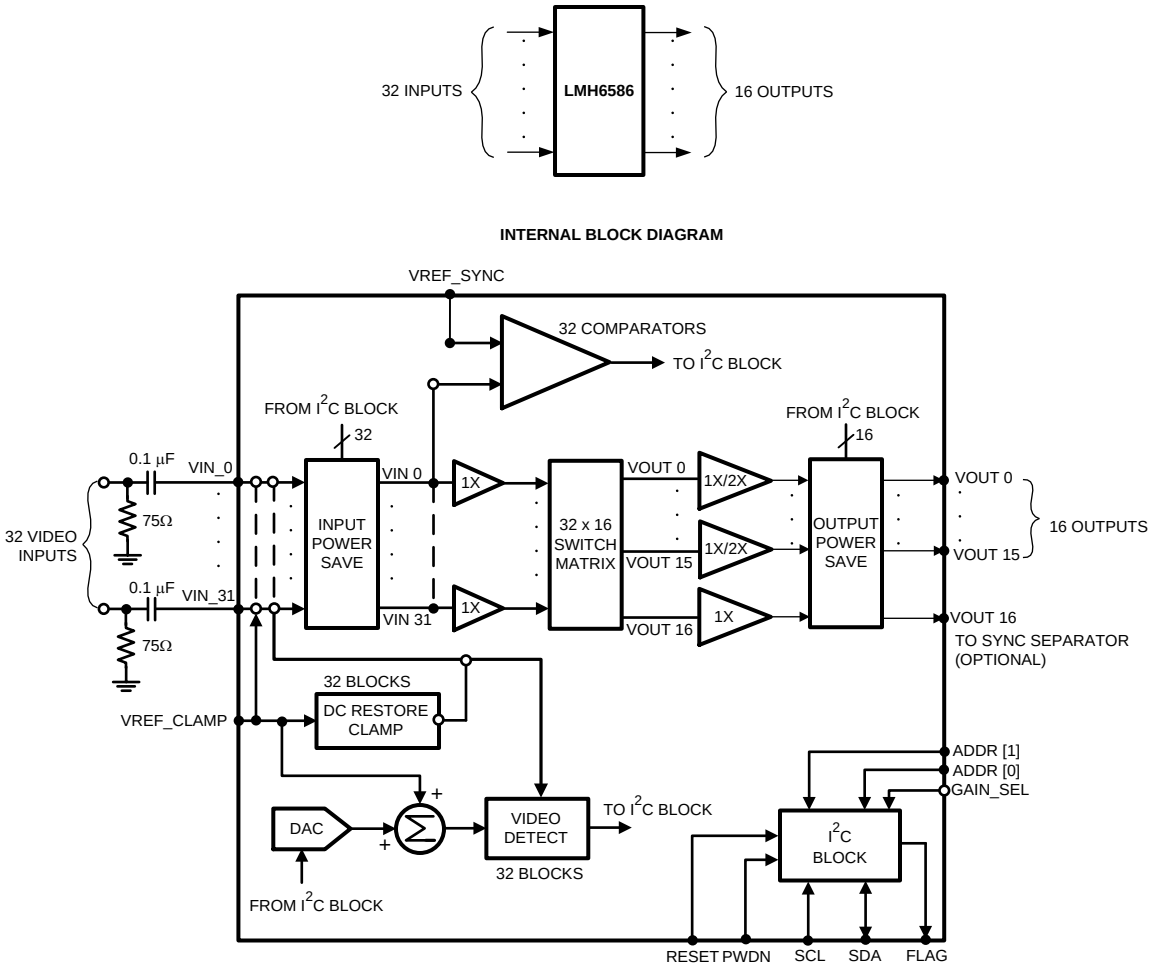
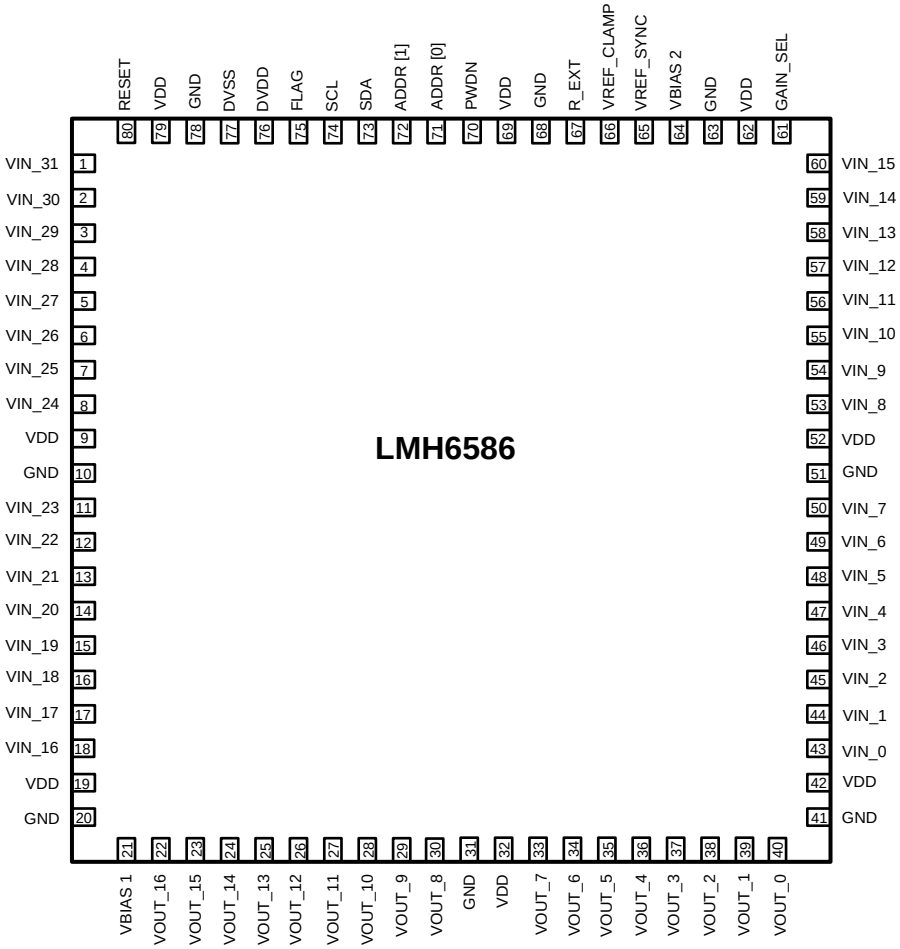


Figure 1. Functional Diagram

Connection Diagram



Pin Functions

Pin Descriptions

Pin #	Pin Name	Pin Description
1	VIN_31	VIDEO INPUT 31
2	VIN_30	VIDEO INPUT 30
3	VIN_29	VIDEO INPUT 29
4	VIN_28	VIDEO INPUT 28
5	VIN_27	VIDEO INPUT 27
6	VIN-26	VIDEO INPUT 26
7	VIN_25	VIDEO INPUT 25
8	VIN_24	VIDEO INPUT 24
9	VDD	VDD (connect to 5V supply)
10	GND	GND
11	VIN_23	VIDEO INPUT 23
12	VIN_22	VIDEO INPUT 22
13	VIN_21	VIDEO INPUT 21
14	VIN_20	VIDEO INPUT 20
15	VIN_19	VIDEO INPUT 19

Pin Descriptions (continued)

Pin #	Pin Name	Pin Description
16	VIN_18	VIDEO INPUT 18
17	VIN_17	VIDEO INPUT 17
18	VIN_16	VIDEO INPUT 16
19	VDD	VDD (connect to 5V supply)
20	GND	GND
21	VBIAS 1	VBIAS 1 (connect to external 0.1 µF capacitor)
22	VOUT_16	VIDEO OUTPUT 16
23	VOUT_15	VIDEO OUTPUT 15
24	VOUT_14	VIDEO OUTPUT 14
25	VOUT_13	VIDEO OUTPUT 13
26	VOUT_12	VIDEO OUTPUT 12
27	VOUT_11	VIDEO OUTPUT 11
28	VOUT_10	VIDEO OUTPUT 10
29	VOUT_9	VIDEO OUTPUT 9
30	VOUT_8	VIDEO OUTPUT 8
31	GND	GND
32	VDD	VDD (connect to 5V supply)
33	VOUT_7	VIDEO OUTPUT 7
34	VOUT_6	VIDEO OUTPUT 6
35	VOUT_5	VIDEO OUTPUT 5
36	VOUT_4	VIDEO OUTPUT 4
37	VOUT_3	VIDEO OUTPUT 3
38	VOUT_2	VIDEO OUTPUT 2
39	VOUT_1	VIDEO OUTPUT 1
40	VOUT_0	VIDEO OUTPUT 0
41	GND	GND
42	VDD	VDD (connect to 5V supply)
43	VIN_0	VIDEO INPUT 0
44	VIN_1	VIDEO INPUT 1
45	VIN_2	VIDEO INPUT 2
46	VIN_3	VIDEO INPUT 3
47	VIN_4	VIDEO INPUT 4
48	VIN_5	VIDEO INPUT 5
49	VIN_6	VIDEO INPUT 6
50	VIN_7	VIDEO INPUT 7
51	GND	GND
52	VDD	VDD (connect to 5V supply)
53	VIN_8	VIDEO INPUT 8
54	VIN_9	VIDEO INPUT 9
55	VIN_10	VIDEO INPUT 10
56	VIN_11	VIDEO INPUT 11
57	VIN_12	VIDEO INPUT 12
58	VIN_13	VIDEO INPUT 13
59	VIN_14	VIDEO INPUT 14
60	VIN_15	VIDEO INPUT 15
61	GAIN	GAIN SELECT INPUT (set low for 1X gain, or set high for 2X gain)
62	VDD	VDD (connect to 5V supply)

Pin Descriptions (continued)

Pin #	Pin Name	Pin Description
63	GND	GND
64	VBIAS 2	VBIAS 2 (connect to external 0.1 µF capacitor)
65	VREF_SYNC	SYNC DETECTION THRESHOLD VOLTAGE INPUT (bias to 350 mV_{DC}, recommended)
66	VREF_CLAMP	DC RESTORE CLAMP VOLTAGE INPUT (bias to 300 mV_{DC}, recommended)
67	R_EXT	R_EXT BIAS RESISTOR (connect to external 10 kΩ 1% resistor)
68	GND	GND
69	VDD	VDD (connect to 5V supply)
70	PWDN	POWER DOWN INPUT (set low for normal operation, set high to power down all video I/O blocks and I^2C interface)
71	ADDR [0]	I^2C SLAVE ADDRESS BIT 0 INPUT (set low for bit0 = 0, or set low for bit0 = 1)
72	ADDR [1]	I^2C SLAVE ADDRESS BIT 1 INPUT (set low for bit1 = 0, or set low for bit1 = 1)
73	SDA	I^2C DATA IN/OUT (requires external pull-up resistor to DVDD supply)
74	SCL	I^2C CLOCK INPUT (requires external pull-up resistor to DVDD supply)
75	FLAG	DETECTION FLAG OUTPUT (active high)
76	DVDD	DIGITAL VDD (connect to 5V supply)
77	DVSS	DIGITAL GND
78	GND	GND
79	VDD	VDD (connect to 5V supply)
80	RESET	RESET INPUT (set low for normal operation, set high to reset device registers to default settings)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

ESD Tolerance (2)	
Human Body Model	2500V
Machine Model	250V
Supply Voltage (V_{DD})	5V
Video Input Voltage Range, V_{IN}	−0.3V to V_{DD} +0.3V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	+150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics tables.

(2) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

Operating Ratings (1)

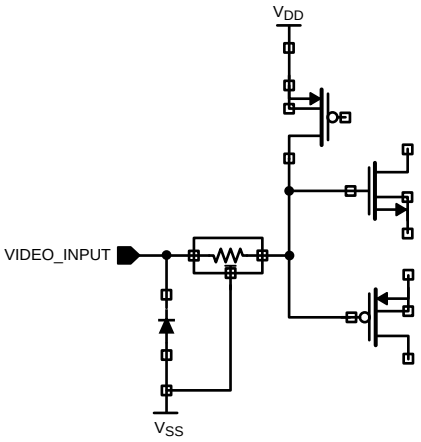
Supply Voltage (V_{DD})	5V ± 10%
Ambient Temperature Range	−40°C ≤ T_A ≤ 85°C
θ_{JA}	25°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics tables.

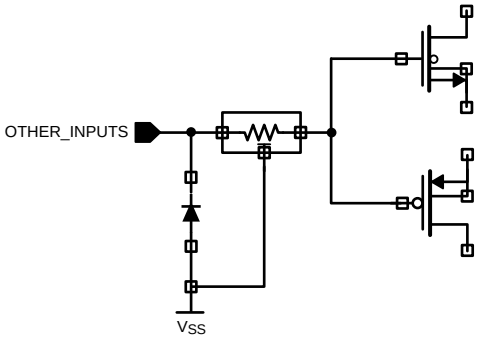
Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_A = 25°C, V_{DD} = 5V, R_{EXT} = 10 kΩ 1%, VREF_CLAMP = 300 mV, R_L = 150Ω, C_L = 12 pF.

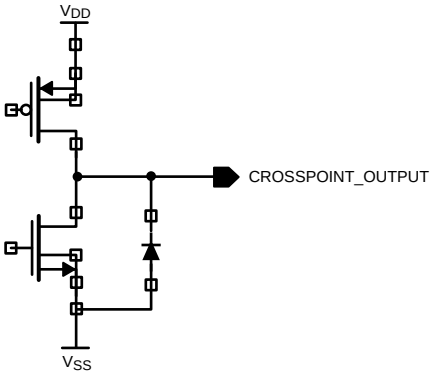
Symbol	Parameter	Conditions	Min	Typ	Max	Units
DC Specifications						
V_{DD}	Operating Supply Voltage		4.5		5.5	V
I_{DD}	Supply Current	No Load, A_V = 1 V/V		300	360	mA
	Power Save Supply Current	No Load, A_V = 1 V/V, SCL= SDA= PWDN= DVDD		1.5		mA
A_V	Gain	2x Gain Buffer	1.92	2.00	2.07	V/V
		1x Gain Buffer	0.95	0.99	1.03	
ΔA_{V_CH-CH}	Gain Matching (Ch to Ch)	A_V = 1 V/V		1.2	3	%
V_{OS}	Output Offset Voltage	A_V = 1 V/V, No Load (referenced to DC restored input)		60		mV
V_{DET_LSB}	Video Detection Threshold LSB		85	95	105	mV
V_{DET}	Video Detection Threshold Offset	Video detection threshold offset measured above sync tip level of DC restored input		±50		mV
AC Specifications						
BW_{SS}	Small Signal Bandwidth (−3 dB)	V_{OUT} = 20 mV_{PP}		66		MHz
BW_{LS}	Large Signal Bandwidth (−3 dB)	V_{OUT} = 1.5 V_{PP}		29		MHz
t_r/t_f	Rise/Fall Time	10% to 90%, V_{OUT} = 2 V_{PP}		35		ns
tp	Propagation Delay	50% to 50%, V_{OUT} = 2 V_{PP}		5		ns
t_{pCh-Ch}	Ch-Ch Propagation Delay	50% to 50%, V_{OUT} = 2 V_{PP}		5		ns
CT	Adjacent CH Crosstalk	f = 6 MHz, A_V = 2 V/V		−58		dB
Off Iso	Input-Output Off-Isolation	f = 6 MHz, A_V = 2 V/V		−70		dB
DG	Differential Gain Error for NTSC	A_V = 2 V/V, 3.5 MHz		0.05		%
DP	Differential Phase Error for NTSC	A_V = 2 V/V, 3.5 MHz		0.05		deg
I^2C Interface and Digital Pin Logic Levels						
V_{IL}	Low Input Voltage				1.5	V
V_{IH}	High Input Voltage		3.3			V
I_{IN}	Input Current			±1		µA
V_{OL}	Low Output Voltage	I_{OL} = 3 mA		0.5		V



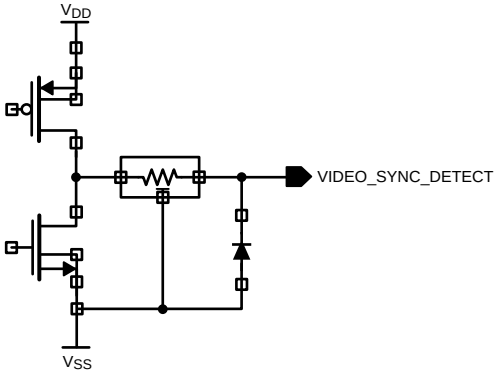
VIDEO INPUT CIRCUIT DIAGRAM



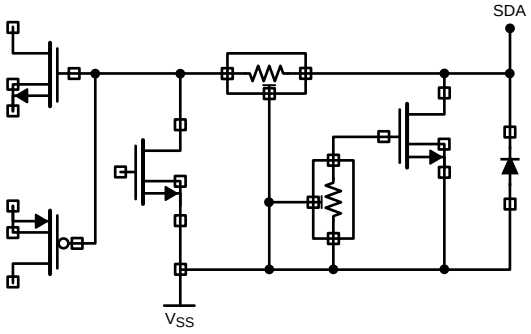
OTHER INPUT CIRCUIT DIAGRAM



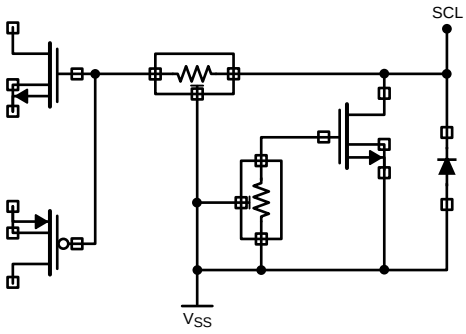
VIDEO OUTPUT CIRCUIT DIAGRAM



VIDEO SYNC DETECT CIRCUIT DIAGRAM



I2C DATA CIRCUIT DIAGRAM



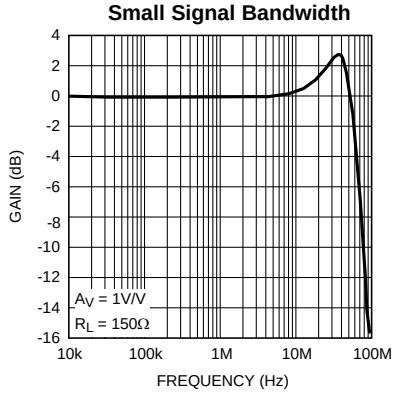
I2C CLOCK CIRCUIT DIAGRAM

Figure 2. Logic Diagram

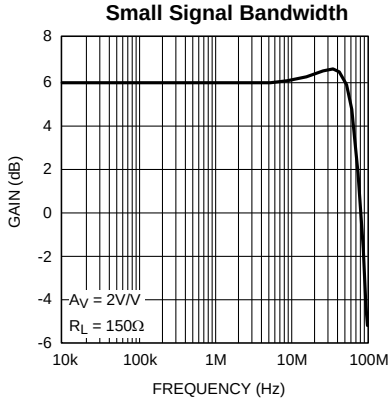
Typical Performance Characteristics

Unless otherwise specified, T_A = 25°C, V_{DD} = 5V, R_{EXT} = 10 kΩ 1%, R_L = 150Ω, C_L = 12 pF. Small Signal Input Signal = 20 mV_{PP}, Medium Signal Input Signal = 200 mV_{PP} , Large Signal Input Signal = 750 mV_{PP}

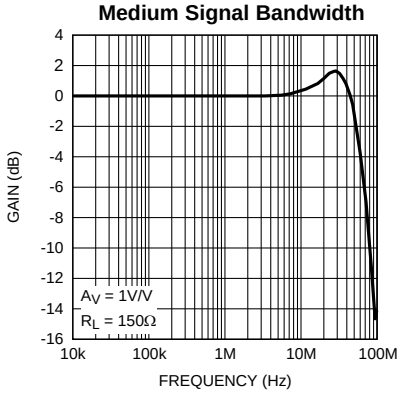
Small Signal Bandwidth



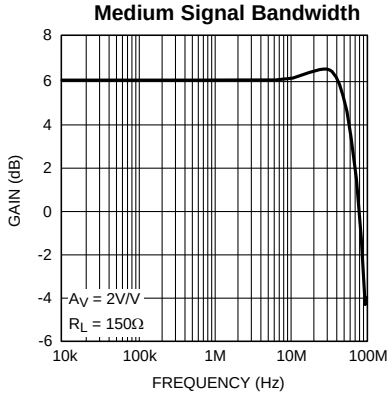
Small Signal Bandwidth



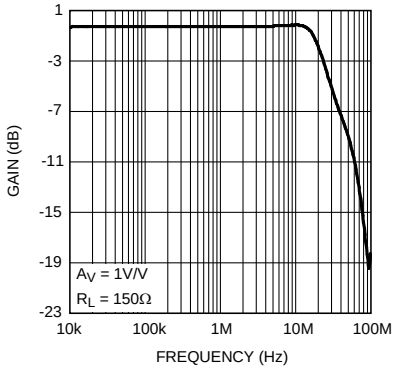
Medium Signal Bandwidth



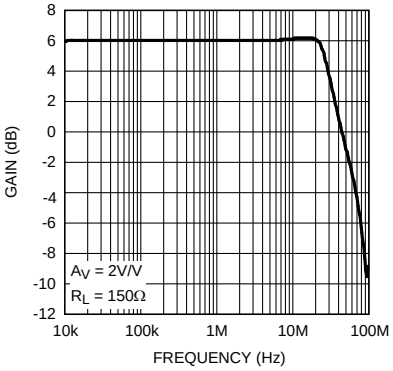
Medium Signal Bandwidth



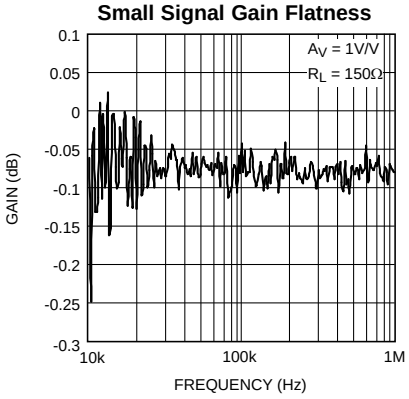
Large Signal Bandwidth



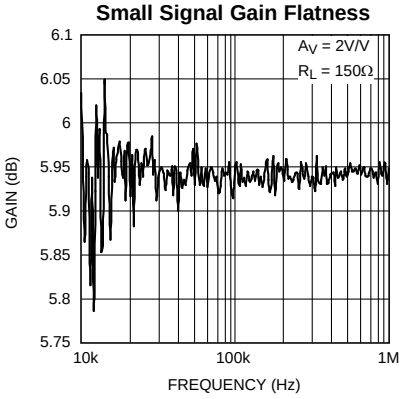
Large Signal Bandwidth



Small Signal Gain Flatness



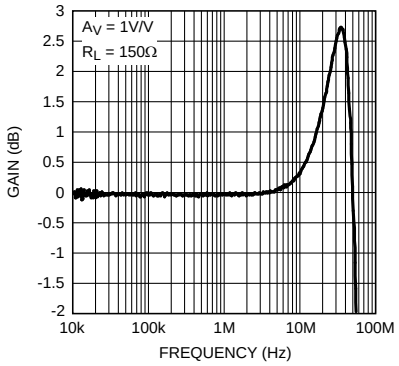
Small Signal Gain Flatness



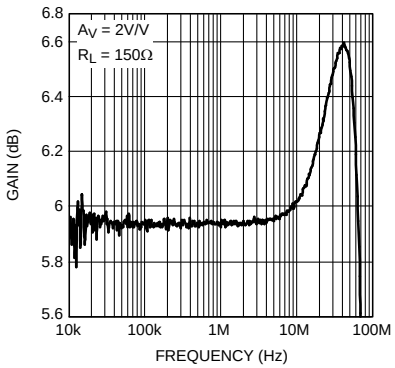
Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V_{DD} = 5V, R_{EXT} = 10 kΩ 1%, R_L = 150Ω, C_L = 12 pF. Small Signal Input Signal = 20 mV_{PP}, Medium Signal Input Signal = 200 mV_{PP} , Large Signal Input Signal = 750 mV_{PP}

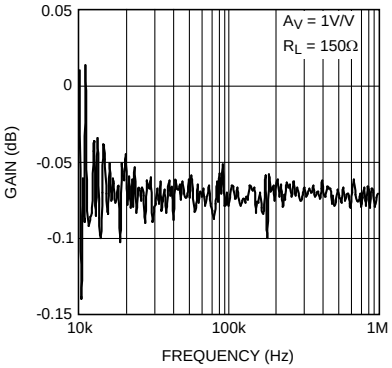
Small Signal Gain Peaking



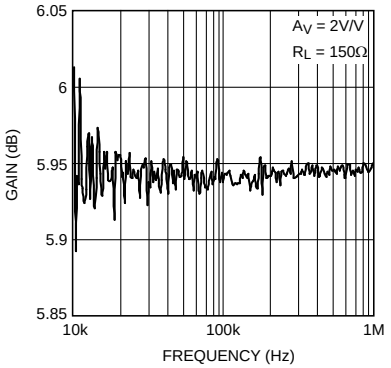
Small Signal Gain Peaking



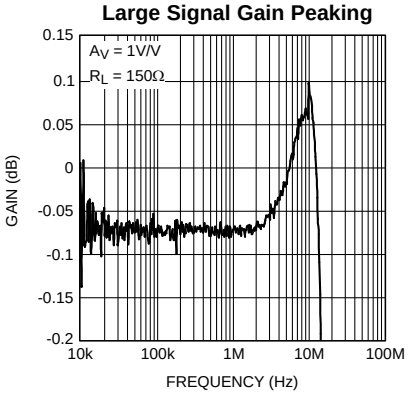
Large Signal Gain Flatness



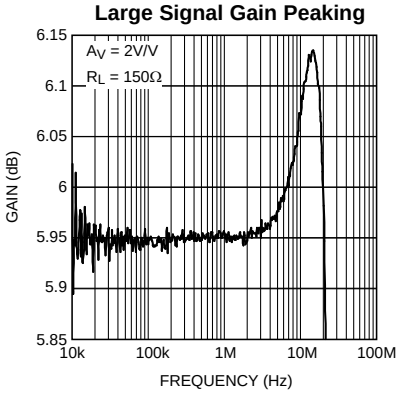
Large Signal Gain Flatness



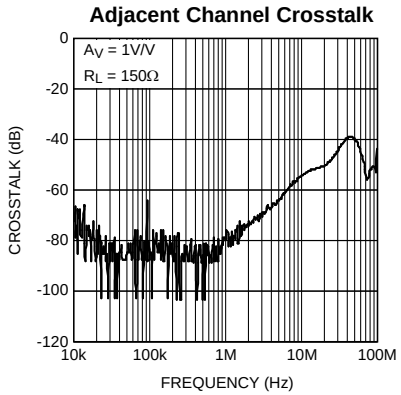
Large Signal Gain Peaking



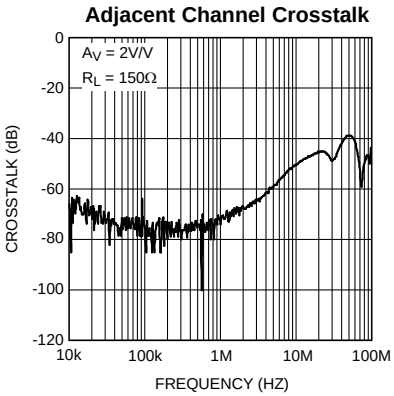
Large Signal Gain Peaking



Adjacent Channel Crosstalk



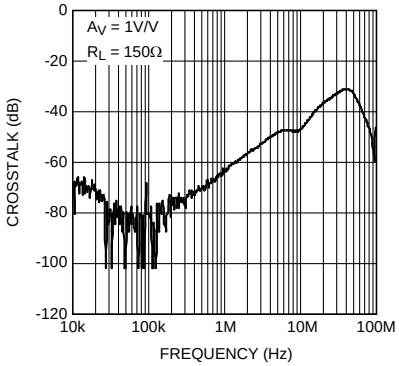
Adjacent Channel Crosstalk



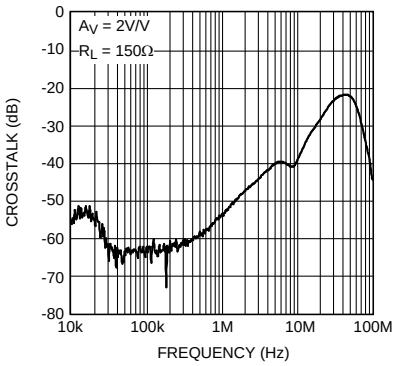
Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V_{DD} = 5V, R_{EXT} = 10 kΩ 1%, R_L = 150Ω, C_L = 12 pF. Small Signal Input Signal = 20 mV_{PP}, Medium Signal Input Signal = 200 mV_{PP} , Large Signal Input Signal = 750 mV_{PP}

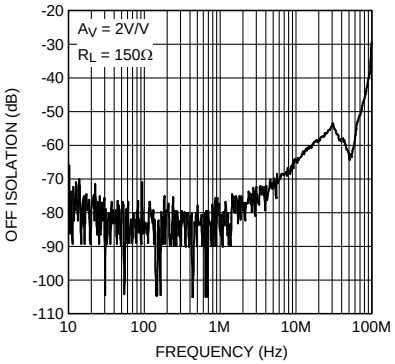
All Hostile Crosstalk



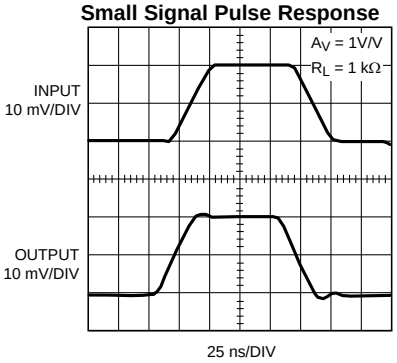
All Hostile Crosstalk



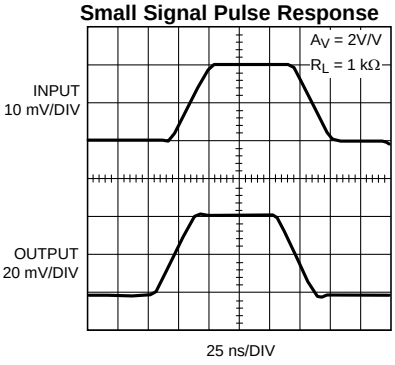
Off Isolation



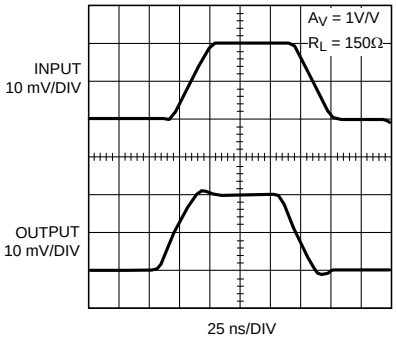
Small Signal Pulse Response



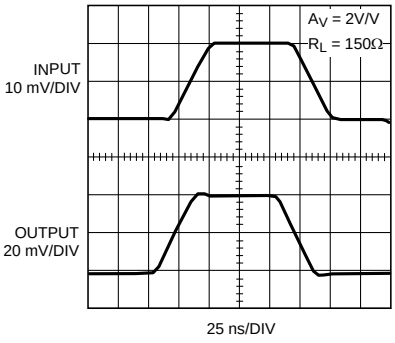
Small Signal Pulse Response



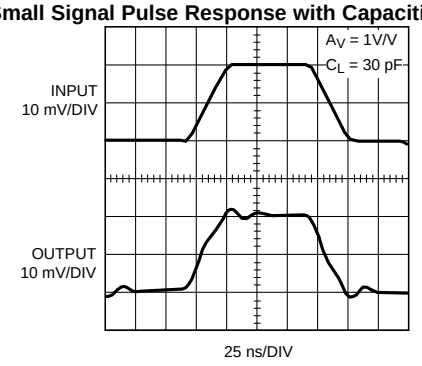
Small Signal Pulse Response



Small Signal Pulse Response



Small Signal Pulse Response with Capacitive Load



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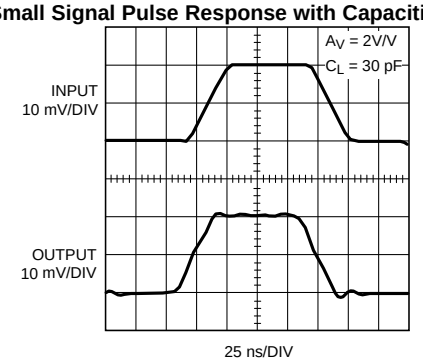
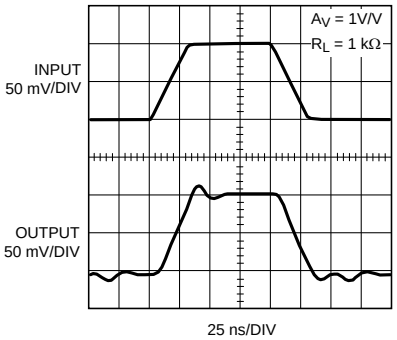
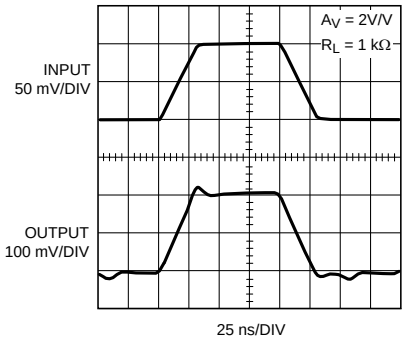
Small Signal Pulse Response with Capacitive Load



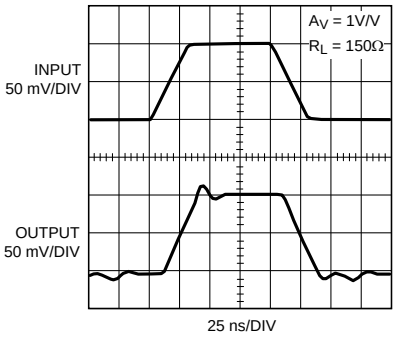
Medium Signal Pulse Response



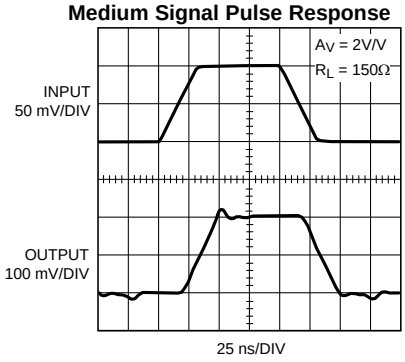
Medium Signal Pulse Response



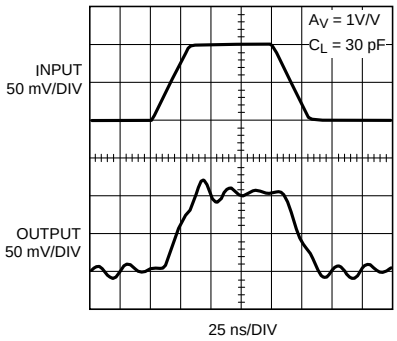
Medium Signal Pulse Response



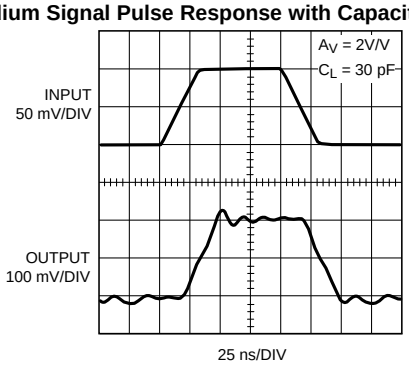
Medium Signal Pulse Response



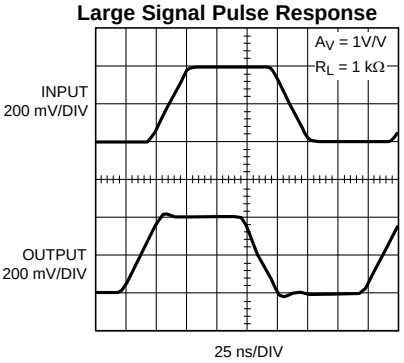
Medium Signal Pulse Response with Capacitive Load



Medium Signal Pulse Response with Capacitive Load



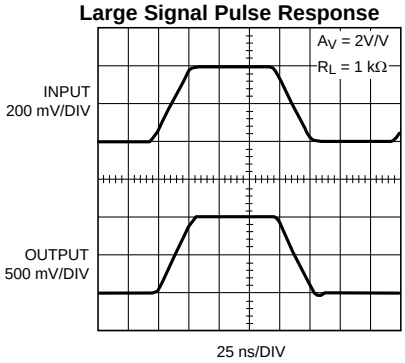
Large Signal Pulse Response



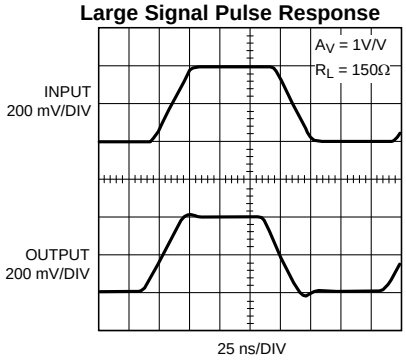
Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V_{DD} = 5V, R_{EXT} = 10 kΩ 1%, R_L = 150Ω, C_L = 12 pF. Small Signal Input Signal = 20 mV_{PP}, Medium Signal Input Signal = 200 mV_{PP} , Large Signal Input Signal = 750 mV_{PP}

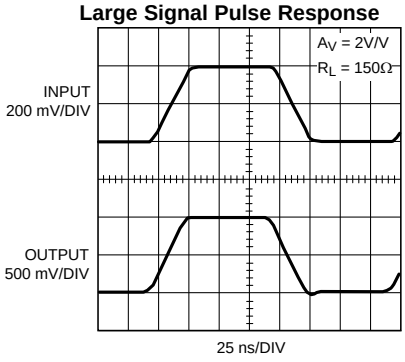
Large Signal Pulse Response



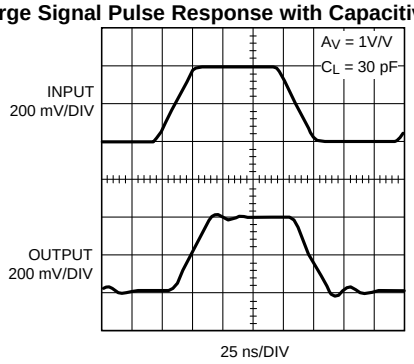
Large Signal Pulse Response



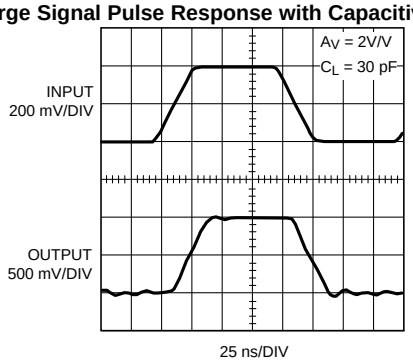
Large Signal Pulse Response



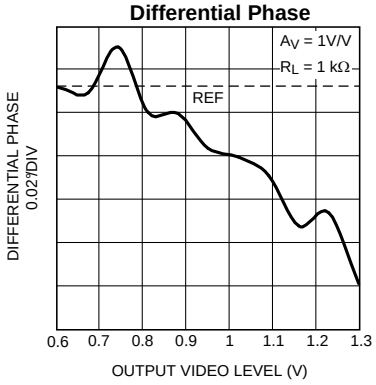
Large Signal Pulse Response with Capacitive Load



Large Signal Pulse Response with Capacitive Load

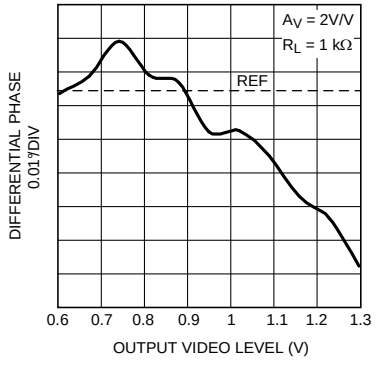


Differential Phase



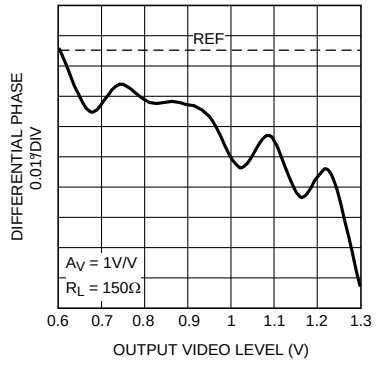
0.6V Output Level = 0 IRE
1.3V Output Level = 100 IRE

Differential Phase



0.6V Output Level = 0 IRE
1.3V Output Level = 100 IRE

Differential Phase

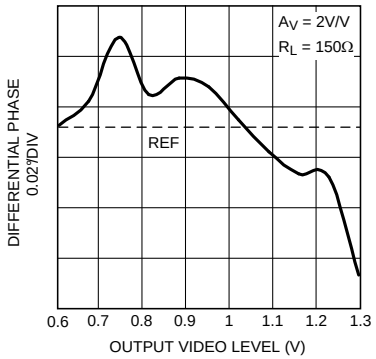


0.6V Output Level = 0 IRE
1.3V Output Level = 100 IRE

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V_{DD} = 5V, R_{EXT} = 10 kΩ 1%, R_L = 150Ω, C_L = 12 pF. Small Signal Input Signal = 20 mV_{PP}, Medium Signal Input Signal = 200 mV_{PP} , Large Signal Input Signal = 750 mV_{PP}

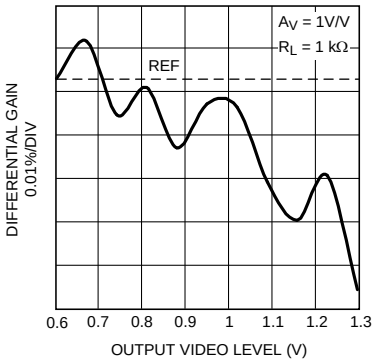
Differential Phase



0.6V Output Level = 0 IRE

1.3V Output Level = 100 IRE

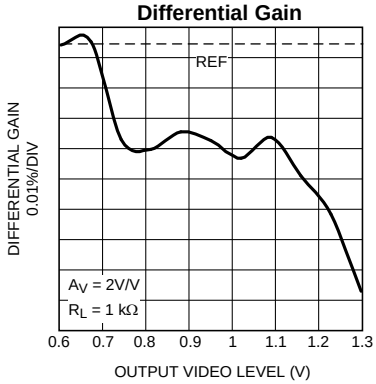
Differential Gain



0.6V Output Level = 0 IRE

1.3V Output Level = 100 IRE

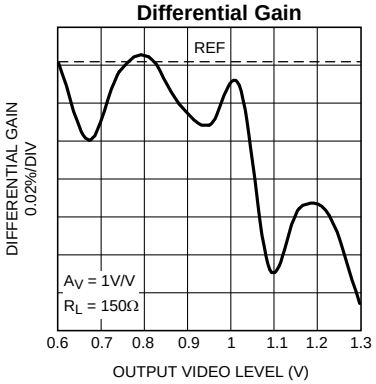
Differential Gain



0.6V Output Level = 0 IRE

1.3V Output Level = 100 IRE

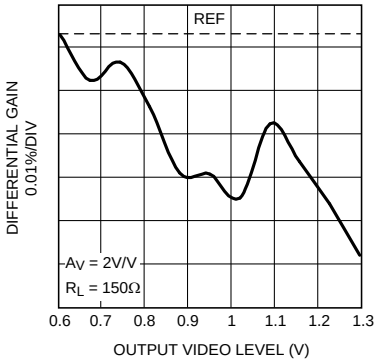
Differential Gain



0.6V Output Level = 0 IRE

1.3V Output Level = 100 IRE

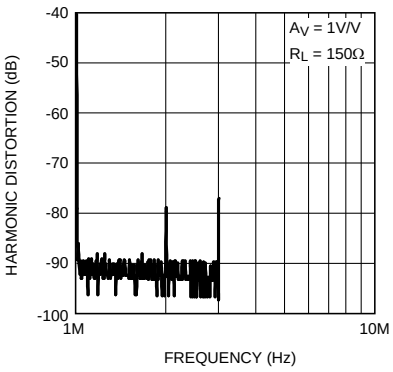
Differential Gain



0.6V Output Level = 0 IRE

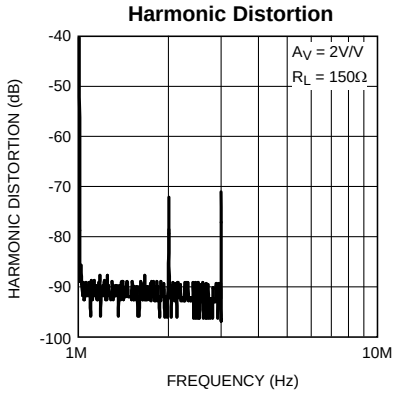
1.3V Output Level = 100 IRE

Harmonic Distortion



Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V_{DD} = 5V, R_{EXT} = 10 kΩ 1%, R_L = 150Ω, C_L = 12 pF. Small Signal Input Signal = 20 mV_{PP}, Medium Signal Input Signal = 200 mV_{PP} , Large Signal Input Signal = 750 mV_{PP}



Application Information

FUNCTIONAL OVERVIEW

The LMH6586 is a non-blocking analog video crosspoint switch with 32 input channels and 16 output channels. The inputs have integrated DC restore clamp circuits for biasing the AC-coupled video inputs. The fully buffered outputs have selectable gain and can drive one back-terminated video load (150Ω). The LMH6586 includes an extra output (VOUT_16) with 1X fixed gain that can be used to feed any input's video signal to an external video sync separator, such as the LMH1980 or LMH1981.

Each input and each output can be individually placed in shutdown mode by programming the input shutdown and output shutdown registers, respectively. Additionally, the PWDN pin (pin 70) can be set high to enable Power Down mode, which shuts down all input and output video channels while preserving all register settings.

The LMH6586 also features both video detection and sync detection functions on each input channel. Additional flexibility is provided by user-defined threshold levels for both video and sync detection features. The status of both detection schemes can be read from the video and sync detection status registers. Additionally, the FLAG output (pin 75) can be used to indicate if video detection or sync detection is triggered on any combination of input channels and detection types enabled by the user.

OUTPUT BUFFER GAIN

The LMH6586 has an output buffer with a selectable gain of 1X or 2X. When the GAIN_SEL input (pin 61) is set low, output channels 0–15 will have a gain of 1X. When it is set high, they will have a gain of 2X. Regardless of the gain select setting, output channel 16 has 1X fixed gain since the output is intended to drive an optional external sync separator through a 0.1 µF capacitor and no load termination.

VIDEO DETECTION

This type of detection can be configured to indicate when an input's video signal is detected above the threshold level (“presence of video”) or below the threshold level (“loss of video”). The video threshold voltage level is common to all 32 input channels and is selectable by programming register 0x1D. As shown in Table 1, the three LSBs (bits 2:0) of this register can be used to set the threshold level in 95 mV steps (typical) above to the sync tip level of the DC-restored input. Additionally, to prevent undesired triggering on high-frequency picture content, such as on-screen display (OSD) or text, the detection circuit actually analyzes a low-pass-filtered version of the video signal. The first-order RC filter is included on-chip and has a corner frequency of about 1 kHz.

Registers 0x04 to 0x07 (read-only) contain the video detection status bits for all 32 input channels. Any input (m) has a video detection status bit (VD_m) that can flag high when either loss of video or presence of video is detected, depending on the respective invert control bit. Registers 0x0C to 0x0F contain the video detection invert control bits for all input channels. When the invert bit (VD_INV_m) is set to 0 (default setting), the respective status bit (VD_m) will flag high when loss of video is detected on the input; otherwise, when the invert bit is set to 1, the status bit will flag high when presence of video is detected.

Table 1. Video Detect Threshold Voltage*

Register 0x1D [2:0]			Threshold level above the sync tip level
0	0	0	491 mV
0	0	1	587 mV
0	1	0	683 mV
0	1	1	778 mV
1	0	0	873 mV
1	0	1	968 mV
1	1	0	1062 mV
1	1	1	1156 mV

The following example illustrates a practical use of video detection in a real-world system. A bank's ATM surveillance system could consist of a video camera, a LMH6586 crosspoint switch, a video recorder, and control system. When no one is using the ATM, the area being monitored by the camera could have strong backlighting, so the camera would output a normally high video level. When a person approaches the area, most of the backlighting would be blocked by the person and cause a measurable decrease in the video level. This change in camera's video level could be detected by the LMH6586, which could then flag the security system to begin recording of the activity. Once the person leaves the area, the LMH6586 could clear the flag.

SYNC DETECTION

The LMH6586 also features a sync detection circuit that can indicate when an input's negative-going sync pulse is not detected below the threshold level (“loss of sync”). The sync threshold voltage level is common to all 32 input channels and is defined by the bias voltage on the VREF_SYNC input (pin 65), which may be set using a simple voltage divider circuit. The recommended voltage level at the VREF_SYNC pin is 350 mV to ensure proper operation.

Registers 0x00 to 0x03 (read-only) contain the sync detection status bits for all 32 input channels. Any input (m) has a sync detection status bit (SD_m) that can flag high when a loss of sync is detected; otherwise, the status bit will be low to indicate presence of sync.

DETECTION FLAG OUTPUT

The FLAG output (pin 75) can flag high if either video detection or sync detection is triggered based on the user-defined enable settings for the video and sync detection status bits. Any of the input's video detection status bits (VD_m) and sync detection status bits (SD_m) can be logically OR-ed into this single FLAG output pin. Registers 0x10 to 0x13 contain the video detection enable bits and registers 0x14 to 0x17 contain the sync detection enable bits for all input channels. Any input (m) has both a video detection enable bit (VD_EN_m) and a sync detection enable bit (SD_EN_m). When any enable bit is set low, the respective status bit will be excluded from the OR-ing function used to set the FLAG output; otherwise, when the enable bit is set high, the respective status bit will be included in the FLAG output function. Therefore, the FLAG will only logical-OR the status bits of the channel(s) and type(s) of detection that are specifically enabled by the user.

SWITCH MATRIX

The LMH6586 uses 512 CMOS analog switches to form a 32 x 16 crosspoint switch. The LMH6586 is a non-blocking crosspoint switch which means that any one of the 32 inputs can be routed to any of the 16 outputs. The switch can only be configured by programming through the I^2C bus interface.

DC RESTORATION

Because the LMH6586 uses a single 5V supply and typical composite video signals contain signal components both above and below 0V (video blanking level), proper input signal biasing is required to ensure the video signal is within the operating range of the amplifier. To simplify the external biasing circuitry, each input of the LMH6586 has a dedicated DC restore clamp circuit to allow AC-coupled input operation using a 0.1 uF coupling capacitor. Please refer to AC COUPLING for details on how the coupling capacitor value was determined.

AC COUPLING

Each video input uses an integrated DC restore clamp circuit to servo the sync tip of the AC-coupled video input signal to the DC voltage received at the VREF_CLAMP input (pin 66). For proper AC-coupled operation, the LMH6586 requires video signals with negative sync pulses. The VREF_CLAMP level can be set in range of 300 mV to 1.0V using a voltage divider network. For optimum performance and reduced power consumption, it is recommended to set VREF_CLAMP to 300 mV. Therefore, assuming a video input amplitude of $1V_{PP}$, the bottom of the sync tip level would be clamped to 300 mV above ground and the peak white video level would be at 1.3V.

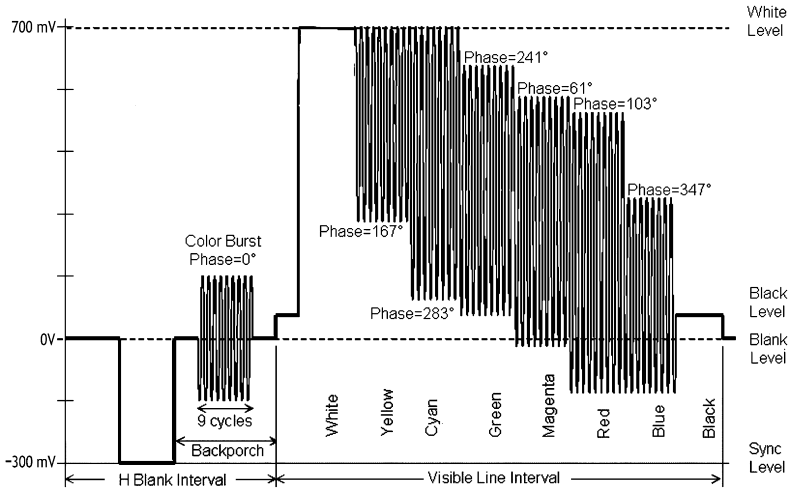


Figure 3. Input Video Signal Before DC Restore Clamp

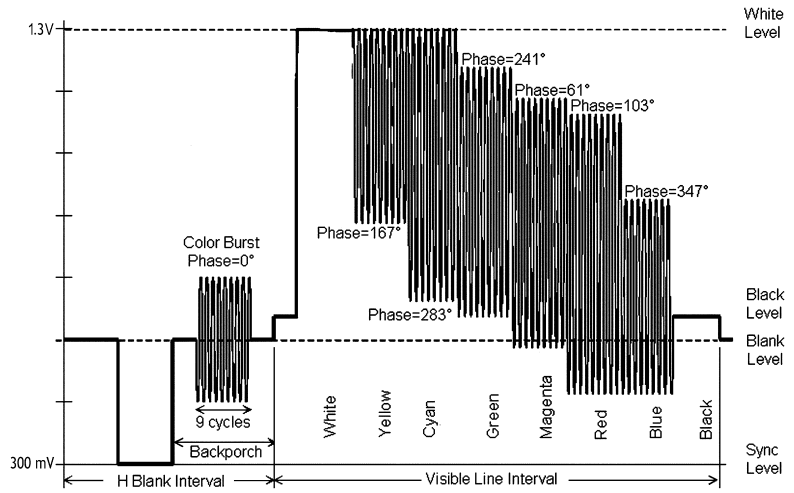


Figure 4. Input Video Signal After DC Restore Clamp

The equivalent DC restore clamp circuit is shown below.

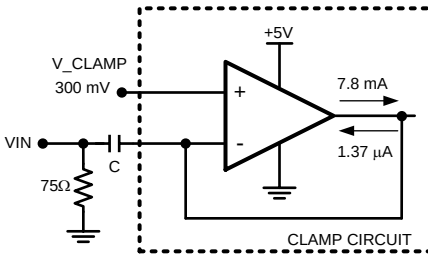


Figure 5. Clamp Circuit

Typically the clamp voltage is set to 300 mV. During the sync pulse period, the clamp circuit amplifier sources current and the coupling capacitor will not discharge. However, during the active video period, the clamp amplifier will sink current and cause the coupling capacitor to discharge through the 75Ω resistor. To limit this discharge to an acceptable value we must choose an appropriate value of the AC coupling capacitor. The value of the AC coupling capacitor can be calculated as follows:

Cap Discharge Time T = Line Period – Sync Period

T = 63.5 µs – 4.7 µs

T= 58.8 µs

Discharge current I = 1.37 µA

Charge Q = I*T

Q = 1.37 µA * 58.8 µs

Q = 80.55 pC

Q = C*V

C = Q/V

Typical acceptable voltage drop V = 0.1% of 700 mV

V = 0.7 mV

Capacitor Value C = 80.55 pC/ 0.7 mV

C = 0.115 µF

Thus the suggested AC coupling capacitor value is 0.1 µF. A larger value will reduce line droop at the expense of longer input settling time.

VIDEO INPUTS AND OUTPUTS

The LMH6586 has 32 inputs which accept standard NTSC or PAL composite video signals. The input video signal should be AC coupled through a 0.1 µF coupling capacitor for proper operation. Each input is buffered before the switch matrix, which provides high input impedance. Input buffering enables any single output to be broadcasted to all 16 outputs at a time without loading of the input source. Each input buffer can be individually shut down using the input shutdown registers. When shutdown the input buffers are high impedance, which reduces power consumption and crosstalk.

The LMH6586 has 16 video outputs each of which is buffered through a programmable 1X or 2X gain output buffer. The outputs are capable of driving 150Ω loads. When the output gain is set to 1X (GAIN_SEL = 0), the output signal sync tip is set to the VREF_CLAMP voltage level; otherwise, when the gain is set to 2X (GAIN_SEL = 1), the output signal sync tip is set to twice the VREF_CLAMP level. Each output can be individually shut down using the output shutdown registers. When shutdown the outputs are high impedance, which reduces power consumption and crosstalk, and also enables multiple outputs to be connected together for expanding the matrix array size. Note that output short circuit protection is not provided, so care must be taken to ensure only one output is active when output channels are tied together in expansion configurations.

INPUT EXPANSION

The LMH6586 has the capability for creating larger switching matrices. Depending on the number of input and output channels required, the number of devices required can be calculated. To implement a 128 x 16 non-blocking matrix arrange the building blocks in a grid. The inputs are connected in parallel while the outputs are wired-or together. When using this configuration care must be taken to ensure that only one of the four outputs is active. The other three outputs should be placed in shutdown mode by using the appropriate shutdown bit in the output shutdown registers. This reduces output loading and the risk of output short circuit conditions, which can lead to device overheating and even damage to the channel or device.

The figure below shows the 128 input x 16 output switching matrix using four LMH6586 devices. To construct larger matrices use the same technique with more devices.

Because the LMH6586 has 2-bit configurable slave address inputs, up to four LMH6586 devices can be connected to a common I^2C bus. For more devices additional I^2C buses may be required.

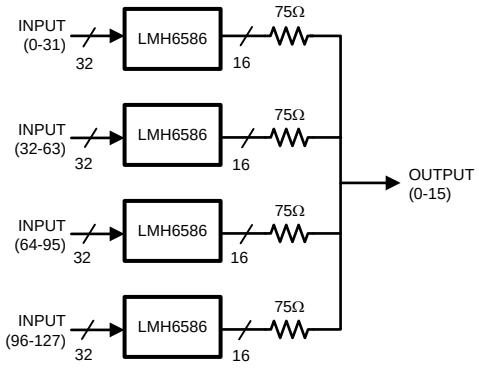


Figure 6. 128 x 16 Crosspoint Array

DRIVING CAPACITIVE LOAD

When many outputs are wired together, as in the case of expansion, each output buffer sees the normal load impedance as well as the impedance the other shutdown outputs. This impedance has a resistive and a capacitive component. The resistive components reduce the total effective load for the driving output. Total capacitance is the sum of the capacitance of all the outputs and depends on the size of the matrix. As the size of the matrix increases, the length of the PC board traces also increases, adding more capacitance. The output buffers have been designed to drive more than 30 pF of capacitance while still maintaining a good AC response. If the output capacitance exceeds this amount then the AC response will be degraded. To prevent this, one option is to reduce the number of output wired-or together by using more LMH6586 device. Another option is to put a resistor in series with the output before the capacitive load to limit excessive ringing and oscillations.

A low pass filter is created from the series resistor (R) and parasitic capacitance (C) to ground. A single R-C does not affect the performance at video frequencies, however, in large system, there may be many such R-Cs cascaded in series. This may result in high frequency roll-off resulting in “softening of the picture”. There are two solutions to improve performance in this case. One way is to design the PC board traces with some inductance between the R and C elements. By routing the traces in a repeating “S” configuration, the traces that are nearest each other will exhibit a mutual inductance increasing the total inductance. This series inductance causes the amplitude response to increase or peak at higher frequencies, offsetting the roll-off from the parasitic capacitance. Another solution is to add a small-value inductor between the R and C elements to add peaking to the frequency response.

THERMAL MANAGEMENT

The LMH6586 operates on a 5V supply and draws a load current of approximately 300 mA. Thus it dissipates approximately 1.75W of power. In addition, each equivalent video load (150Ω) connected to the outputs should be budgeted 30 mW of power consumption.

The following calculations show the thermal resistance, θ_{JA}, required, to ensure safe operation and to prevent exceeding the maximum junction temperature, given the maximum power dissipation.

$$P_{DMAX} = (T_{JMAX} - T_{AMAX})/\theta_{JA} \quad (1)$$

Where:

- T_{JMAX} = Maximum junction temperature = 150°C
- T_{AMAX} = Maximum ambient temperature = +85°C
- θ_{JA} = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or:

$$P_{DMAX} = V_S \times I_{SMAX} + \sum_{i=1}^{n} (V_S - V_{OUTi}) \times \frac{V_{OUTi}}{R_{Li}} \quad (2)$$

Where:

- V_S = Supply voltage = 5V
- I_{SMAX} = Maximum quiescent supply current = 300 mA
- V_{OUT} = Maximum output voltage of the application = 2.6V
- R_L = Load resistance tied to ground = 150Ω
- n = 1 to 16 channels

Calculating :

P_{DMAX} = 2.2656

The required θ_{JA} to dissipate P_{DMAX} is = $(T_{JMAX} - T_{AMAX})/P_{DMAX}$

The table below shows the θ_{JA} values with airflow and different heatsinks.

LMH6586VS 80-Pin TQFT LMHXPT Analog Video Crosspoint Board	**0 LFPM @ 0.50 watt**	**0 LFPM @ 1.0 watt**	**0 LFPM @ 2.0 watt**	**0 LFPM @2.8 watt**	**225 LFPM @ 2.8 watt**	**500 LFPM @ 2.8 watt**
NO Heat Sink	32.2	30.9	29.4	28.6	26.8	25.3
Small Tower x y = 9.57x9.69 mm/ht. 6.28 mm	25.5	24.6	23.6	22.9	19.2	15.9
Aluminum 12 rail x y = 9.82x10.73 mm/ht.10.07 mm	25.2	24.1	23.0	22.2	16.4	14.2
Anodized 9 rail x y = 6.10x7.30 mm/ht. 13.67 mm	24.4	23.3	22.1	21.3	15.6	13.6
Round Tower diameter = 14.35 mm/ht. 4.47 mm	24.2	23.9	22.9	22.4	18.2	15.4

REXT RESISTOR

The REXT external resistor (pin 67) establishes the internal bias current and precise reference voltage for the LMH6586. For optimal performance, REXT should be a 10 kΩ 1% precision resistor with a low temperature coefficient to ensure proper operation over a wide temperature range. Using a REXT resistor with less precision may result in reduced performance against temperature, supply voltage, input signal, or part-to-part variations.

SYNC SEPARATOR OUTPUT

In addition to the 16 video outputs, the LMH6586 has an extra output (V_OUT16) which can select any input channel. This channel's output buffer only has a gain of 1 since it is not meant to drive a 150Ω video load. Instead, this video output can be AC coupled to a non-terminated input of an external video sync separator, such as National's LMH1980 or LMH1981. The sync separator can extract the synchronization (sync) timing signals, which can be useful for video triggering or phase-locked loop (PLL) clock generation circuits. Refer to the LMH1980 or LMH1981 datasheet for more information about these sync separator devices.

I²C INTERFACE

A microcontroller can be used to configure the LMH6586 via the I²C interface. The protocol of the interface begins with a start pulse followed by a byte comprised of a seven-bit slave device address and a read/write bit as the LSB. The two lowest bits of the seven-bit slave address are defined by the external connections of inputs ADDR[1] (pin 72) and ADDR[0] (pin 71), where ADDR[0] is the least significant bit. Because there are four different combinations of the two ADDR pins, it's possible to have up to four different LMH6586 devices with unique slave addresses on a common I²C bus. See *I²C Device Slave Address Lookup Table*.

Table 2. I²C Device Slave Address Lookup Table

ADDR[1] (pin 72)	ADDR[0] (pin 71)	7-bit I²C Slave Address (binary)
0	0	0000 000x
0	1	0000 001x
1	0	0000 010x
1	1	0000 011x

For example, if ADDR[1] is set low and ADDR[0] is set high, then the 7-bit slave address would be “0000 0**01**” in binary. Therefore, the address byte for write sequences is 0x02 (“0000 0010”) and the address byte read sequences is 0x03 (“0000 0011”). Figure 7 and Figure 8 show write and read sequences across the I²C interface.

WRITE SEQUENCE

The write sequence begins with a start condition, which consists of the master pulling SDA low while SCL is held high. The slave device address is sent next. The address byte is made up of an address of seven bits (7:1) and the read/write bit (0). Bit 0 is low to indicate a write operation. Each byte that is sent is followed by an acknowledge (ACK) bit. When SCL is high the master will release the SDA line. The slave must pull SDA low to acknowledge. The address of the register to be written to is sent next. Following the register address and the ACK bit, the data byte for the register is sent. When more than one data byte is sent, the register pointer is automatically incremented to write to the next address location. Note that each data byte is followed by an ACK bit until a stop condition is encountered, indicating the end of the sequence.

The timing diagram for the write sequence is shown in Figure 7, which uses the 7-bit slave device address from the previous example above.

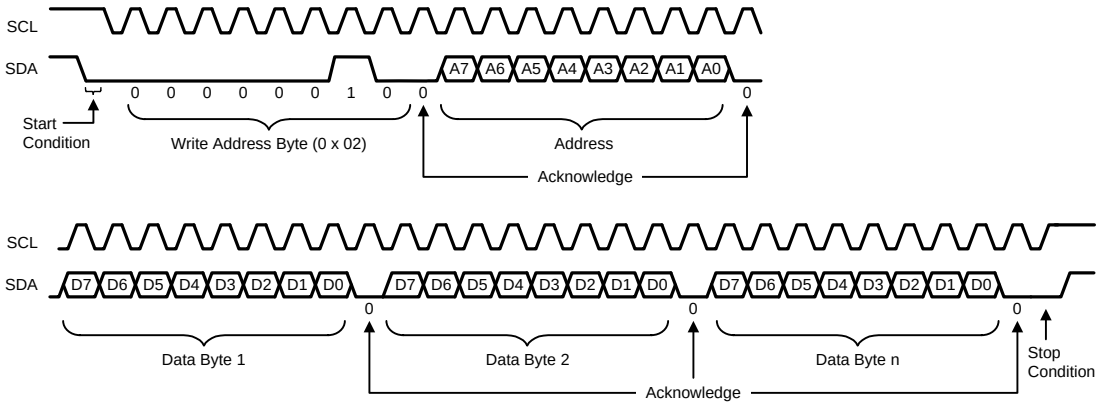


Figure 7. LMH6586 Write Sequence

READ SEQUENCE

Read sequences are comprised of two I²C transfers shown. The first is the address access transfer, which consists of a write sequence that transfers only the address to be accessed. The second is the data read transfer, which starts at the address accessed in the first transfer and increments to the next address per data byte read until a stop condition is encountered.

The address access transfer consists of a start condition, the slave device address including the read/write bit (a zero, indicating a write), and the ACK bit. The next byte is the address to be accessed, followed by the ACK bit and the stop condition to indicate the end of the address access transfer.

The subsequent read data transfer consists of a start condition, the slave device address including the read/write bit (a one, indicating a read), and the ACK bit. The next byte is the data read from the initial access address. Subsequent read data bytes will correspond to the next increment address locations. Note that each data byte is followed by an ACK bit until a stop condition is encountered, indicating the end of the sequence.

The timing diagram for the read sequence is shown in Figure 8, which uses the 7-bit slave address from the previous examples.

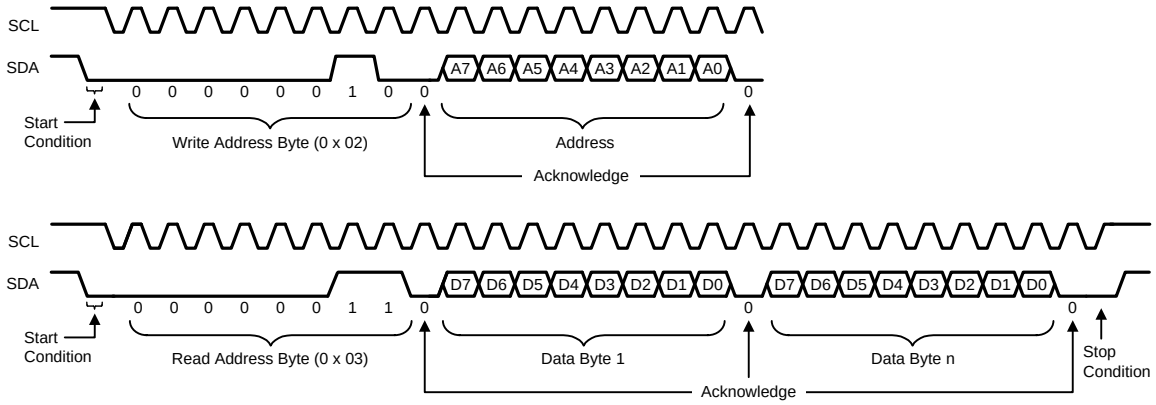


Figure 8. LMH6586 Read Sequence

REGISTER DESCRIPTIONS

Video and Sync Detection Status Registers

Registers 0x00 to 0x03 (read-only) contain the sync detection status bits for all 32 input channels. Any input (m) has a sync detection status bit (SD_m) that can flag high when a loss of sync is detected; otherwise, the status bit will be low to indicate presence of sync.

Registers 0x04 to 0x07 (read-only) contain the video detection status bits for all 32 input channels. Any input (m) has a video detection status bit (VD_m) that can flag high when either loss of video or presence of video is detected, depending on the respective invert control bit (see Video Detection Invert Registers:). Assuming the default setting for the invert control bit, the status bit (VD_m) will flag high when loss of video is detected on the input; otherwise, the status bit will be low indicating presence of video.

Video and Sync Detection Control Registers

Video Detection Invert Registers:

Registers 0x0C to 0x0F contain the video detection invert control bits for all input channels. Any input (m) has a invert control bit that can invert the polarity of the video detection status bit (VD_INV_m). When the invert bit (VD_INV_m) is set to 0 (default), the respective status bit (VD_m) will flag high to indicate loss of video on the input; otherwise, when the invert bit is set to 1, the status bit will flag high to indicate presence of video.

Video and Sync Detection Enable Registers:

Registers 0x10 to 0x13 contain the video detection enable bits and registers 0x14 to 0x17 contain the sync detection enable bits for all input channels. Any input (m) has both a video detection enable bit (VD_EN_m) and a sync detection enable bit (SD_EN_m). When any enable bit is set low, the respective status bit will be excluded from the OR-ing function used to set the FLAG output; otherwise, when the enable bit is set high, the respective status bit will be included in the FLAG output function. Therefore, the FLAG will only logical-OR the status bits of the channel(s) and type(s) of detection that are specifically enabled by the user as described in DETECTION FLAG OUTPUT.

Video Detection Threshold Control Register

The video threshold voltage level is common to all 32 input channels and is selectable by programming VDT[2:0] in register 0x1D. As shown in Table 1, the three LSBs (bits 2:0) of this register can be used to set the threshold level in 95 mV steps (typical) above to the sync tip level of the DC-restored input. Refer to VIDEO DETECTION for more information.

Input and Output Shutdown Registers

Each input channel and each output channel can be individually placed in shutdown (power save) mode to reduce power consumption. Registers 0x18 to 0x1B contain the input shutdown bits (IN_PS_m) and registers 0x1E and 0x1F contain the output shutdown bits (OUT_PS_n), where “m” is any input channel and “n” is any output channel. To place any input or output channel in shutdown mode, the respective bit should be set high; otherwise, it should be set low for normal input or output operation. When in shutdown mode, the buffer (input or output) will be placed in a high-impedance state.

Note: To put the entire device in power save mode, the PWDN input (pin 70) should be set high; otherwise, it should be set low for normal operation.

Video Input Selection Registers

Registers 0x20 to 0x30 are used to control the routing of the crosspoint switch. Each output has a dedicated input selection register, which can be programmed to select any input channel for routing to its respective output.

LMH6586 REGISTER MAP

Table 3. Video and Sync Detection Status Registers

Register	Address	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SYNC DETECT OUT (CH 0-7)	0x00h	R		SD_7	SD_6	SD_5	SD_4	SD_3	SD_2	SD_1	SD_0
SYNC DETECT OUT (CH 8-15)	0x01h	R		SD_15	SD_14	SD_13	SD_12	SD_11	SD_10	SD_9	SD_8
SYNC DETECT OUT (CH 16-23)	0x02h	R		SD_23	SD_22	SD_21	SD_20	SD_19	SD_18	SD_17	SD_16
SYNC DETECT OUT (CH 24-31)	0x03h	R		SD_31	SD_30	SD_29	SD_28	SD_27	SD_26	SD_24	SD_24
VIDEO DETECT OUT (CH 0-7)	0x04h	R		VD_7	VD_6	VD_5	VD_4	VD_3	VD_2	VD_1	VD_0
VIDEO DETECT OUT (CH 8-15)	0x05h	R		VD_15	VD_14	VD_13	VD_12	VD_11	VD_10	VD_9	VD_8
VIDEO DETECT OUT (CH 16-23)	0x06h	R		VD_23	VD_22	VD_21	VD_20	VD_19	VD_18	VD_17	VD_16
VIDEO DETECT OUT (CH 24-31)	0x07h	R		VD_31	VD_30	VD_29	VD_28	VD_27	VD_26	VD_24	VD_24

Table 4. Video and Sync Detection Control Registers

Register	Address	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED	0x08h 0x0Bh	R/W	0x00	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV
VIDEO DETECT INVERT (CH 0-7)	0x0Ch	R/W	0x00	VD_ INV_7	VD_ INV_6	VD_ INV_5	VD_ INV_4	VD_ INV_3	VD_ INV_2	VD_ INV_1	VD_ INV_0
VIDEO DETECT INVERT (CH 8-15)	0x0Dh	R/W	0x00	VD_ INV_15	VD_ INV_14	VD_ INV_13	VD_ INV_12	VD_ INV_11	VD_ INV_10	VD_ INV_9	VD_ INV_8
VIDEO DETECT INVERT (CH 16-23)	0x0Eh	R/W	0x00	VD_ INV_23	VD_ INV_22	VD_ INV_21	VD_ INV_20	VD_ INV_19	VD_ INV_18	VD_ INV_17	VD_ INV_16
VIDEO DETECT INVERT (CH 24-31)	0x0Fh	R/W	0x00	VD_ INV_31	VD_ INV_30	VD_ INV_29	VD_ INV_28	VD_ INV_27	VD_ INV_26	VD_ INV_24	VD_ INV_24
SYNC DETECT ENABLE (CH 0-7)	0x10h	R/W	0x00	SD_ EN_7	SD_ EN_6	SD_ EN_5	SD_ EN_4	SD_ EN_3	SD_ EN_2	SD_ EN_1	SD_ EN_0

Table 4. Video and Sync Detection Control Registers (continued)

Register	Address	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SYNC DETECT ENABLE (CH 8-15)	0x11h	R/W	0x00	SD_EN_15	SD_EN_14	SD_EN_13	SD_EN_12	SD_EN_11	SD_EN_10	SD_EN_9	SD_EN_8
SYNC DETECT ENABLE (CH 16-23)	0x12h	R/W	0x00	SD_EN_23	SD_EN_22	SD_EN_21	SD_EN_20	SD_EN_19	SD_EN_18	SD_EN_17	SD_EN_16
SYNC DETECT ENABLE (CH 24-31)	0x13h	R/W	0x00	SD_EN_31	SD_EN_30	SD_EN_29	SD_EN_28	SD_EN_27	SD_EN_26	SD_EN_25	SD_EN_24
VIDEO DETECT ENABLE (CH 0-7)	0x14h	R/W	0x00	VD_EN_7	VD_EN_6	VD_EN_5	VD_EN_4	VD_EN_3	VD_EN_2	VD_EN_1	VD_EN_0
VIDEO DETECT ENABLE (CH 8-15)	0x15h	R/W	0x00	VD_EN_15	VD_EN_14	VD_EN_13	VD_EN_12	VD_EN_11	VD_EN_10	VD_EN_9	VD_EN_8
VIDEO DETECT ENABLE (CH 16-23)	0x16h	R/W	0x00	VD_EN_23	VD_EN_22	VD_EN_21	VD_EN_20	VD_EN_19	VD_EN_18	VD_EN_17	VD_EN_16
VIDEO DETECT ENABLE (CH 24-31)	0x17h	R/W	0x00	VD_EN_31	VD_EN_30	VD_EN_29	VD_EN_28	VD_EN_27	VD_EN_26	VD_EN_25	SD_EN_24

Table 5. Video Detection Threshold Control Registers

Register	Address	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VIDEO DETECT THRESHOLD	0x1Dh	R/W	0x00	RSV					VDT[2:0]		

Table 6. Input and Output Shutdown Registers

Register	Address	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INPUT SHUTDOWN (CH 0-7)	0x18h	R/W	0x00	IN_PS_7	IN_PS_6	IN_PS_5	IN_PS_4	IN_PS_3	IN_PS_2	IN_PS_1	IN_PS_0
INPUT SHUTDOWN (CH 8-15)	0x19h	R/W	0x00	IN_PS_15	IN_PS_14	IN_PS_13	IN_PS_12	IN_PS_11	IN_PS_10	IN_PS_9	IN_PS_8
INPUT SHUTDOWN (CH 16-23)	0x1Ah	R/W	0x00	IN_PS_23	IN_PS_22	IN_PS_21	IN_PS_20	IN_PS_19	IN_PS_18	IN_PS_17	IN_PS_16
INPUT SHUTDOWN (CH 24-31)	0x1Bh	R/W	0x00	IN_PS_31	IN_PS_30	IN_PS_29	IN_PS_28	IN_PS_27	IN_PS_26	IN_PS_25	IN_PS_24
OUTPUT SHUTDOWN (CH 0-7)	0x1Eh	R/W	0x00	OUT_PS_7	OUT_PS_6	OUT_PS_5	OUT_PS_4	OUT_PS_3	OUT_PS_2	OUT_PS_1	OUT_PS_0
OUTPUT SHUTDOWN (CH 8-15)	0x1Fh	R/W	0x00	OUT_PS_15	OUT_PS_14	OUT_PS_13	OUT_PS_12	OUT_PS_11	OUT_PS_10	OUT_PS_9	OUT_PS_8

Table 7. Video Input Selection Registers

Register	Address	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CH 0 OUTPUT	0x20h	R/W	0x00	RSV			SELECTED INPUT CH[4:0]				
CH 1 OUTPUT	0x21h	R/W	0x00	RSV			SELECTED INPUT CH[4:0]				
CH 2 OUTPUT	0x22h	R/W	0x00	RSV			SELECTED INPUT CH[4:0]				
CH 3 OUTPUT	0x23h	R/W	0x00	RSV			SELECTED INPUT CH[4:0]				
CH 4 OUTPUT	0x24h	R/W	0x00	RSV			SELECTED INPUT CH[4:0]				
CH 5 OUTPUT	0x25h	R/W	0x00	RSV			SELECTED INPUT CH[4:0]				
CH 6 OUTPUT	0x26h	R/W	0x00	RSV			SELECTED INPUT CH[4:0]				
CH 7 OUTPUT	0x27h	R/W	0x00	RSV			SELECTED INPUT CH[4:0]				
CH 8 OUTPUT	0x28h	R/W	0x00	RSV			SELECTED INPUT CH[4:0]				
CH 9 OUTPUT	0x29h	R/W	0x00	RSV			SELECTED INPUT CH[4:0]				
CH 10 OUTPUT	0x2Ah	R/W	0x00	RSV			SELECTED INPUT CH[4:0]				
CH 11 OUTPUT	0x2Bh	R/W	0x00	RSV			SELECTED INPUT CH[4:0]				
CH 12 OUTPUT	0x2Ch	R/W	0x00	RSV			SELECTED INPUT CH[4:0]				

Table 7. Video Input Selection Registers (continued)

Register	Address	R/W	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CH 13 OUTPUT	0x2Dh	R/W	0x00	RSV			SELECTED INPUT CH[4:0]				
CH 14 OUTPUT	0x2Eh	R/W	0x00	RSV			SELECTED INPUT CH[4:0]				
CH 15 OUTPUT	0x2Fh	R/W	0x00	RSV			SELECTED INPUT CH[4:0]				
CH 16 OUTPUT (extra)	0x30h	R/W	0x00	RSV			SELECTED INPUT CH[4:0]				

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
LMH6586VS/NOPB	ACTIVE	TQFP	PFC	80	119	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
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OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

MTQF009A – OCTOBER 1994 – REVISED DECEMBER 1996

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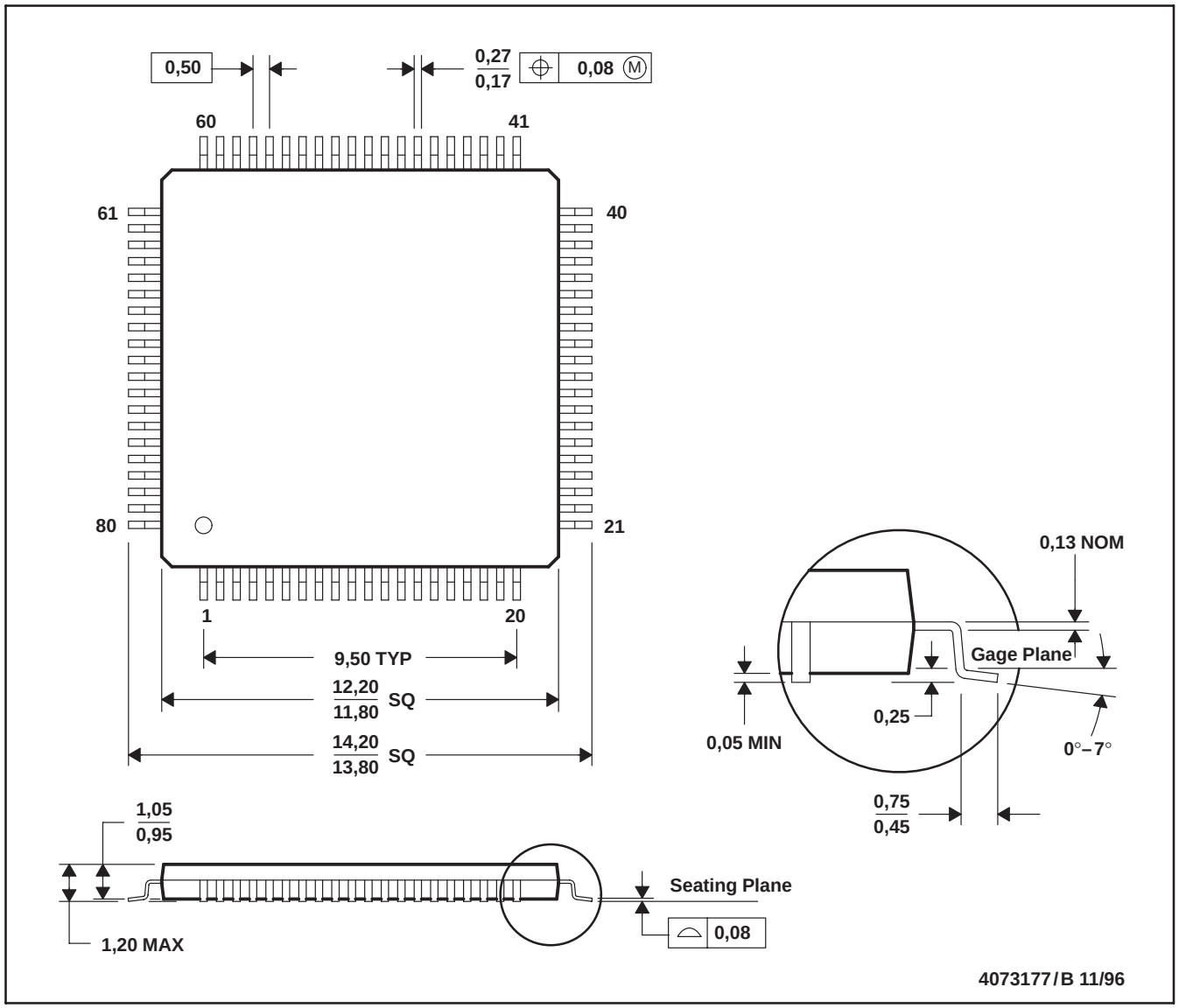

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
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