LM98714 Three Channel, 16-Bit, 45 MSPS Digital Copier Analog Front End with Integrated CCD/CIS Sensor Timing Generator and LVDS Output

Check for Samples: LM98714

FEATURES

- **LVDS/CMOS Outputs**
- **LVDS/CMOS Pixel Rate Input Clock or ADC Input Clock**
- **CDS or S/H Processing for CCD or CIS Sensors**
- **Independent Gain/Offset Correction for Each Channel**
- **Digital Black Level Correction Loop for Each Channel**
- **Programmable Input Clamp Voltage**
- **Flexible CCD/CIS Sensor Timing Generator**

APPLICATIONS

- **Multi-Function Peripherals**
- **Facsimile Equipment**
- **Flatbed or Handheld Color Scanners**
- **High-Speed Document Scanner**

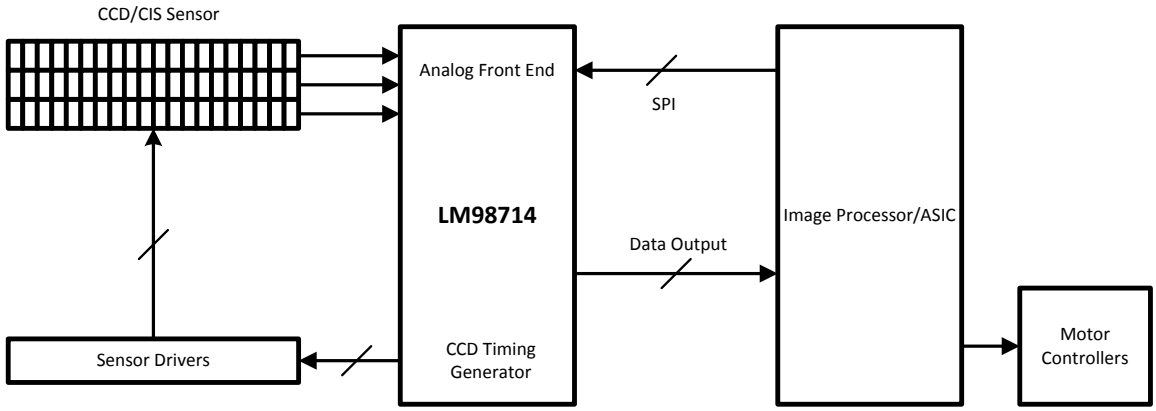
KEY SPECIFICATIONS

- **Maximum Input Level 1.2 or 2.4 Volt Modes**
  - **(Both with + or - Polarity Option)**
- **ADC Resolution 16-Bit**
- **ADC Sampling Rate 45 MSPS**
- **INL +/- 23 LSB (typ)**
- **Channel Sampling Rate 15/22.5/30 MSPS**
- **PGA Gain Steps 256 Steps**
- **PGA Gain Range 0.7 to 7.84x**
- **Analog DAC Resolution +/-9 Bits**
- **Analog DAC Range +/-300mV or +/-600mV**
- **Digital DAC Resolution +/-6 Bits**
- **Digital DAC Range -1024 LSB to + 1008 LSB**
- **SNR -74dB (@0dB PGA Gain)**
- **Power Dissipation 505mW (LVDS) 610mW (CMOS)**
- **Operating Temp 0 to 70°C**
- **Supply Voltage 3.3V Nominal (3.0V to 3.6V Range)**

DESCRIPTION

The LM98714 is a fully integrated, high performance 16-Bit, 45 MSPS signal processing solution for digital color copiers, scanners, and other image processing applications. High-speed signal throughput is achieved with an innovative architecture utilizing Correlated Double Sampling (CDS), typically employed with CCD arrays, or Sample and Hold (S/H) inputs (for Contact Image Sensors and CMOS image sensors). The signal paths utilize 8 bit Programmable Gain Amplifiers (PGA), a +/-9-Bit offset correction DAC and independently controlled Digital Black Level correction loops for each input. The PGA and offset DAC are programmed independently allowing unique values of gain and offset for each of the three inputs. The signals are then routed to a 45MHz high performance analog-to-digital converter (ADC). The fully differential processing channel shows exceptional noise immunity, having a very low noise floor of -74dB. The 16-bit ADC has excellent dynamic performance making the LM98714 transparent in the image reproduction chain.

System Block Diagram



LM98714 Overall Chip Block Diagram

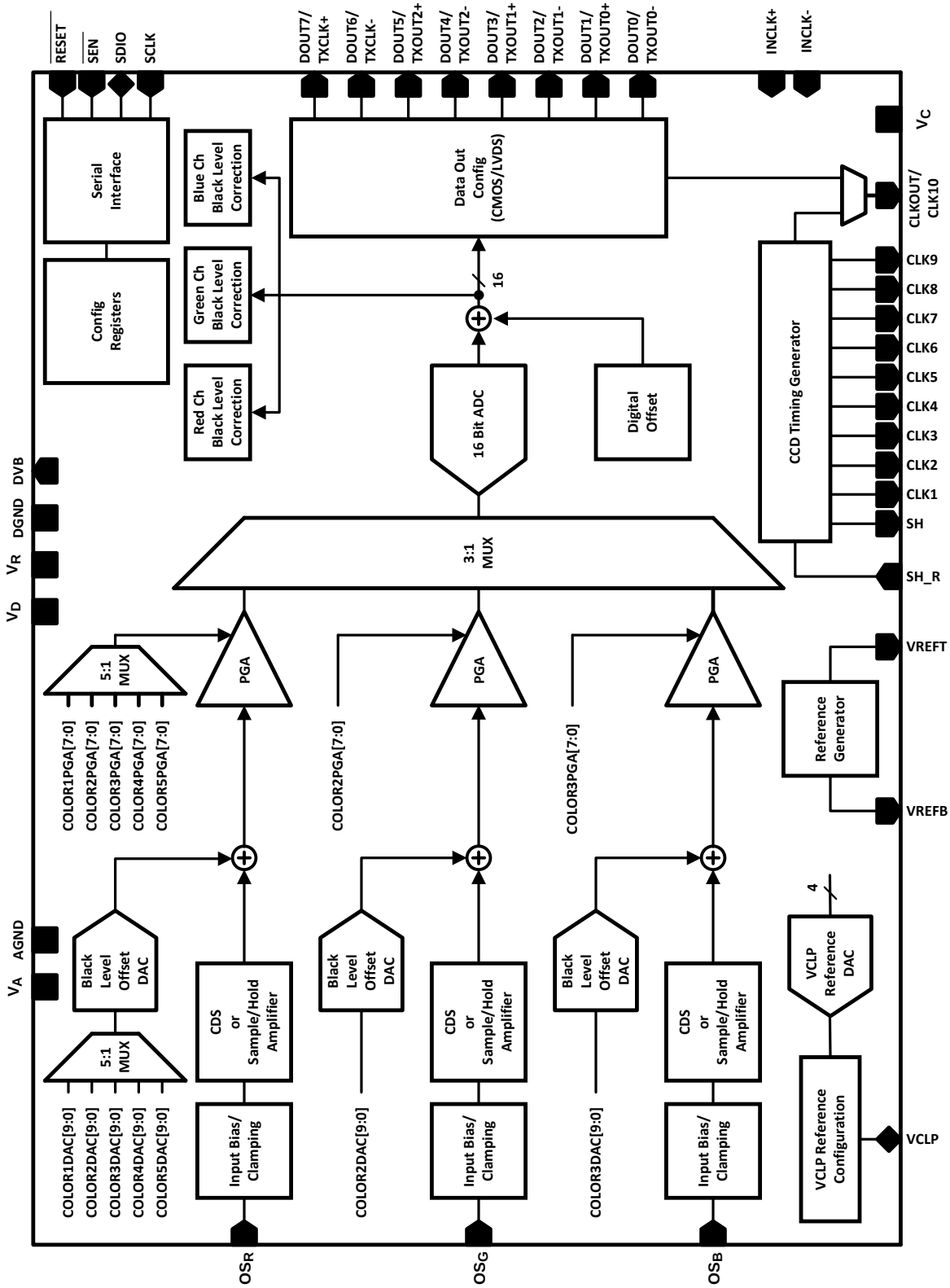


Figure 1. Chip Block Diagram

LM98714 Pin Out Diagram

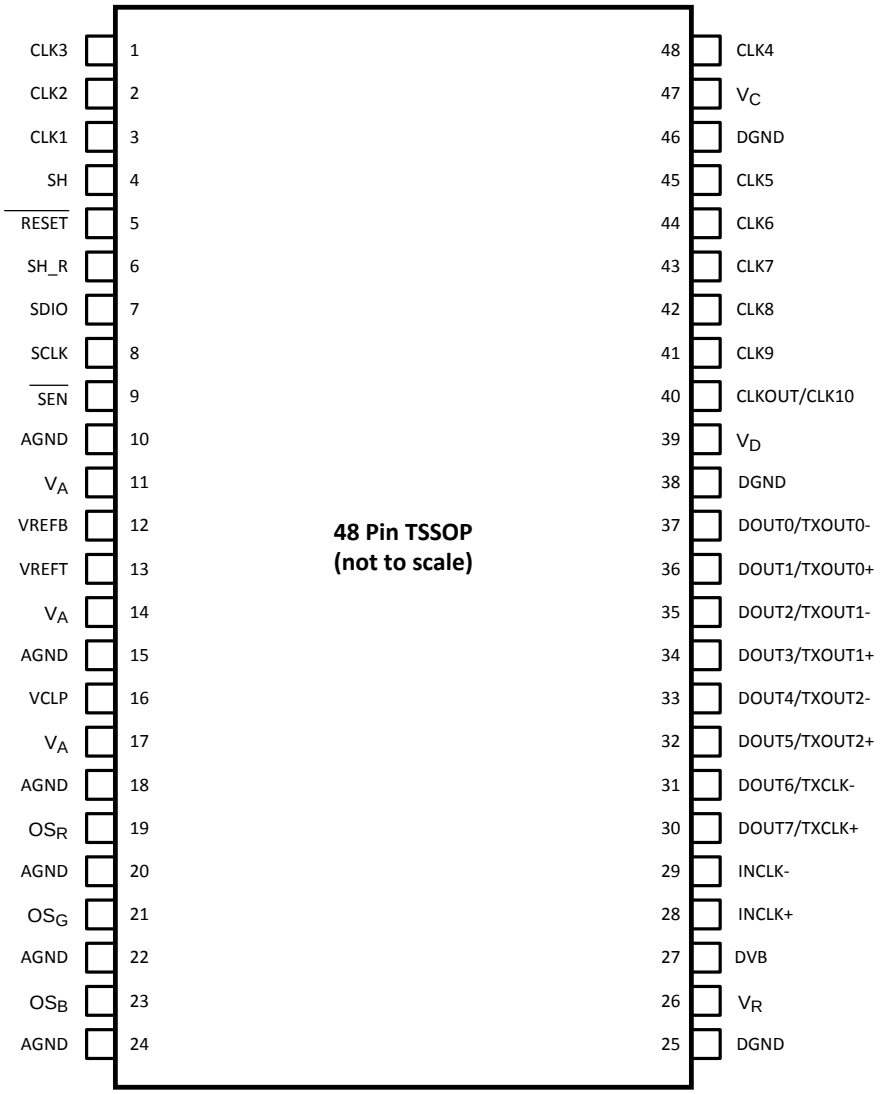


Figure 2. LM98714 Pin Out Diagram

Typical Application Diagram

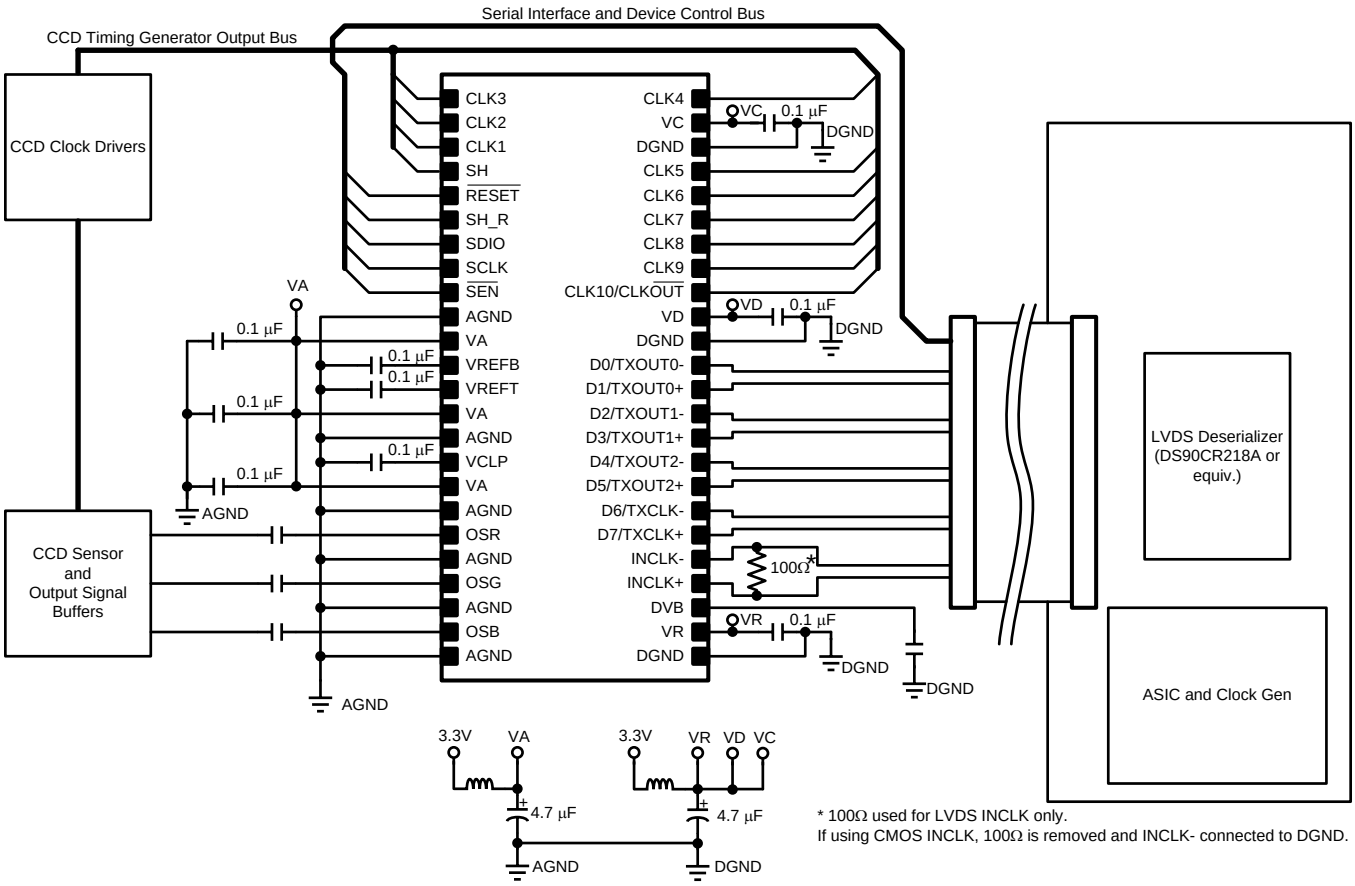


Figure 3. Typical Application Diagram

Pin Descriptions

Pin	Name	I/O[1]	Typ	Res	Description
1	CLK3	O	D	PU	Configurable sensor control output.
2	CLK2	O	D	PD	Configurable sensor control output.
3	CLK1	O	D	PU	Configurable sensor control output.
4	SH	O	D	PD	Sensor - Shift or transfer control signal for CCD and CIS sensors.
5	$\overline{\text{RESET}}$	I	D	PU	Active-low master reset. NC when function not being used.
6	SH_R	I	D	PD	External request for an SH pulse.
7	SDIO	I/O	D		Serial Interface Data Input
8	SCLK	I	D	PD	Serial Interface shift register clock.
9	$\overline{\text{SEN}}$	I	D	PU	Active-low chip enable for the Serial Interface.
10	AGND		P		Analog ground return.
11	V_A		P		Analog power supply. Bypass voltage source with 4.7µF and pin with 0.1µF to AGND.
12	VREFB	O	A		Bottom of ADC reference. Bypass with a 0.1µF capacitor to ground.
13	VREFT	O	A		Top of ADC reference. Bypass with a 0.1µF capacitor to ground.
14	V_A		P		Analog power supply. Bypass voltage source with 4.7µF and pin with 0.1µF to AGND.
15	AGND		P		Analog ground return.
16	VCLP	IO	A		Input Clamp Voltage. Normally bypassed with a 0.1µF, and a 4.7µF capacitor to AGND. An external reference voltage may be applied to this pin.

(1) (I=Input), (O=Output), (IO=Bi-directional), (P=Power), (D=Digital), (A=Analog), (PU=Pull Up with an internal resistor), (PD=Pull Down with an internal resistor.).

Pin Descriptions (continued)

Pin	Name	I/O[1]	Typ	Res	Description
17	V_A		P		Analog power supply. Bypass voltage source with 4.7µF and pin with 0.1µF to AGND.
18	AGND		P		Analog ground return.
19	OS_R	I	A		Analog input signal. Typically sensor Red output AC-coupled thru a capacitor.
20	AGND		P		Analog ground return.
21	OS_G	I	A		Analog input signal. Typically sensor Green output AC-coupled thru a capacitor.
22	AGND		P		Analog ground return.
23	OS_B	I	A		Analog input signal. Typically sensor Blue output AC-coupled thru a capacitor.
24	AGND		P		Analog ground return.
25	DGND		P		Digital ground return.
26	V_R		P		Power supply input for internal voltage reference generator. Bypass this supply pin with a 0.1µF capacitor.
27	DVB	O	P		Digital Core Voltage bypass. Not an input. Bypass with 0.1µF capacitor to DGND.
28	INCLK+	I	D		Clock Input. Non-Inverting input for LVDS clocks or CMOS clock input. CMOS clock is selected when pin 29 is held at DGND, otherwise clock is configured for LVDS operation.
29	INCLK-	I	D		Clock Input. Inverting input for LVDS clocks, connect to DGND for CMOS clock.
30	DOUT7/ TXCLK+	O	D		Bit 7 of the digital video output bus in CMOS Mode, LVDS Frame Clock+ in LVDS Mode.
31	DOUT6/ TXCLK-	O	D		Bit 6 of the digital video output bus in CMOS Mode, LVDS Frame Clock- in LVDS Mode.
32	DOUT5/ TXOUT2+	O	D		Bit 5 of the digital video output bus in CMOS Mode, LVDS Data Out2+ in LVDS Mode.
33	DOUT4/ TXOUT2-	O	D		Bit 4 of the digital video output bus in CMOS Mode, LVDS Data Out2- in LVDS Mode.
34	DOUT3/ TXOUT1+	O	D		Bit 3 of the digital video output bus in CMOS Mode, LVDS Data Out1+ in LVDS Mode.
35	DOUT2/ TXOUT1-	O	D		Bit 2 of the digital video output bus in CMOS Mode, LVDS Data Out1- in LVDS Mode.
36	DOUT1/ TXOUT0+	O	D		Bit 1 of the digital video output bus in CMOS Mode, LVDS Data Out0+ in LVDS Mode.
37	DOUT0/ TXOUT0-	O	D		Bit 0 of the digital video output bus in CMOS Mode, LVDS Data Out0- in LVDS Mode.
38	DGND		P		Digital ground return.
39	V_D		P		Power supply for the digital circuits. Bypass this supply pin with 0.1µF capacitor. A single 4.7µF capacitor should be used between the supply and the VD, VR and VC pins.
40	CLKOUT/ CLK10	O	D	PD	Output clock for registering output data when using CMOS outputs, or configurable sensor control output.
41	CLK9	O	D	PD	Configurable sensor control output.
42	CLK8	O	D	PD	Configurable sensor control output.
43	CLK7	O	D	PD	Configurable sensor control output.
44	CLK6	O	D	PU	Configurable sensor control output.
45	CLK5	O	D	PD	Configurable sensor control output.
46	DGND		P		Digital ground return.
47	V_C		P		Power supply for the sensor control outputs. Bypass this supply pin with 0.1µF capacitor.
48	CLK4	O	D	PD	Configurable sensor control output.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)(3)

Supply Voltage (VA,VR,VD,VC)		4.2V
Voltage on Any Input Pin (Not to exceed 4.2V)		−0.3V to (VA + 0.3V)
Voltage on Any Output Pin (except DVB and not to exceed 4.2V)		−0.3V to (VA + 0.3V)
DVB Output Pin Voltage		2.0V
Input Current at any pin other than Supply Pins (4)		±25 mA
Package Input Current (except Supply Pins) (4)		±50 mA
Maximum Junction Temperature (TA)		150°C
Thermal Resistance (θ_{JA})		66°C/W
Package Dissipation at T_A = 25°C (5)		1.89W
ESD Rating (6)	Human Body Model	2500V
	Machine Model	250V
Storage Temperature		−65°C to +150°C
Soldering process must comply with TI's Reflow Temperature Profile specifications. Refer to www.ti.com/packaging. (7)		

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the Operating Ratings is not recommended.
(2) All voltages are measured with respect to AGND = DGND = 0V, unless otherwise specified.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) When the input voltage (V_{IN}) at any pin exceeds the power supplies (V_{IN} < GND or V_{IN} > V_A or V_D), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can simultaneously safely exceed the power supplies with an input current of 25 mA to two.
(5) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} – T_A)/\theta_{JA}$. The values for maximum power dissipation listed above will be reached only when the device is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Such conditions should always be avoided.
(6) Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through 0Ω.
(7) Reflow temperature profiles are different for lead-free and non-lead-free packages.

Operating Ratings (1)(2)

Operating Temperature Range	0°C ≤ T_A ≤ +70°C
All Supply Voltage	+3.0V to +3.6V

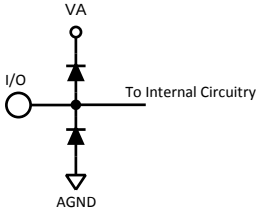
(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the Operating Ratings is not recommended.
(2) All voltages are measured with respect to AGND = DGND = 0V, unless otherwise specified.

Electrical Characteristics

The following specifications apply for VA = VD = VR = VC = 3.3V, C_L = 10pF, and f_{INCLK} = 15MHz unless otherwise specified. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX};** all other limits T_A = 25°C. (1)

Symbol	Parameter	Conditions	Min	Typ (2)	Max	Units
CMOS Digital Input DC Specifications (RESETb, SH_R, SCLK, SENb)						
V_{IH}	Logical “1” Input Voltage		2.0			V
V_{IL}	Logical “0” Input Voltage				0.8	V
I_{IH}	Logical “1” Input Current	V_{IH} = VD				
		$\overline{RESET}$		235		nA
		SH_R, SCLK		70		µA
		$\overline{SEN}$		130		nA
I_{IL}	Logical “0” Input Current	VIL = DGND				
		$\overline{RESET}$		70		µA
		SH_R, SCLK		235		nA
		$\overline{SEN}$		70		µA
CMOS Digital Output DC Specifications (SH, CLK1 to CLK10, CMOS Data Outputs)						
V_{OH}	Logical “1” Output Voltage	I_{OUT} = -0.5mA	2.95			V
V_{OL}	Logical “0” Output Voltage	I_{OUT} = 1.6mA			0.25	V
I_{OS}	Output Short Circuit Current	V_{OUT} = DGND		16		mA
		V_{OUT}= VD		-20		
I_{OZ}	CMOS Output TRI-STATE Current	V_{OUT} = DGND		20		nA
		V_{OUT} = VD		-25		
CMOS Digital Input/Output DC Specifications (SDIO)						
I_{IH}	Logical “1” Input Current	V_{IH} = VD		90		nA
I_{IL}	Logical “0” Input Current	V_{IL} = DGND		90		nA
LVDS/CMOS Clock Receiver DC Specifications (INCLK+ and INCLK- Pins)						
V_{IHL}	Differential LVDS Clock High Threshold Voltage	R_L = 100W V_{CM} (LVDS Input Common Mode Voltage)= 1.25V			100	mV
V_{ILL}	Differential LVDS Clock Low Threshold Voltage		-100			mV
V_{IHC}	CMOS Clock High Threshold Voltage	INCLK- = DGND	2.0			V
V_{ILC}	CMOS Clock Low Threshold Voltage				0.8	V
I_{IHL}	CMOS Clock Input High Current				280	µA
I_{ILC}	CMOS Clock Input Low Current				-150	µA
LVDS Output DC Specifications						
V_{OD}	Differential Output Voltage	R_L = 100Ω	180	328	450	mV
V_{OS}	LVDS Output Offset Voltage		1.17	1.23	1.3	V

(1) The analog inputs are protected as shown below. Input voltage magnitudes beyond the supply rails will not damage the device, provided the current is limited per Absolute Maximum Ratings, Note 4. However, input errors will be generated If the input goes above VA and below AGND.



(2) Typical figures are at T_A = 25°C, and represent most likely parametric norms at the time of product characterization. The typical specifications are not ensured.

Electrical Characteristics (continued)

The following specifications apply for VA = VD = VR = VC = 3.3V, C_L = 10pF, and f_{INCLK} = 15MHz unless otherwise specified. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX};** all other limits T_A = 25°C.(1)

Symbol	Parameter	Conditions	Min	Typ (2)	Max	Units
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100Ω		7.9		mA
Power Supply Specifications						
IA	VA Analog Supply Current	VA Normal State	60	97	125	mA
		VA Low Power State (Powerdown)	12	23	32	mA
IR	VR Digital Supply Current	VR Normal State (LVDS Outputs)	30	64	75	mA
		CMOS Output Data Format	15	47	55	mA
		LVDS Output Data Format with Data Outputs Disabled		47		mA
ID	VD Digital Output Driver Supply Current	LVDS Output Data Format		0.05		mA
		CMOS Output Data Format (ATE Loading of CMOS Outputs > 50pF)	12		40	mA
IC	VC CCD Timing Generator Output Driver Supply Current	Typical sensor outputs: SH, CLK1=Φ1A, CLK2=Φ2A, CLK3=ΦB, CLK4=ΦC, CLK5=RS, CLK6=CP (ATE Loading of CMOS Outputs > 50pF)	0.5		12	mA
PWR	Average Power Dissipation	LVDS Output Data Format	350	505	650	mW
		CMOS Output Data Format (ATE Loading of CMOS Outputs > 50pF)	380	610	700	mW
Input Sampling Circuit Specifications						
V_{IN}	Input Voltage Level	CDS Gain=1x, PGA Gain=1x		2.3		Vp-p
		CDS Gain=2x, PGA Gain= 1x		1.22		
I_{IN_SH}	Sample and Hold Mode Input Leakage Current	Source Followers Off CDS Gain = 1x OS_X = VA (OS_X = AGND)	50 (-70)		70 (-40)	µA
		Source Followers Off CDS Gain = 2x OS_X = VA (OS_X = AGND)	75 (-105)		105 (-75)	µA
		Source Followers On CDS Gain = 2x OS_X = VA (OS_X = AGND)	-200	-10 -16	200	nA
C_{SH}	Sample/Hold Mode Equivalent Input Capacitance	CDS Gain = 1x		2.5		pF
		CDS Gain = 2x		4		pF
I_{IN_CDS}	CDS Mode Input Leakage Current	Source Followers Off OS_X = VA (OS_X = AGND)	-300	7 (-25)	300	nA
R_{CLPIN}	CLPIN Switch Resistance			16	50	Ω
VCLP Reference Circuit Specifications						
	VCLP DAC Resolution			4		Bits
	VCLP DAC Step Size			0.16		V
V_{VCLP}	VCLP DAC Voltage Min Output	VCLP Config. Register = 0001 0000b	0.14	0.26	0.43	V
	VCLP DAC Voltage Max Output	VCLP Config. Register = 0001 1111b	2.38	2.68	2.93	V
	Resistor Ladder Enabled	VCLP Config. Register = 0010 xxxxb	1.54	V_A / 2	1.73	V

Electrical Characteristics (continued)

The following specifications apply for VA = VD = VR = VC = 3.3V, C_L = 10pF, and f_{INCLK} = 15MHz unless otherwise specified. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX};** all other limits T_A = 25°C.(1)

Symbol	Parameter	Conditions	Min	Typ (2)	Max	Units
I_{SC}	VCLP DAC Short Circuit Output Current	VCLP Config. Register = 0001 xxxxb		30		mA
Black Level Offset DAC Specifications						
	Resolution			10		Bits
	Monotonicity			Specified by characterization		
	Offset Adjustment Range Referred to AFE Input	CDS Gain = 1x Minimum DAC Code = 0x000 Maximum DAC Code = 0x3FF		 -614 614		mV
		CDS Gain = 2x Minimum DAC Code = 0x000 Maximum DAC Code = 0x3FF		 -307 307		mV
	Offset Adjustment Range Referred to AFE Output	Minimum DAC Code = 0x000 Maximum DAC Code = 0x3FF	-16000 16000		-18200 18200	LSB
	DAC LSB Step Size	CDS Gain = 1x Referred to AFE Output		1.2 (32)		mV (LSB)
DNL	Differential Non-Linearity		-0.95		3.25	LSB
INL	Integral Non-Linearity		-3.1		2.65	LSB
PGA Specifications						
	Gain Resolution			8		Bits
	Monotonicity			Specified by characterization		
	Maximum Gain	CDS Gain = 1x	7.18	7.9	8.77	V/V
		CDS Gain = 1x	17.1	17.9	18.9	dB
	Minimum Gain	CDS Gain = 1x	0.56	0.7	0.82	V/V
		CDS Gain = 1x	-5	-3	-1.72	dB
	PGA Function	Gain (V/V) = (196/(280-PGA Code))				
		Gain (dB) = 20LOG10(196/(280-PGA Code))				
	Channel Matching	Minimum PGA Gain Maximum PGA Gain		3 12.7		%
ADC Specifications						
V_{REFT}	Top of Reference			2.07		V
V_{REFB}	Bottom of Reference			0.89		V
V_{REFT} - V_{REFB}	Differential Reference Voltage		1.07	1.18	1.29	V
	Overrange Output Code			65535		
	Underrange Output Code			0		
Digital Offset "DAC" Specifications						
	Resolution			7		Bits
	Digital Offset DAC LSB Step Size	Referred to AFE Output		16		LSB
	Offset Adjustment Range Referred to AFE Output	Min DAC Code =7b0000000 Mid DAC Code =7b1000000 Max DAC Code = 7b1111111		-1024 0 1008		LSB
Full Channel Performance Specifications						
DNL	Differential Non-Linearity		-0.99	0.8/-0.6	2.55	LSB
INL	Integral Non-Linearity		-73	+/-23	78	LSB

Electrical Characteristics (continued)

The following specifications apply for VA = VD = VR = VC = 3.3V, C_L = 10pF, and f_{INCLK} = 15MHz unless otherwise specified. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX};** all other limits T_A = 25°C.(1)

Symbol	Parameter	Conditions	Min	Typ (2)	Max	Units
SNR	Total Output Noise	Minimum PGA Gain		-79		dB
				7.2		LSB RMS
		PGA Gain = 1x		-74		dB
				13	30	LSB RMS
		Maximum PGA Gain		-56		dB
				104		LSB RMS
	Channel to Channel Crosstalk	Mode 3		47		LSB
		Mode 2		16		

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM98714BCMT/NOPB	ACTIVE	TSSOP	DGG	48	38	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 70	LM98714 BCMT	Samples
LM98714BCMTX/NOPB	ACTIVE	TSSOP	DGG	48	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 70	LM98714 BCMT	Samples
LM98714CCMT	ACTIVE	TSSOP	DGG	48	38	TBD	Call TI	Call TI	0 to 70	LM98714 CCMT	Samples
LM98714CCMT/NOPB	ACTIVE	TSSOP	DGG	48	38	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 70	LM98714 CCMT	Samples
LM98714CCMTX	ACTIVE	TSSOP	DGG	48	1000	TBD	Call TI	Call TI	0 to 70	LM98714 CCMT	Samples
LM98714CCMTX/NOPB	ACTIVE	TSSOP	DGG	48	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	0 to 70	LM98714 CCMT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

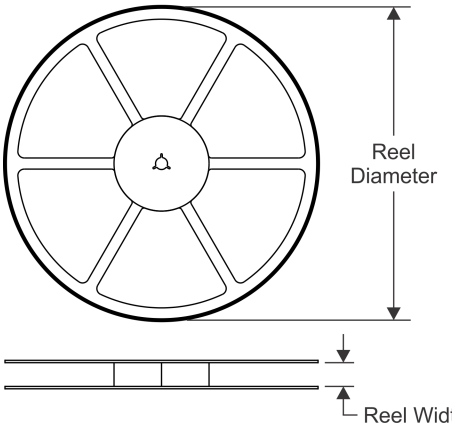
(4) Only one of markings shown within the brackets will appear on the physical device.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

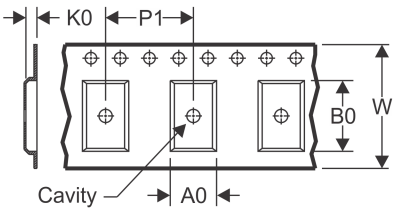
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

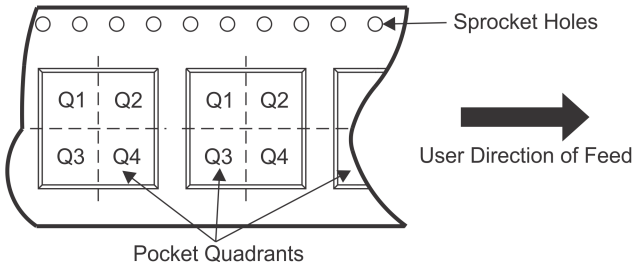


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

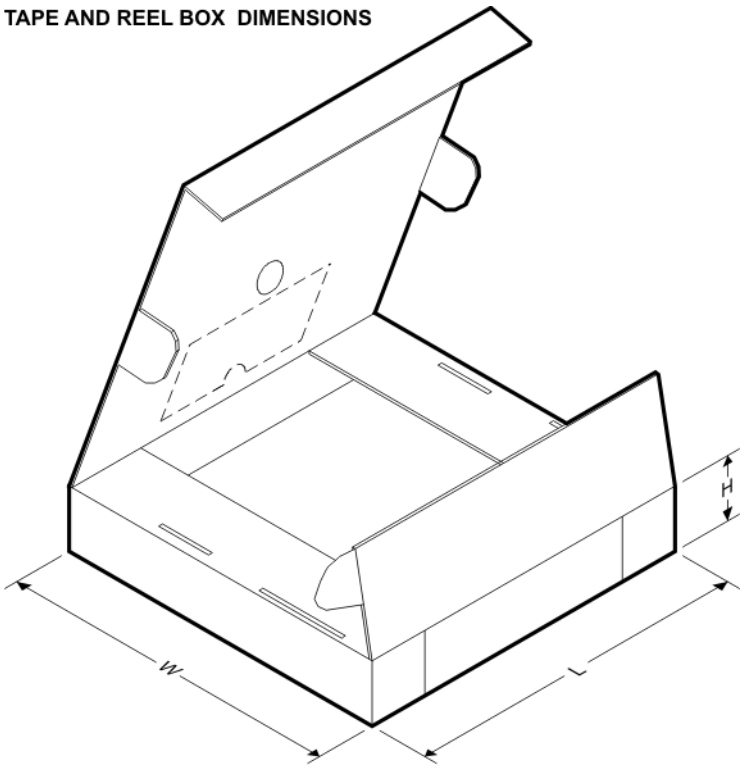
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM98714BCMTX/NOPB	TSSOP	DGG	48	1000	330.0	24.4	8.6	13.2	1.6	12.0	24.0	Q1
LM98714CCMTX	TSSOP	DGG	48	1000	330.0	24.4	8.6	13.2	1.6	12.0	24.0	Q1
LM98714CCMTX/NOPB	TSSOP	DGG	48	1000	330.0	24.4	8.6	13.2	1.6	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

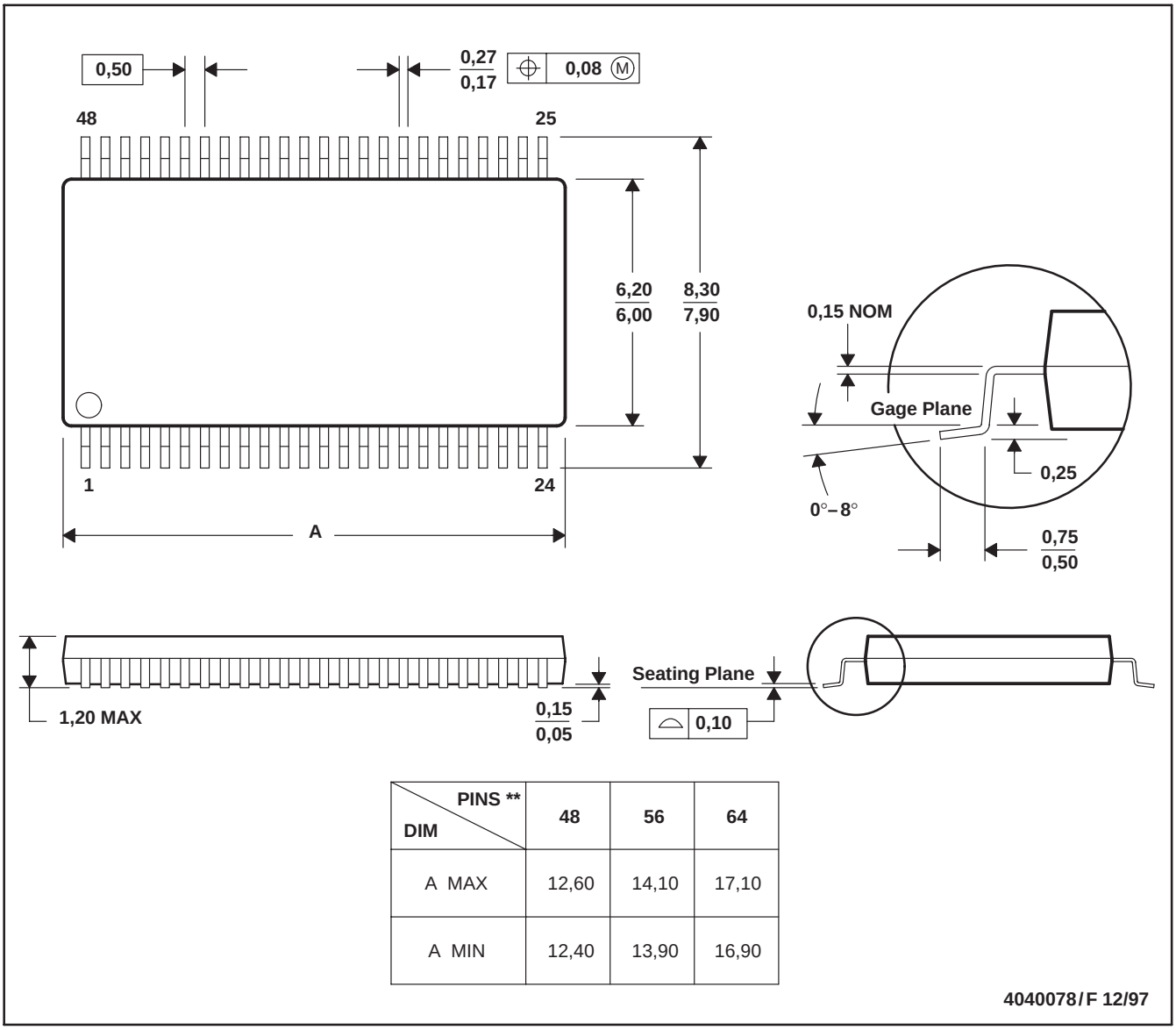


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM98714BCMTX/NOPB	TSSOP	DGG	48	1000	358.0	343.0	63.0
LM98714CCMTX	TSSOP	DGG	48	1000	358.0	343.0	63.0
LM98714CCMTX/NOPB	TSSOP	DGG	48	1000	358.0	343.0	63.0

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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