EQ50F100
6.25Gbps Backplane Equalizer
Evaluation Kit User Manual

Part Number: EQ50EVK

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Communication Interface Division
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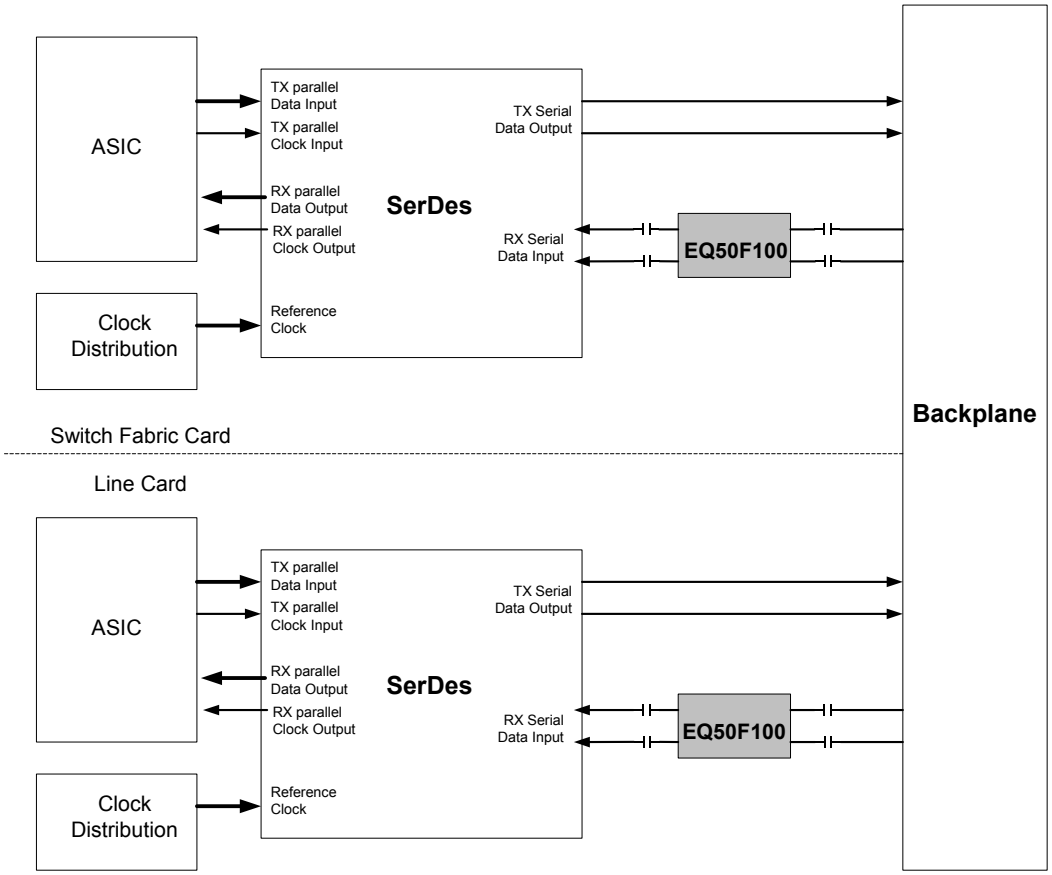
Introduction

The National Semiconductor EQ50F100 evaluation kit (EQ50EVK) demonstrates the performance of the 6.25Gbps Backplane Equalizer.

The printed circuit board (PCB) is optimized for giga-bit operation. The CML differential traces impedance is 100 Ohms differential and it is equipped with AC-coupling capacitors on both input and output trace. All CML traces have matched trace lengths for low skew.

This evaluation kit can be used to test and verify the performance of the EQ50F100 equalizer in backplane and cable application.

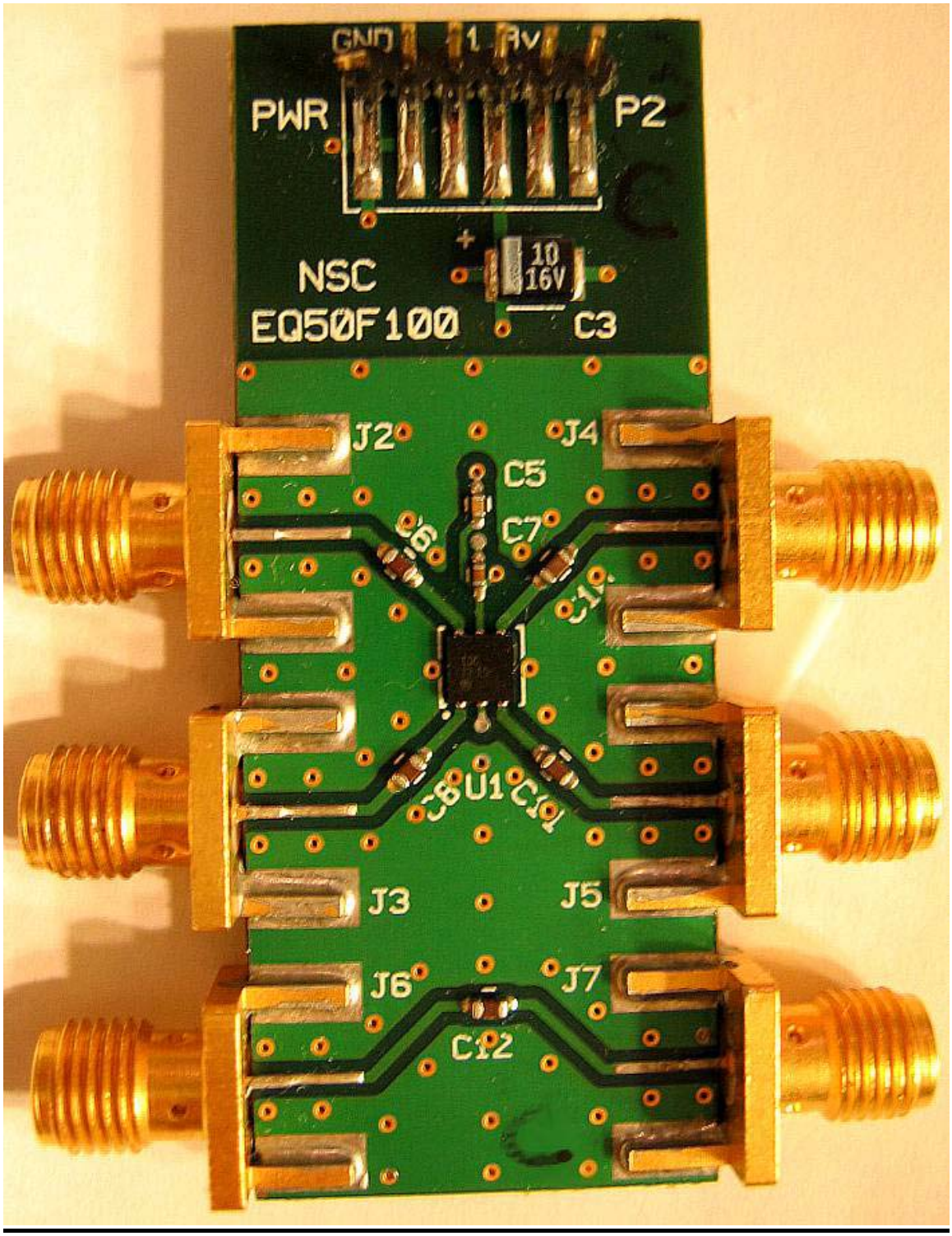
Application



The diagram above illustrates the use of the EQ50EVK along with a Backplane SerDes, in a giga-bit backplane transmission application.

Please refer to datasheet for information.

Evaluation Board



Setup

The setup of EQ50EVK evaluation board is very straightforward. To start using the evaluation kit, follow these steps:

1) Connect signal source positive output to EQ50EVK positive input (J2).
2) Connect signal source negative output to EQ50EVK negative input (J3).
3) Connect EQ50EVK positive output (J4) to the positive input of SerDes/ASIC/FPGA/Test Equipment.
4) Connect EQ50EVK positive output (J5) to negative input of SerDes/ASIC/FPGA/Test Equipment.
5) Apply power (+1.8V) and ground to EQ50EVK PWR section (P2). See Figure 1 for detail.

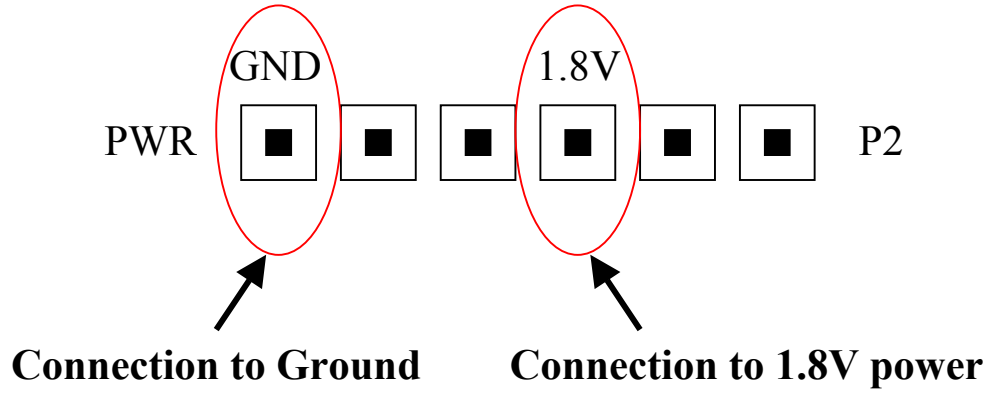


Figure 1

Overview

The EQ50EVK has total of 4 layers: 1) Signal layer, 2) GND layer, 3) +1.8V power layer and 4) bottom layer. The total board thickness is 62mil. The high-speed CML signal traces are 20mil wide with impedance of 100-Ohm differential.

The CML input and output of the EQ50F100 is access through SMA connector (J2 – J5). Power and ground are supplied through 2mm Header-pin connector P2. See Figure 1 for detail.

Tantalum 10uF capacitors (C3) placed near the power connection provide bulk energy storage. In addition to excellent bypassing provided by the closely sandwiched power and ground planes, a network of 10nF (C5) and 100pF (C7) bypass capacitors is placed between Vcc and ground to provide additional bypassing near the device.

Troubleshooting

If the demo boards are not performing properly, use the following as a guide for quick solutions to common problems. If the problem persists, contact the hotline number listed under Additional Information section of this document.

Check the following:

1. Power and Ground are connected to the power connections of the board.
2. Supply voltage (+1.8V) and current (It's around 40mA).
3. Input signal to input SMA connectors.
4. Connection and signal to the input SMA connectors (J2, J3) on the board.
5. Connection from the output SMA connectors (J4, J5) on the board.
6. Soldering on the input and output SMA connectors.

Other Resources

For more information on High Speed Backplane Solution, refer to the National's LVDS website at:

LVDS.national.com

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