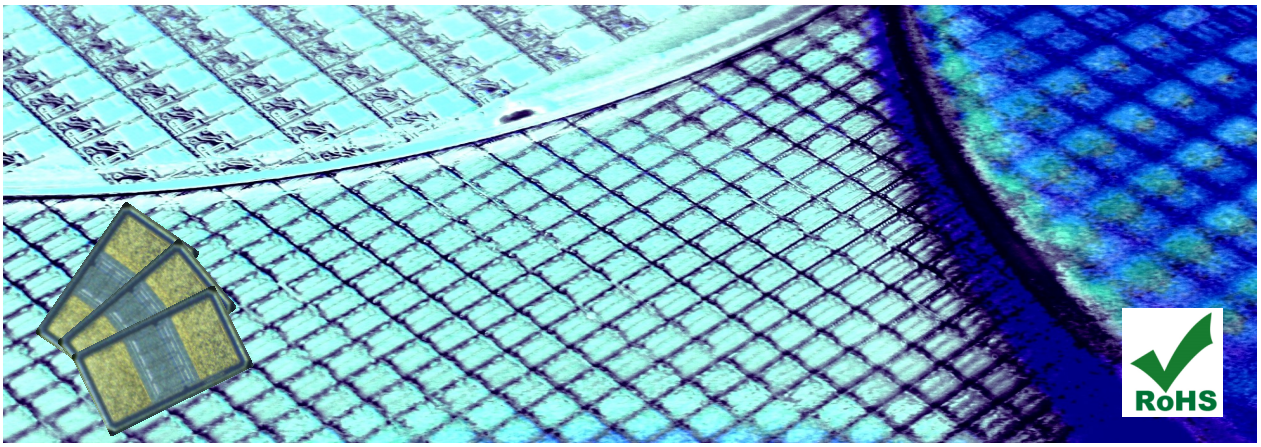
UBSC/ULSC – 60^{+}GHz Ultra Broadband Silicon Capacitors – Surface Mounted

Rev 2.5



Key Features

- Ultra broadband performance up to 60^{+}GHz
- Resonance free
- Phase stability
- Ultra high stability of capacitance value over:
  - Temperature < ± 0.5 % (-55°C to +150°C)
  - Voltage < 0.1 %/V
  - Aging < 0.001 %/1000 hours
- Low ESL
- High reliability (FIT < 0.017 parts/billion hours)
- Compatible with lead free reflow-soldering*

  * Please refer to our Assembly Application Note for more details

Key Applications

- Optoelectronics/high-speed data
- Trans-Impedance Amplifiers (TIA)
- Receive-and-Transmit Optical Sub-Assembly (ROSA/TOSA)
- Synchronous Optical Networking (SONET)
- High speed digital logic
- Broadband test equipment
- Broadband microwave/millimeter wave
- Replacement of X7R and NP0
- Low profile applications (400 or 100 µm)

UBSC/ULSC Capacitors target **optical communication systems** (ROSA/TOSA, SONET and all optoelectronics) as well as **high speed data systems** or products. The UBSC/ULSC are designed for DC blocking, feedback, coupling and bypass grounding applications. The unique technology of integrated passive devices in silicon developed by IPDiA, offers **low insertion loss, low reflection and high phase stability** from 16 kHz up to 60 GHz for the UBSC and up to 20 GHz for the ULSC. These deep trench silicon capacitors have been developed with a semiconductor MOS process.

The UBSC / ULSC capacitors provide **very high reliability** and capacitance stability over temperature (±0.5 %) and voltage. They have an extended operating temperature range from -55 to 150°C. **Reliable and repeatable performances** are obtained thanks to a fully controlled production line with high temperature curing (above 900°C) generating a highly pure oxide. The UBSC / ULSC series are compliant with standard JEDEC assembly rules, making the product fully compatible with high speed automated pick-and-place manufacturing operations. Case sizes of 0201 and 0603 are also available. These capacitors are RoHS-compliant and are available with ENIG terminations.

ipdia
The 3D Silicon Leader

Electrical Specifications

Part number	Product description	Case Size	Thickness
UBSC.xxx	Surface Mount Ultra Broad Band Silicon Capacitor from -55 to 150°C, 60⁺GHz with ENIG termination		
935 151 423 510	Ultra Broadband Si Cap 10nF 60+GHz 400µm, BV>11V	0201	400µm
935 151 723 510	Ultra Broadband Si Cap 10nF 60+GHz 400µm, BV>30V	0201	400µm
935 152 423 510	Ultra Broadband Si Cap 10nF 60+GHz 100µm, BV>11V	0201	100µm
935 152 723 510	Ultra Broadband Si Cap 10nF 60+GHz 100µm, BV>30V	0201	100µm
935 151 424 610	Ultra Broadband Si Cap 100nF 60+GHz 400µm, BV>11V	0402	400µm
935 152 424 610	Ultra Broadband Si Cap 100nF 60+GHz 100µm, BV>11V	0402	100µm
935 151 425 610	Ultra Broadband Si Cap 100nF 60+GHz 400µm, BV>11V	0603	400µm
935 152 425 610	Ultra Broadband Si Cap 100nF 60+GHz 100µm, BV>11V	0603	100µm

ULSC.xxx	Surface Mount Ultra Broad Band Silicon Capacitor from -55 to 150°C, 20 GHz with ENIG termination		
935 155 424 610	Ultra Broadband Si Cap 100nF 20 GHz 400µm, BV>11V	0402	400µm
935 156 424 610	Ultra Broadband Si Cap 100nF 20 GHz 100µm, BV>11V	0402	100µm

Parameters	Value
Capacitance range	*10nF to 100 nF(**)*
Capacitance tolerance	*± 15 %(**)*
Operating temperature range	*-55 °C to 150 °C*
Storage temperature	*- 70 °C to 165 °C*
Temperature coefficient	*<±0.5 %, from -55 °C to +150 °C*
Breakdown voltage (BV)	*11, 30 V(**)*
Capacitance variation versus RVDC	*0.1 %/V (from 0 V to RVDC)*
Equivalent Serial Inductance (ESL)	*Max 100 pH(***)*
Equivalent Serial Resistance (ESR)	*Max 400 mΩ(***)*
Insulation resistance	*100 GΩ min @ RVDC & +25°C*
Aging	*Negligible, < 0.001 % / 1000h*
Reliability	*FIT<0.017 parts / billion hours*
Capacitor height	*Max 400 µm or 100 µm*

(**) Other values on request.

(***) e.g. 100nF/0402/BV 11V

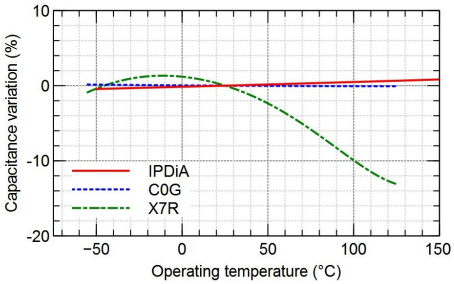


Fig.1: Capacitance variation vs temperature (for UBSC and MLCC technologies)

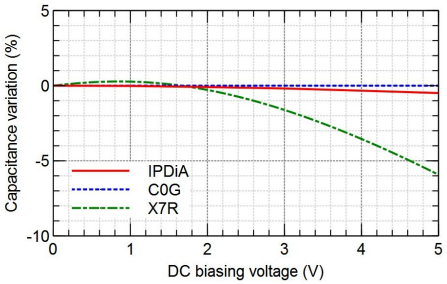


Fig.2: Capacitance variation vs DC biasing voltage (for UBSC and MLCC technologies)

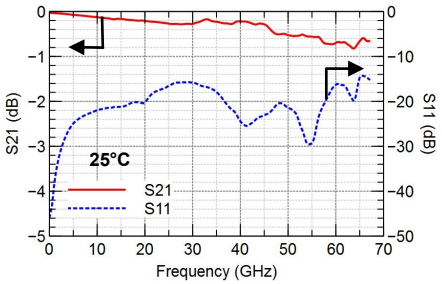
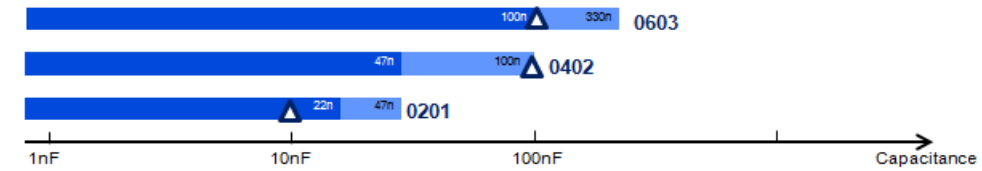


Fig.3: 100 nF/0402 UBSC measurement results (S-parameters in transmission mode)

UBSC/ULSC Capacitance Range



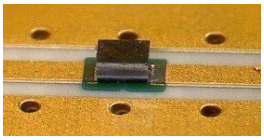
Δ Available parts – see table above
For other values, contact your IPDiA sales representative

BV 30V BV 11V

Termination and Outline

Termination

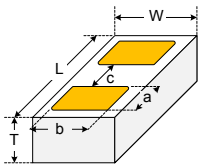
Lead-free nickel/solder coating compatible with automatic soldering technologies: reflow and manual.



Package Outline

For landing pad dimensions on your PCB layout, please refer to IPDiA assembly application note.

(mm)	Pad dimensions			Case size (typ. ±0.01mm)		
	a	b	c	L	W	T
0201	0.15	0.40	0.30	0.80	0.60	0.40 (standard profile) or 0.10 (low profile)
0402	0.30	0.50	0.40	1.20	0.70	
0603	0.40	0.90	0.80	1.80	1.10	



Packaging

Tape and reel, waffle pack, film frame carrier or raw wafer delivery.

For more information, please visit: http://www.ipdia.com
To contact us, email to: sales@ipdia.com

Date of release: May 13th 2015
Document identifier: CL

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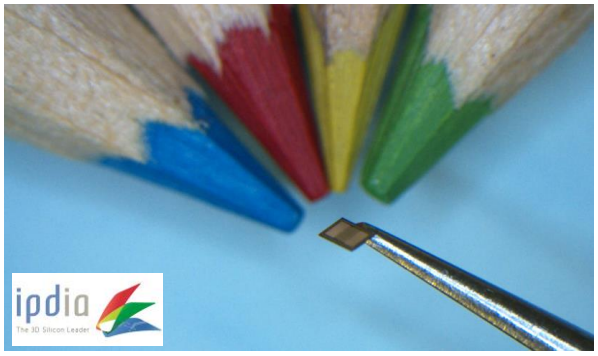
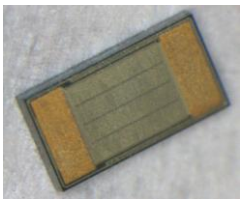
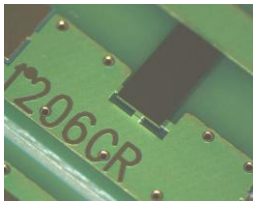


Introduction

This document describes the attachment techniques recommended by IPDiA for their UBSC/ULSCC (100µm thickness) silicon capacitors on the customer substrates. This document is non-exhaustive. Customers with specific attachment requirements or attachment scenarios that are not covered by this document should contact IPDiA. The solder printing is described in this document but other processes like solder jetting, capacitors pre-bumped, … can also be used with the same recommendations.



IPDiA Silicon capacitor (1206)



The silicon capacitor mounted on PCB board

Handling precautions and storage

Silicon die must always be handled in a clean room environment (usually class 1000 (ISO 6)) but the assembled devices don't need to be handled in such an environment as the product is already well packed. The remaining quantities have to be repacked immediately after any process step, in the same conditions as before the opening (ESD bag + N2)

Store the capacitors in the manufacturer's package in the following conditions without a rapid thermal change in an indoor room:

- Temperature: -10 to 40 degree C
- Humidity: 30 to 70%RH

Avoid storing the capacitors in the following conditions:

(a) Ambient air containing corrosive gas. (Chlorine, Hydrogen sulfide, Ammonia, Sulfuric acid, Nitric oxide, etc.)
(b) Ambient air containing volatile or combustible gas
(c) In environments with a high concentration of airborne particles
(d) In liquid (water, oil, chemical solution, organic solvents, etc.)
(e) In direct sunlight
(f) In freezing environments

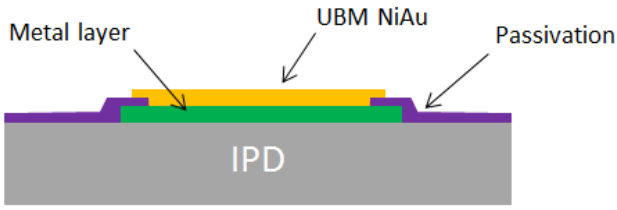
To avoid contamination and damage like scratches and cracks, our recommendations are:

- Die must never be handled with bare hands
- Avoid touching the active face
- Do not store and transport die outside protective bags, tubes, boxes, sawn tape
- Work only in ESD environments
- Plastic tweezers or a soft vacuum tool are recommended to remove the silicon die from the packing.

Standard packing is tape & reel for die size larger than 0201 but silicon capacitors can be provided within waffle pack, gelpak or sawing frame. Please contact the IPDIA sales contact for drawing and references (sales@ipdia.com).

Pad opening

The top surface of the IPDiA silicon capacitors are protected with a mineral passivation. The finishing of the contact pads are in nickel gold (generally 5µm nickel and 0.2µm gold) conforming with the soldering process.



IPDiA recommends having an opening on the board which matches the pad of the capacitor (size, position and spacing) – see figure 1. On the substrate, the metal layer can be larger than the varnish coating opening size but in this case, the varnish coating opening has to be mirror with the pad size of the capacitor. These recommendations will improve the die placement, tilting and will avoid the contact between the solder paste and the bare silicon die (see figure 2).

Solder paste after reflow:

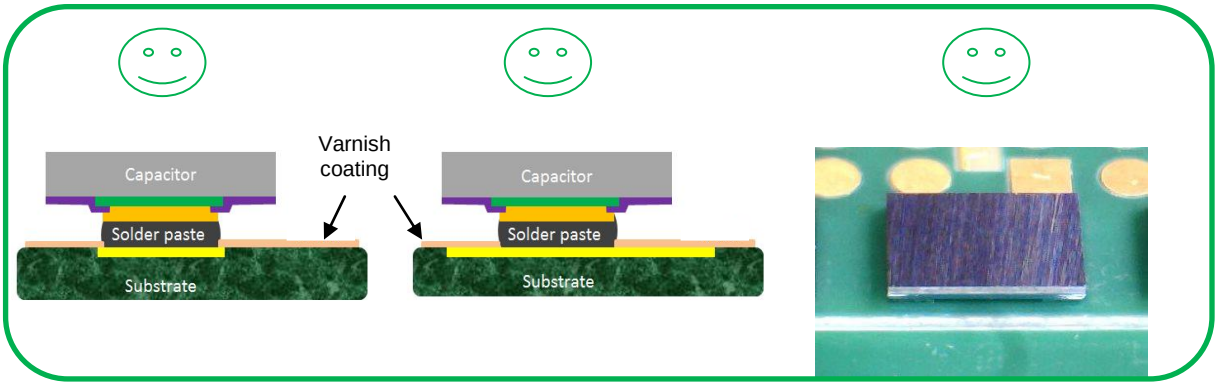


Figure 1: Solder paste after reflow - Targeted

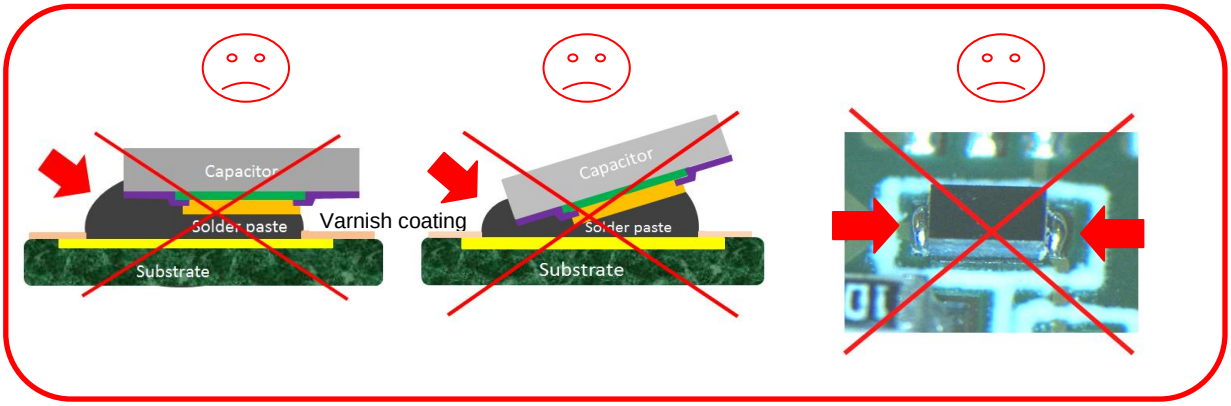


Figure 2: Solder paste after reflow - Rejected

Design of the board:

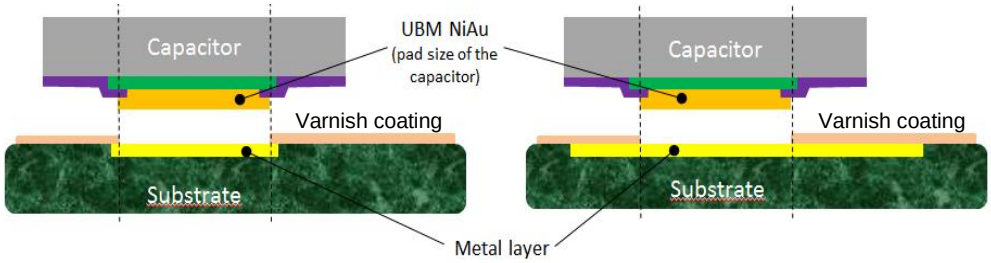
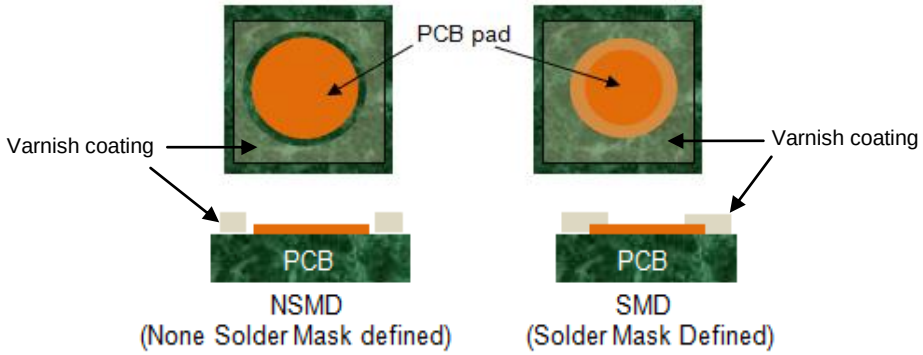
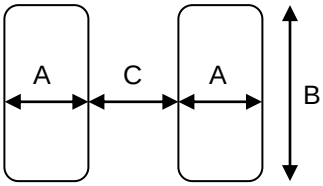


Figure 3: Opening of the metal layer on the customer substrate should match the pad of the silicon die

On the customer substrate, IPDiA recommends SMD (Solder Mask Design) to control the solder flowing on the tracks:



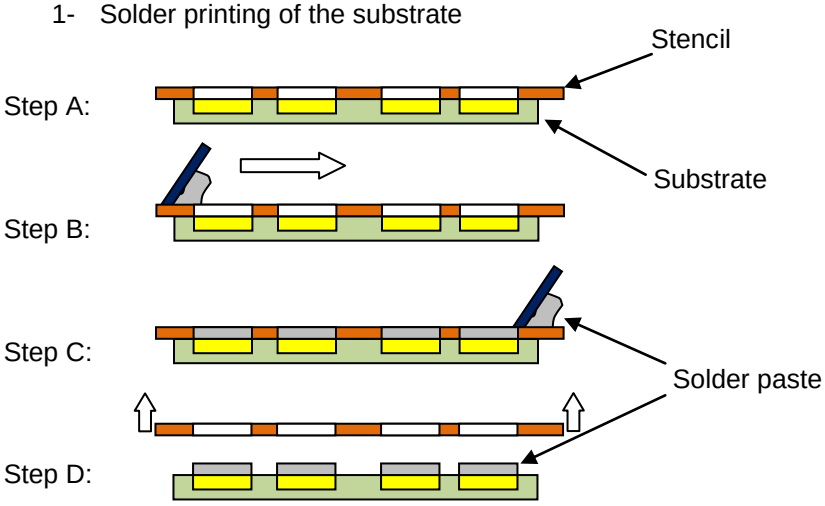
Landing pad for the PCB and die pad dimensions for the IPDiA silicon die:



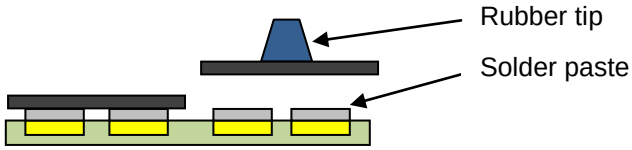
Silicon Capacitor Type	Capacitor size (µm²)	Capacitor thickness	A (µm)	B (µm)	C (µm)
0201	800 x 600	100µm	150	400	300
0402	1200 x 700		300	500	400
0603	1800 x 1100		400	900	800
0805	2200 x 1400		500	1200	1000
1206	3400 x 1800		600	1600	2000
1812	4700 x 3600		900	3400	2700

Process Flow

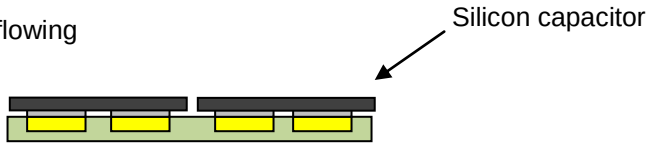
1- Solder printing of the substrate



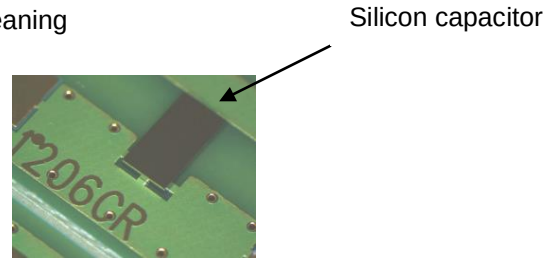
2- Picking of the silicon die and placement



3- Reflowing



4- Cleaning



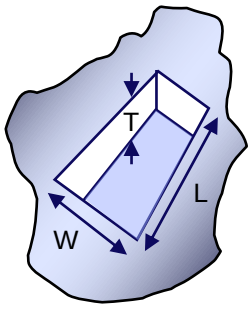
Solder print material and stencil printing recommendations

Solder pastes SnPb63/37 or SAC305 are usually used and recommended but other materials compatible with the die pad finishing are also possible.
In function of the die pad size, powder size could be adjusted.

ALLOY	COMPOSITION	SOLIDUS	LIQUIDUS	COMMENTS
Sn63	63Sn, 37Pb	183°c	183°c	Eutectic
SAC305	96,5Sn, 3Ag, 0.5Cu	217°c	217°c	Eutectic

Water soluble and no clean flux can be used. In case of water soluble flux, remove the flux immediately after reflow to avoid the potential issue of leakage current between pads.

Stencil design rules in function of the quality :



INOX LASER: [(L*W)/(2*(L+W)*T)] > 0.66 & W > 1.5*T

NICKEL LASER: [(L*W)/(2*(L+W)*T)] > 0.53 & W > 1.2*T

ELECTROFORMED: [(L*W)/(2*(L+W)*T)] > 0.44 & W > 1.0*T

And in all cases : W > 5 * powder size

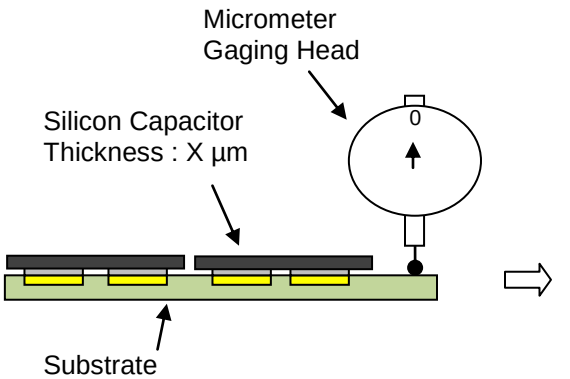
A solder joint thickness of 40µm +/-10 is targeted to limit the risk of contact between the solder paste and the side of the capacitor. Such a contact would have a negative effect and would probably create a high leakage or a short circuit. Limited solder joint thickness will also avoid an excessive tilting of the capacitor.

For example, design of stencils done by IPDiA (SAC305 type 6 with 50% of flux):

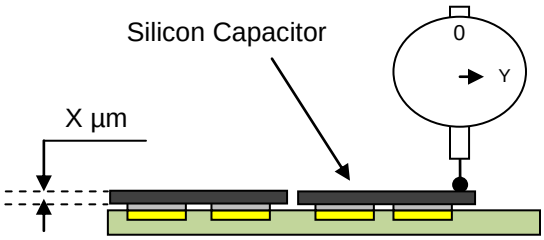
Silicon Capacitor Type	Stencil opening size µm²	Stencil thickness µm	Stencil quality
0201	150 x 320	100	ELECTROFORMED
0402	260 x 369	125	NICKEL LASER
0603	300 x 768	125	NICKEL LASER
0805	400 x 960	125	NICKEL LASER
1206	500 x 1229	125	NICKEL LASER
1812	700 x 2798	125	NICKEL LASER

Procedure for the solder joint measurement (After reflow):

STEP 1:



STEP 2:



Y µm (Measured value)
\- X µm (Capacitor thickness)
40µm (Solder joint thickness)

Pick and Place

The most common approach is with automatic equipment using vision assist to correct placement after picking but manual placement can also be done.
Using a rubber tip is particularly preferred for the die manipulation.
A minimum pressure of 50 grams and a maximum of 150 grams is recommended for the die placement on the solder paste.

Reflow soldering

IPDiA recommends convection reflow but vapor phase reflow and infrared reflow could be also used.
The reflow has to be done conforming with the standard JEDEC.

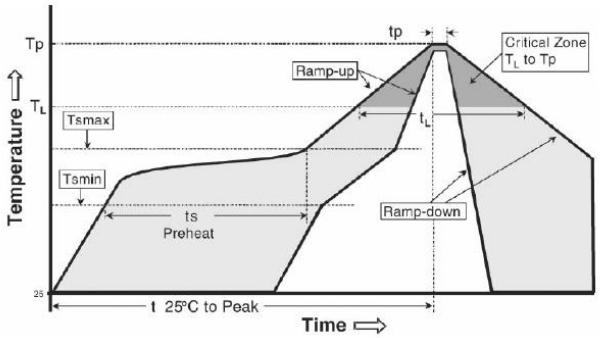


Figure 4: Generic reflow profile according to JEDEC J-STD-020-C

PROFILE FEATURE	SnPb 63/37	SAC305 (Lead-Free Assembly)
Preheat/soak		
Temperature min (Ts min)	100°C	150°C
Temperature max (Ts max)	150°C	200°C
Time (ts) from (Ts min to Ts max)	60 to 120s	60 to 120s
Ramp-up		
Ramp-up rate (tL to tp)	3°C/s maximum	3°C/s maximum
Liquidus temperature(TL)	183°C	217°C
Time (tL) maintained above TL	60s to 150s	60s to 150s
Peak temperature (Tp)	220°C	260°C
Time 25°C to peak temperature	6 minutes maximum	8 minutes maximum
Ramp-down		
Ramp-down rate (Tp to TL)	6°C/s maximum	6°C/s maximum

Flux removes tarnish films, maintains surface cleanliness and facilitates solder spread during attachment operations. The flux must be compatible with the soldering temperature and soldering times. In case of water soluble flux, please refer to the solder paste supplier for the cleaning and flux removal. Flux residues could be responsible for current leakage or short circuits. For optimum results, clean the circuits immediately after reflow.

Revision

Version	Author	Date	Description
1.0	Mickael POMMIER	28/04/2015	Creation of the document

For more information, please visit: http://www.ipdia.com
To contact us, e-mail: sales@ipdia.com

Release date: April 17th 2014
Document identifier: AN

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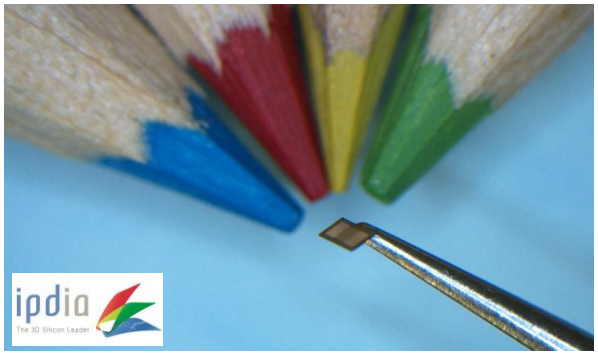

Introduction

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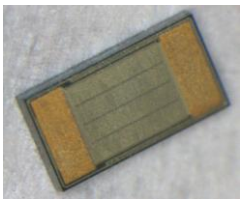
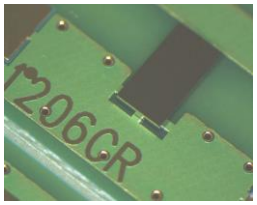


IPDiA Silicon capacitor (1206)



The silicon capacitor mounted on PCB board

Handling precautions and storage

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Store the capacitors in the manufacturer's package in the following conditions without a rapid thermal change in an indoor room:

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To avoid contamination and damage like scratches and cracks, our recommendations are:

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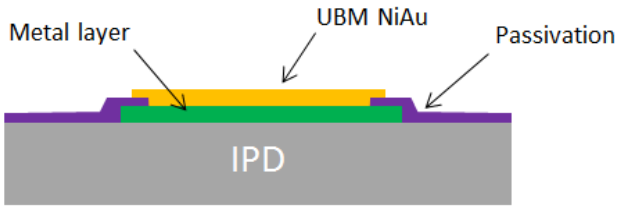

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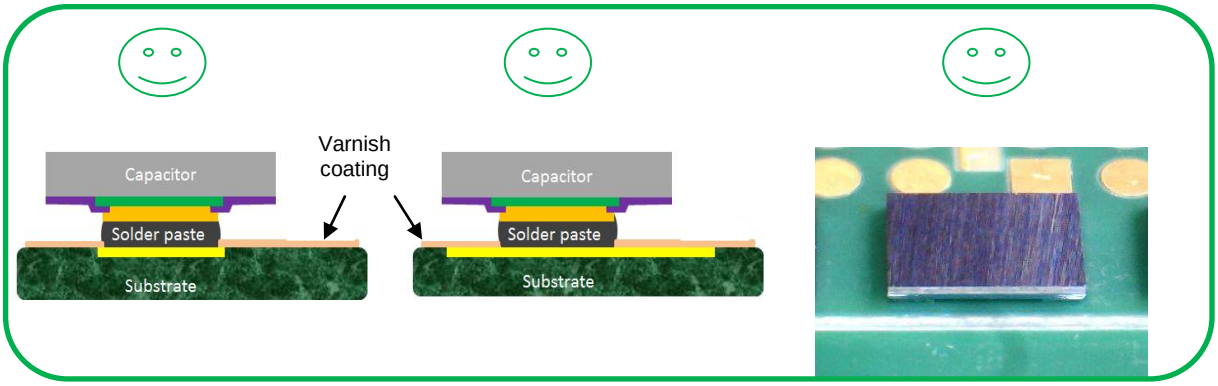


Figure 1: Solder paste after reflow - Targeted

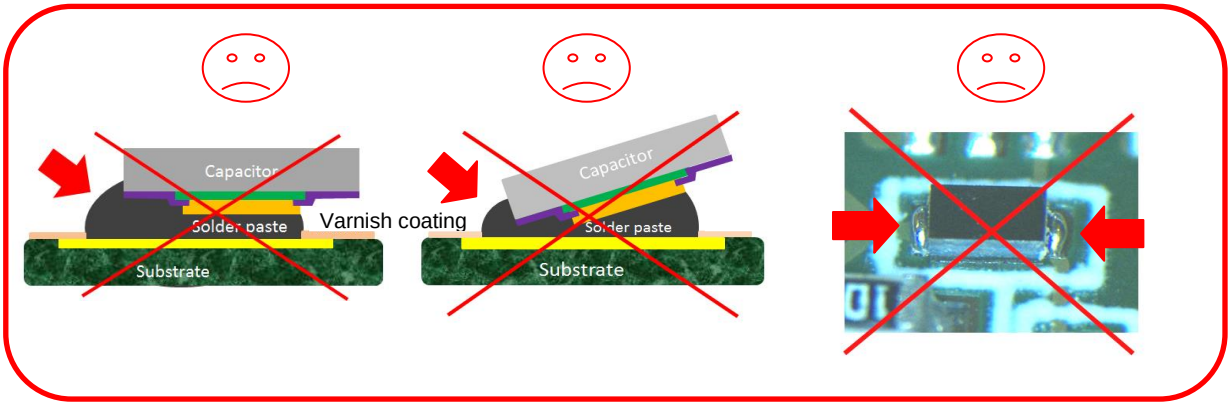


Figure 2: Solder paste after reflow - Rejected

Design of the board:

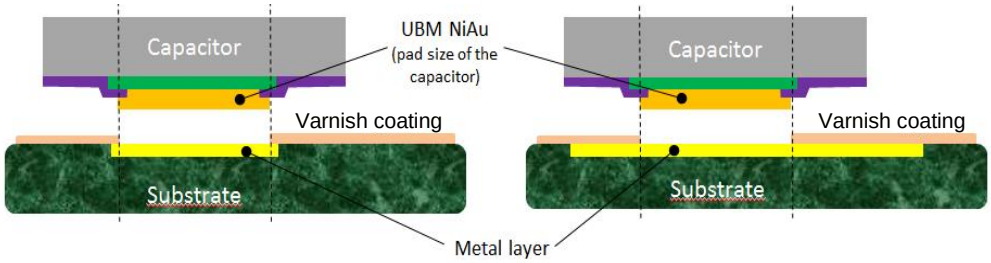
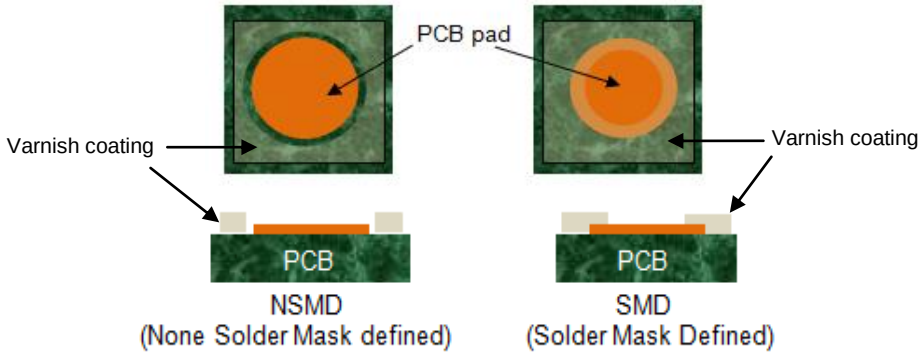
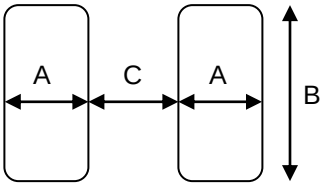


Figure 3: Opening of the metal layer on the customer substrate should match the pad of the silicon die

On the customer substrate, IPDiA recommends SMD (Solder Mask Design) to control the solder flowing on the tracks:



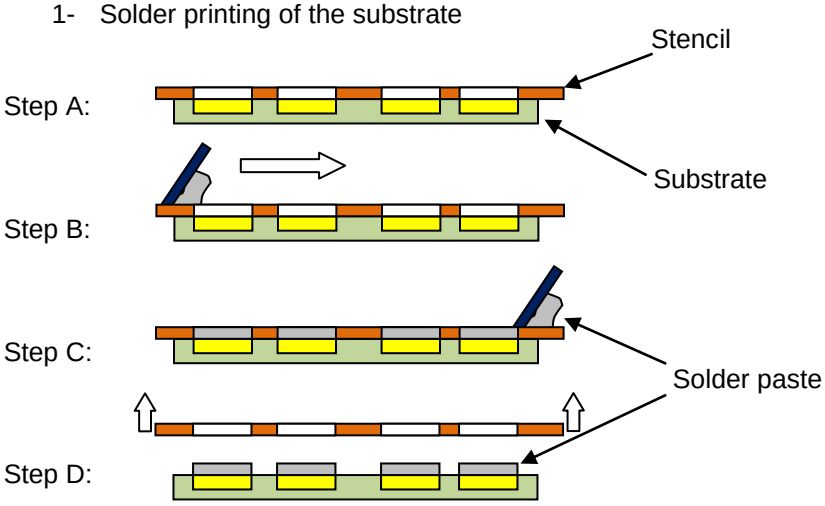
Landing pad for the PCB and die pad dimensions for the IPDiA silicon die:



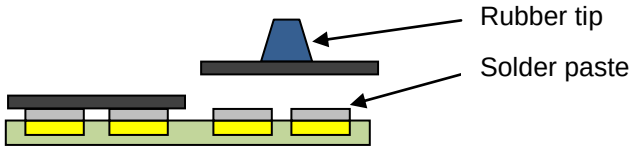
Silicon Capacitor Type	Capacitor size (µm²)	Capacitor thickness	A (µm)	B (µm)	C (µm)
0201	800 x 600	400µm	150	400	300
0402	1200 x 700		300	500	400
0603	1800 x 1100		400	900	800
0805	2200 x 1400		500	1200	1000
1206	3400 x 1800		600	1600	2000
1812	4700 x 3600		900	3400	2700

Process Flow

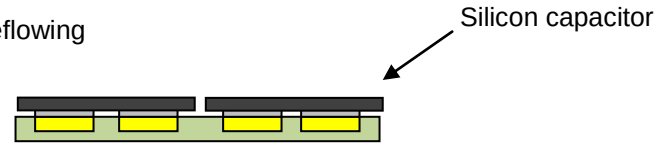
1- Solder printing of the substrate



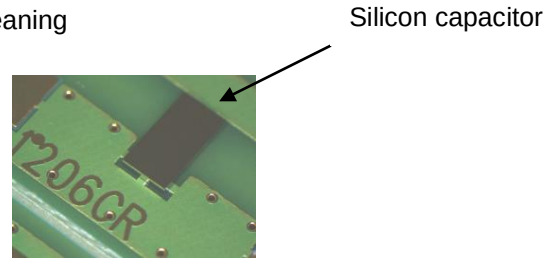
2- Picking of the silicon die and placement



3- Reflowing



4- Cleaning



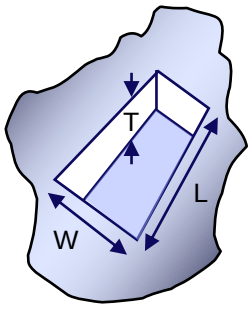
Solder print material and stencil printing recommendations

Solder pastes SnPb63/37 or SAC305 are usually used and recommended but other materials compatible with the die pad finishing are also possible.
In function of the die pad size, powder size could be adjusted.

ALLOY	COMPOSITION	SOLIDUS	LIQUIDUS	COMMENTS
Sn63	63Sn, 37Pb	183°c	183°c	Eutectic
SAC305	96,5Sn, 3Ag, 0.5Cu	217°c	217°c	Eutectic

Water soluble and no clean flux can be used. In case of water soluble flux, remove the flux immediately after reflow to avoid the potential issue of leakage current between pads.

Stencil design rules in function of the quality :



INOX LASER: [(L*W)/(2*(L+W)*T)] > 0.66 & W > 1.5*T

NICKEL LASER: [(L*W)/(2*(L+W)*T)] > 0.53 & W > 1.2*T

ELECTROFORMED: [(L*W)/(2*(L+W)*T)] > 0.44 & W > 1.0*T

And in all cases : W > 5 * powder size

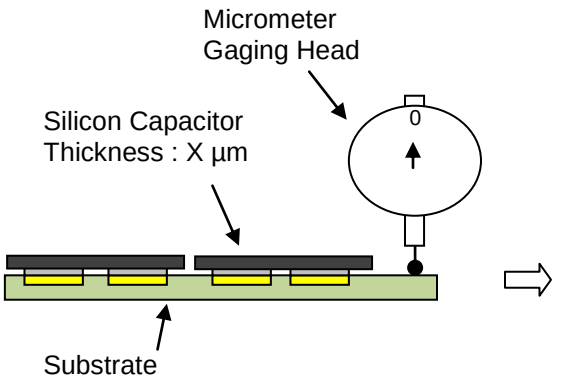
A solder joint thickness of 40µm +/-10 is targeted to limit the risk of contact between the solder paste and the side of the capacitor. Such a contact would have a negative effect and would probably create a high leakage or a short circuit. Limited solder joint thickness will also avoid an excessive tilting of the capacitor.

For example, design of stencils done by IPDiA (SAC305 type 6 with 50% of flux):

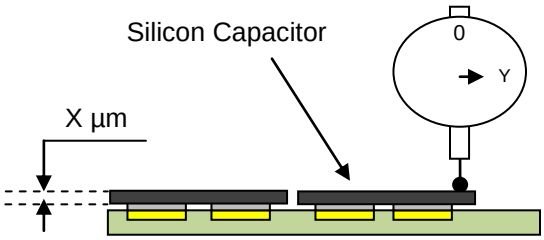
Silicon Capacitor Type	Stencil opening size µm²	Stencil thickness µm	Stencil quality
0201	150 x 320	100	ELECTROFORMED
0402	260 x 369	125	NICKEL LASER
0603	300 x 768	125	NICKEL LASER
0805	400 x 960	125	NICKEL LASER
1206	500 x 1229	125	NICKEL LASER
1812	700 x 2798	125	NICKEL LASER

Procedure for the solder joint measurement (After reflow):

STEP 1:



STEP 2:



Y µm (Measured value)
\- X µm (Capacitor thickness)
40µm (Solder joint thickness)

Pick and Place

The most common approach is with automatic equipment using vision assist to correct placement after picking but manual placement can also be done.
Using a rubber tip is particularly preferred for the die manipulation.
A minimum pressure of 50 grams and a maximum of 150 grams is recommended for the die placement on the solder paste.

Reflow soldering

IPDiA recommends convection reflow but vapor phase reflow and infrared reflow could be also used.
The reflow has to be done conforming with the standard JEDEC.

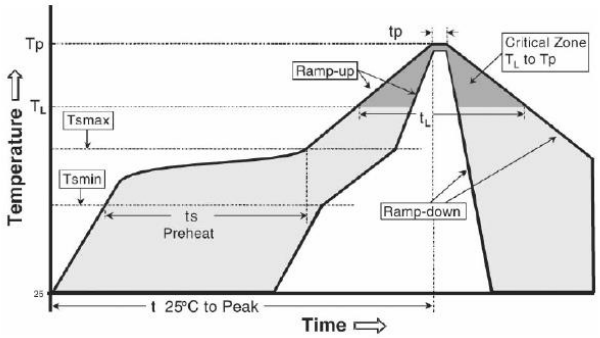


Figure 4: Generic reflow profile according to JEDEC J-STD-020-C

PROFILE FEATURE	SnPb 63/37	SAC305 (Lead-Free Assembly)
Preheat/soak		
Temperature min (Ts min)	100°C	150°C
Temperature max (Ts max)	150°C	200°C
Time (ts) from (Ts min to Ts max)	60 to 120s	60 to 120s
Ramp-up		
Ramp-up rate (tL to tp)	3°C/s maximum	3°C/s maximum
Liquidus temperature(TL)	183°C	217°C
Time (tL) maintained above TL	60s to 150s	60s to 150s
Peak temperature (Tp)	220°C	260°C
Time 25°C to peak temperature	6 minutes maximum	8 minutes maximum
Ramp-down		
Ramp-down rate (Tp to TL)	6°C/s maximum	6°C/s maximum

Flux removes tarnish films, maintains surface cleanliness and facilitates solder spread during attachment operations. The flux must be compatible with the soldering temperature and soldering times. In case of water soluble flux, please refer to the solder paste supplier for the cleaning and flux removal. Flux residues could be responsible for current leakage or short circuits. For optimum results, clean the circuits immediately after reflow.

Revision

Version	Author	Date	Description
1.0	Mickael POMMIER	28/04/2015	Creation of the document

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