

#### DESCRIPTION

The MP6914 is an ideal diode that integrates a 30V, 5.3mΩ power MOSFET to replace bypass diodes in photovoltaic panel. The power loss can be significantly reduced with the MP6914 due to its low voltage drop and reverse leakage current. The part is available with SOIC8-EP package.

#### FEATURES

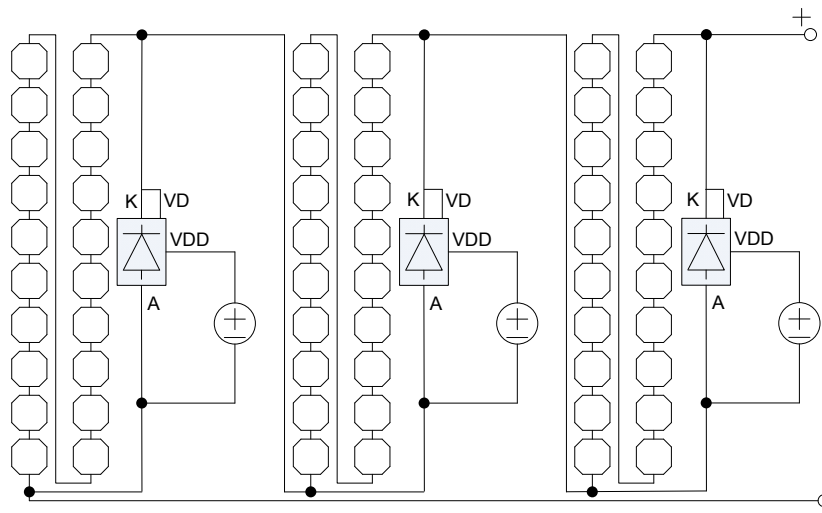
- Integrated 5.3mΩ 30V Power Switch
- Very low reverse leakage current
- Rugged design for long lifetime
- Available in SOIC8-EP package

#### APPLICATIONS

- Bypass diode in photovoltaic panels

All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Quality Assurance. "MPS" and "The Future of Analog IC Technology" are Registered Trademarks of Monolithic Power Systems, Inc.

#### TYPICAL APPLICATION



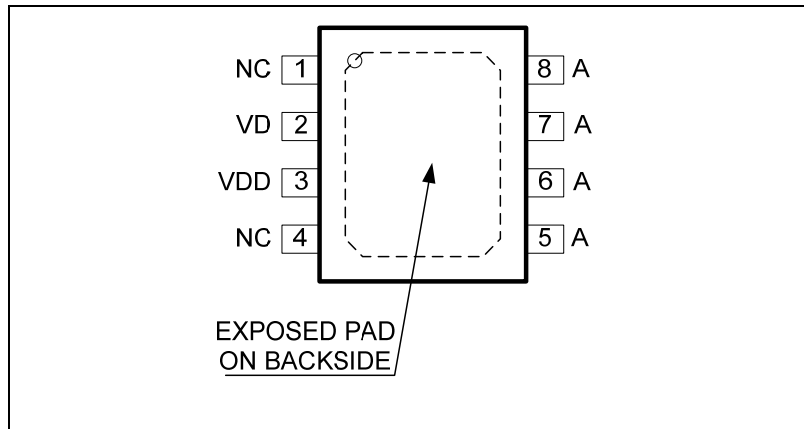
### ORDERING INFORMATION

Part Number*	Package	Top Marking
MP6914DN	SOIC8E	MP6914

\* For Tape & Reel, add suffix –Z (e.g. MP6914DN–Z);

For RoHS, compliant packaging, add suffix –LF (e.g. MP6914DN–LF–Z).

### PACKAGE REFERENCE



#### ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

Cathode to Anode.....	-0.8V to +30V
Continuous Power Dissipation (T <sub>A</sub> = +25°C) <sup>(2)</sup>	2.5W
Junction Temperature.....	150°C
Lead Temperature (Solder).....	260°C
Storage Temperature.....	-55°C to +150°C

#### Recommended Operation Conditions <sup>(3)</sup>

V <sub>DD</sub> to Anode.....	6V to 24V
Operating Junction Temp. (T <sub>J</sub> ). -40°C to +125°C	

Thermal Resistance <sup>(4)</sup>	$\theta_{JA}$	$\theta_{JC}$
SOIC8E.....	50	10 ... °C/W

#### Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature T<sub>J</sub>(MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature T<sub>A</sub>. The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$ . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

$T_A = +25^\circ\text{C}$ , unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VDD Voltage Range	$V_{DD}$		6		24	V
VDD UVLO Rising	$V_{DD\_rs}$		3.4	3.8	4.2	V
VDD UVLO Hysteresis	$V_{DD\_hs}$		0	0.6	1	V
Operating Current	$I_{op}$	$V_{DD}=12\text{V}$ , $V_{AK}=0.5\text{V}$		1	2	mA
Quiescent Current	$I_q$	$V_{DD}=12\text{V}$ , $V_{AK}=0\text{V}$	60	90	120	$\mu\text{A}$
A-K Forward Voltage	$V_{fwd}$	$I_{AK}=1\text{A}$	20	30	40	mV
A-K Forward Voltage	$V_{fwd}$	$I_{AK}=10\text{A}$ , $T_j=25^\circ\text{C}$		53		mV
		$I_{AK}=10\text{A}$ , $T_j=75^\circ\text{C}$		61		mV
Turn-off Total Delay	$T_{Doff}$		2	4	6	$\mu\text{s}$
<b>POWER SWITCH SECTION</b>						
Drain-Source Breakdown Voltage <sup>(5)</sup>	$V_{(BR)DSS}$	$V_{GS}=0\text{V}$ , $I_{KA}=250\mu\text{A}$	30	32		V
Gate-Threshold Voltage	$V_{GS\_th}$	$V_{DS}=V_{GS}$ , $I_{KA}=250\mu\text{A}$		1.9		V
AK Turn-on Threshold	$V_{AK\_ON}$	$V_{DD}=12\text{V}$		125	250	mV
Gate-Body Leakage	$I_{GSS}$	$V_{DS}=0\text{V}$ , $V_{GS}=\pm 12\text{V}$		$\pm 100$		nA
Leakage Current	$I_{LK}$	From K to A, $V_{DD}=0\text{V}$			1	$\mu\text{A}$
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$ , $I_D=10\text{A}$ , $T_j=25^\circ\text{C}$		5.3		$\text{m}\Omega$
		$V_{GS}=10\text{V}$ , $I_D=10\text{A}$ , $T_j=75^\circ\text{C}$		6.1		$\text{m}\Omega$
Input Capacitance	$C_{iss}$	$V_{DS}=30\text{V}$ , $f=1\text{MHz}$		2800		pF
Output Capacitance	$C_{oss}$			450		pF
Reverse Transfer Capacitance	$C_{rss}$			300		pF
<b>Body Diode Characteristics</b>						
Diode Forward Voltage	$V_{AK}$	$V_{DD}=2.5\text{V}$ , $I_{AK}=1\text{A}$		0.7	0.8	V

Note:

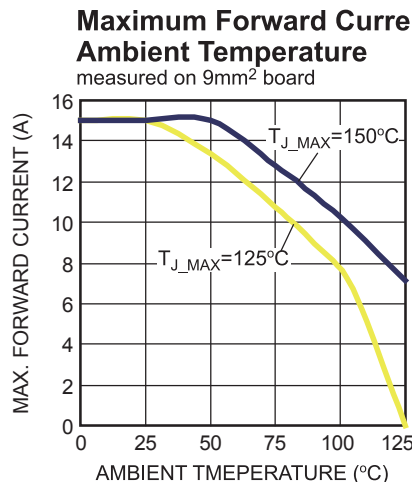
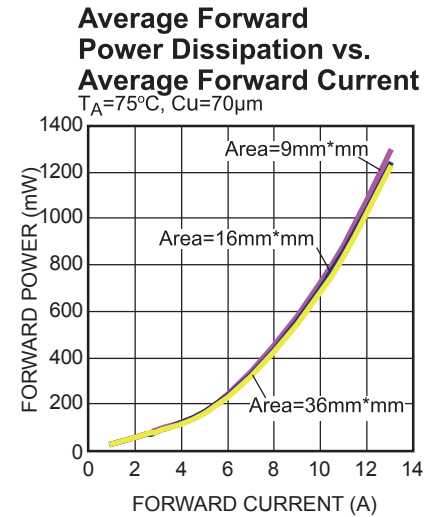
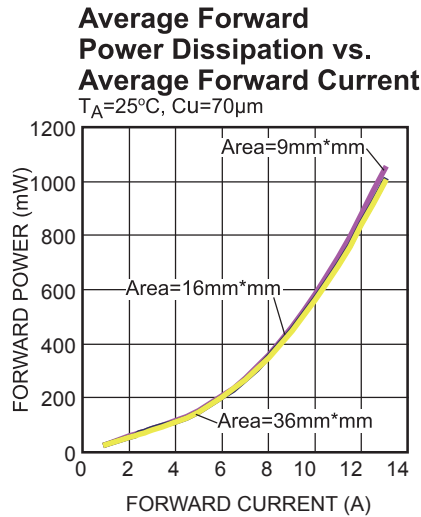
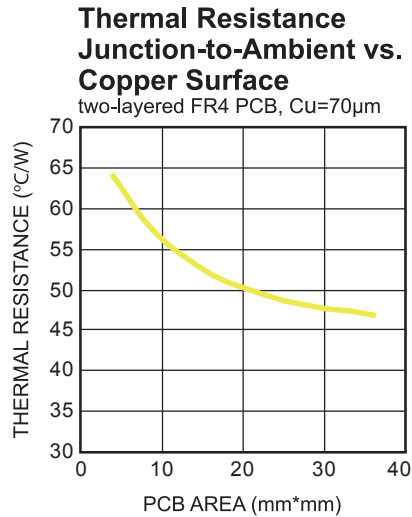
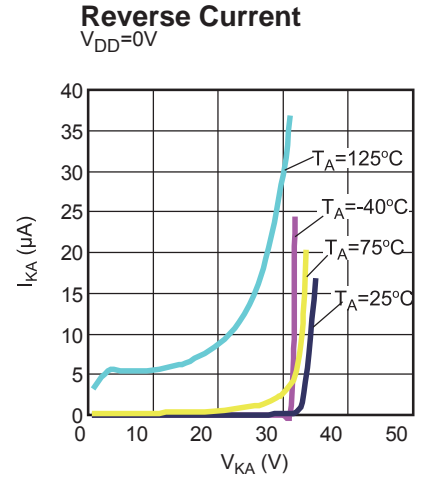
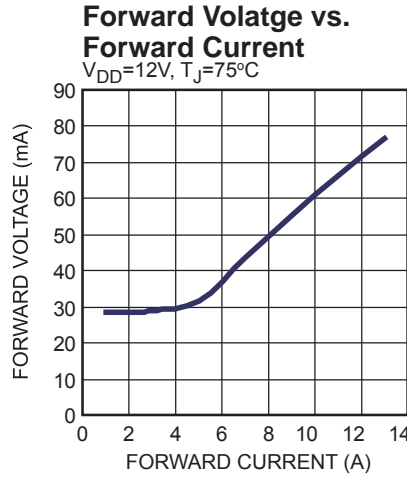
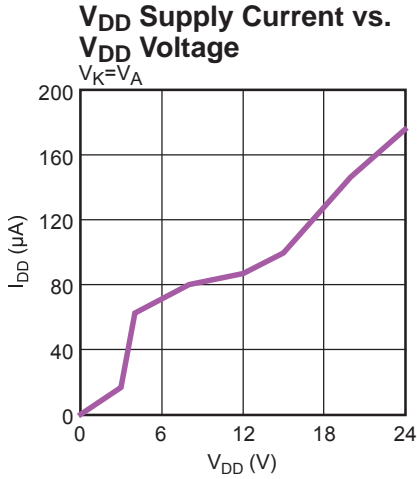
5) D is K, S is A, refer to "BLOCK DIAGRAM"

**PIN FUNCTIONS**

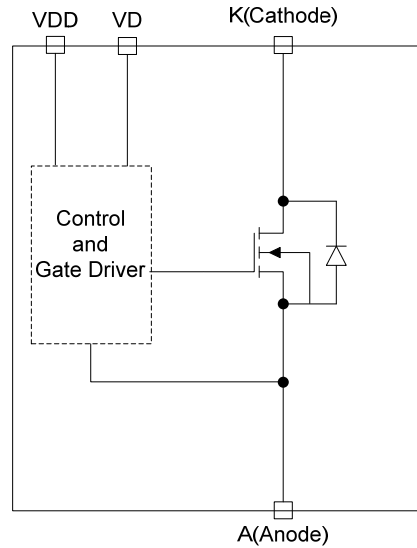
<b>Pin #</b>	<b>Name</b>	<b>Description</b>
1,4	NC	No Connection
2	VD	Drain voltage sense, need to connect K pin.
3	VDD	Supply Voltage, reference to anode.
5-8	A	FET Source, also used as diode anode
EP	K	FET Drain, also used as diode cathode

## TYPICAL PERFORMANCE CHARACTERISTICS

V<sub>DD</sub>=12V, T<sub>A</sub>=+25°C, tested on two-layered FR4 PCB with 70µm Cu, otherwise noted



**BLOCK DIAGRAM**



**Figure 1—Function Block Diagram**

## OPERATION

Photovoltaic cells can not generate power in some conditions, such as clouds or fog. Due to the mismatch currents between the series connected cells, the shaded cells will work like a load while the good cells still produce power. They dissipate power instead of generating power and cause hot spot. To protect the PV from the damage due to hot spot, bypass diodes in PV junction box are commonly used to allow the current pass around the shaded PV cells. MP6914 is comprised of an internal power MOSFET and control circuits. It need an external power for VDD and behaves like a diode. Compared with a bypass diode, MP6914 has significantly low forward voltage drop and a very low reverse leakage current.

### Turn-on Phase

When current goes through the internal body diode, the body diode voltage drop from A to K ( $>500\text{mV}$ ) is much larger than the turn-on threshold ( $125\text{mV}$ ) of internal control circuitry, which leads to the turn on of the internal MOSFET. The control circuitry will regulate the  $V_{AK}$  at about  $30\text{mV}$  by controlling the gate driver voltage of the internal MOSFET.

### Turn-off Phase

When the shaded PV cells start to generate power (this means the voltage which drops across A-K is smaller than  $30\text{mV}$ ), the control circuitry stops working and the internal MOSFET is turned off.

## APPLICATION INFORMATION

### Loss Calculation

The MP6914 provide solutions for photovoltaic applications, designed to increase system efficiency by implementing a bypass function through a 5.3mΩpower MOSFET transistor instead of a conventional Schottky diode.

MP6914 should be connected in parallel to the cell string which is intended to be protected. In normal work this string produce enery with a voltage  $V_{KA}$ . In normal work MP6914 consumes a power determined by:

$$P_{LOSS}(W) = V_{KA}(V) * I_{KA}(\mu A) * 10^{-6}$$

Where  $I_{KA}$  is the reverse current (see Figure 3), typically  $<3\mu A$ , so  $P_{LOSS}$  is very small.

When this cell string is shaded to act as a load of other cells, MP6914 will turn on the internal MOSFET to prevent hot-spot issue. Now  $I_{KA}$  is the negative forward current  $I_F$  (typically 0~10A), equal to current in the real load of PV cells.  $V_{KA}$  is the negative forward voltage  $V_F$ .if  $I_F$  is below 5A,  $V_F$  is clamped to about 30mV, otherwise can be found in Figure “Forward Voltage vs. Forward Current”. Then substituting  $V_F$  and  $I_F$  into previous equation can calculate out the loss in this case.

$P_{LOSS}$  (W),  $\theta_{JA}$  (45-65°C/W), ambient temperature  $T_a$  (°C) and maximum allowed junction temperature (150°C) decide the maximum  $I_F$  (A). In common case, this relation can be expressed:

$$I_F = (150 - T_a) / (\theta_{JA} * V_F * 0.001)$$

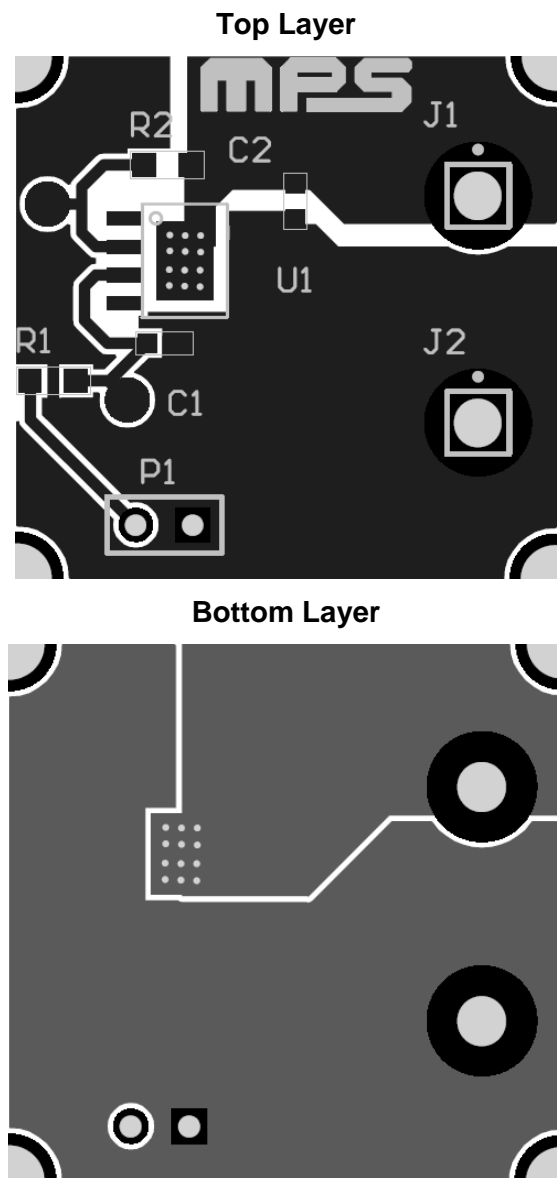
Where  $V_F$  in mV, and can be found in the anterior Figure “Forward Voltage vs. Forward Current”, and the maximum  $I_F$  is sketched in Figure “Maximum Forward Current vs. Ambient Temperature”.

### Component Selection

A small capacitor is needed to keep a clean voltage for  $V_{DD}$  pin, 0.1μF is enough. A resistor of 1kΩ is needed between  $V_D$  and K pins in order to prevent noise from PV cells line. This resistor doesn't consume power.

### PCB Layout Guide

As usually the current flowing into A pin through K pin is big, the copper plane connected to these pins is recommended as big as possible, as shown in the figures below:





The  $V_{DD}$  decoupling capacitor should be closed to  $V_{DD}$  and A pins (C1 in the upper figure). The  $V_D$  resistor (R2 in the upper figure) connects a joint close to K pin and keeps the  $V_D$  trace short. MP6914DN-00A is a good example.

And many vias from top layer through bottom layer needed for current conducting and thermal radiating.

### Design Example

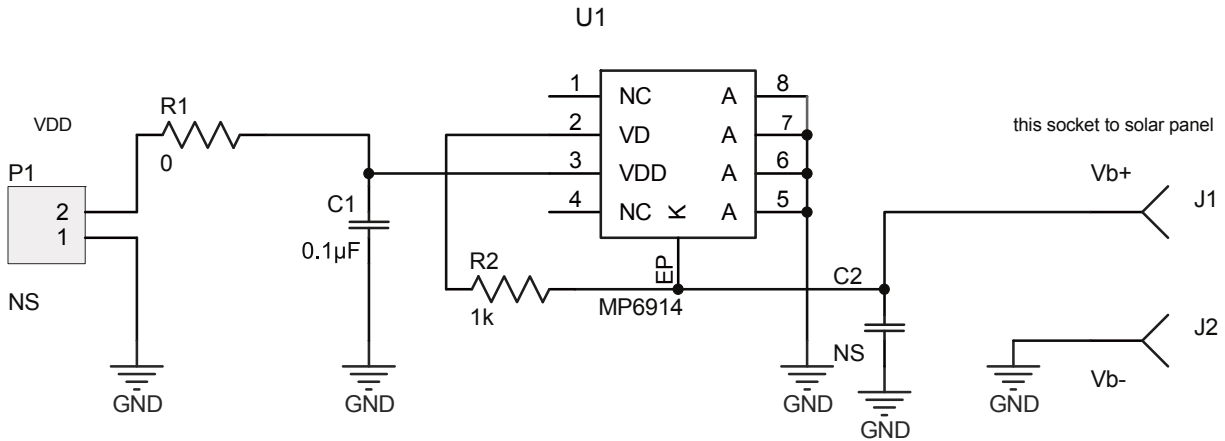
Below is a design example following the application guidelines for the specifications:

**Table 1: Design Example**

$V_{DD}$ (V)	6-24
$V_b$ (V)	-0.8-30
$I_b$ ( $I_{AK}$ : A)	0-10

The detailed application schematic is shown in figure 2. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device applications, please refer to the related Evaluation Board Datasheets.

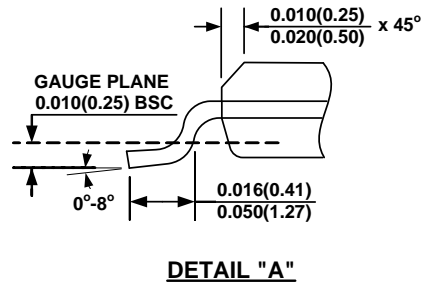
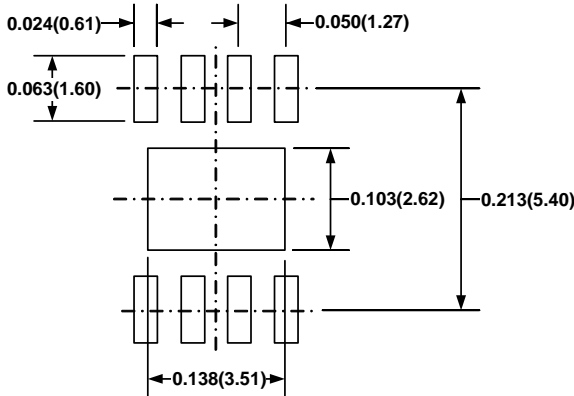
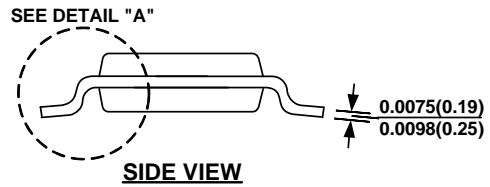
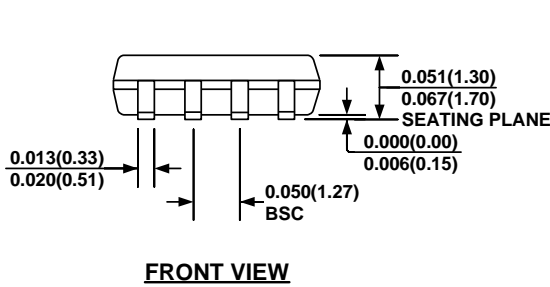
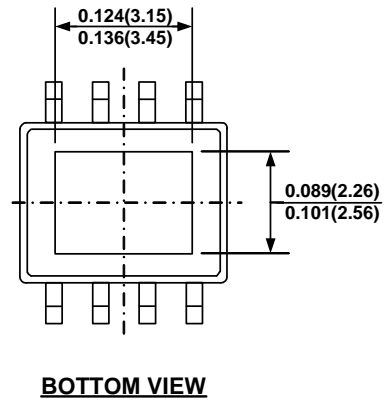
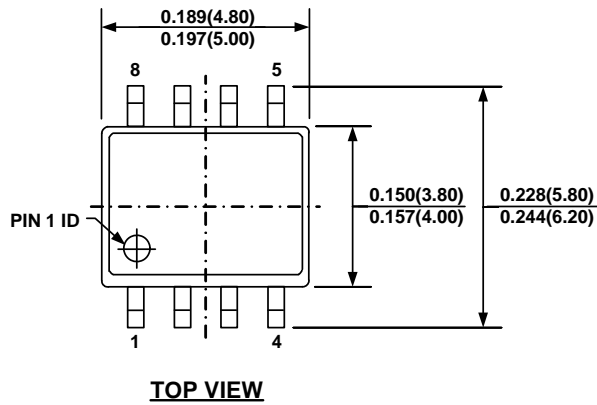
## TYPICAL APPLICATION CIRCUITS



**Figure 2—24V/10A Application Circuit**

## PACKAGE INFORMATION

## SOIC8E


**NOTE:**

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
- 6) DRAWING IS NOT TO SCALE.

**NOTICE:** The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Monolithic Power Systems \(MPS\):](#)

[MP6914DN-LF](#) [MP6914DN-LF-Z](#)