



P-Channel Enhancement-Mode Vertical DMOS FET

Features

- ▶ Low threshold (-2.0V max.)
- ▶ High input impedance
- ▶ Low input capacitance
- ▶ Fast switching speeds
- ▶ Low on-resistance
- ▶ Free from secondary breakdown
- ▶ Low input and output leakage

Applications

- ▶ Logic level interfaces - ideal for TTL and CMOS
- ▶ Solid state relays
- ▶ Battery operated systems
- ▶ Photo voltaic drives
- ▶ Analog switches
- ▶ General purpose line drivers
- ▶ Telecom switches

Ordering Information

Part Number	Package Option	Packing
TP2640LG-G	8-Lead SOIC	2500/Reel
TP2640N3-G	3-Lead TO-92	1000/Bag
TP2640N3-G P002	3-Lead TO-92	2000/Reel
TP2640N3-G P003		
TP2640N3-G P005		
TP2640N3-G P013		
TP2640N3-G P014		

-G denotes a lead (Pb)-free / RoHS compliant package.

Contact factory for Wafer / Die availability.

Devices in Wafer / Die form are lead (Pb)-free / RoHS compliant.

Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	BV_{DSS}
Drain-to-gate voltage	BV_{DGS}
Gate-to-source voltage	$\pm 20V$
Operating and storage temperature	-55°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Typical Thermal Resistance

Package	θ_{ja}
8-Lead SOIC	101°C/W
TO-92	132°C/W

General Description

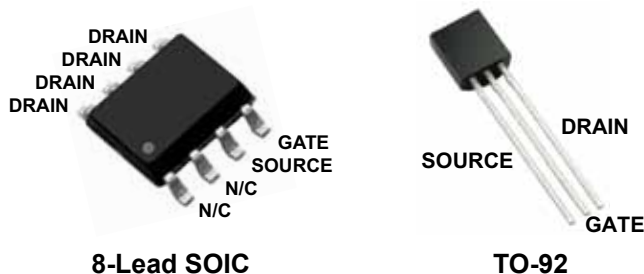
This low threshold, enhancement-mode (normally-off) transistor utilizes a vertical DMOS structure and Supertex's well-proven, silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Product Summary

BV_{DSS}/BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)
-400V	15Ω	-2.0A	-0.7V

Pin Configuration



Product Marking



YY = Year Sealed
WW = Week Sealed
L = Lot Number
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

8-Lead SOIC



YY = Year Sealed
WW = Week Sealed
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

TO-92

Thermal Characteristics

Package	I_D (continuous) [†]	I_D (pulsed)	Power Dissipation @ $T_A = 25^\circ\text{C}$	I_{DR} [†]	I_{DRM}
8-Lead SOIC	-86mA	-600mA	0.74W [‡]	-86mA	-600mA
TO-92	-180mA	-0.8mA	1.0W	-180mA	-0.8mA

[†] I_D (continuous) is limited by max rated T_J .

[‡] Mounted on FR5 board, 25mm x 25mm x 1.57mm.

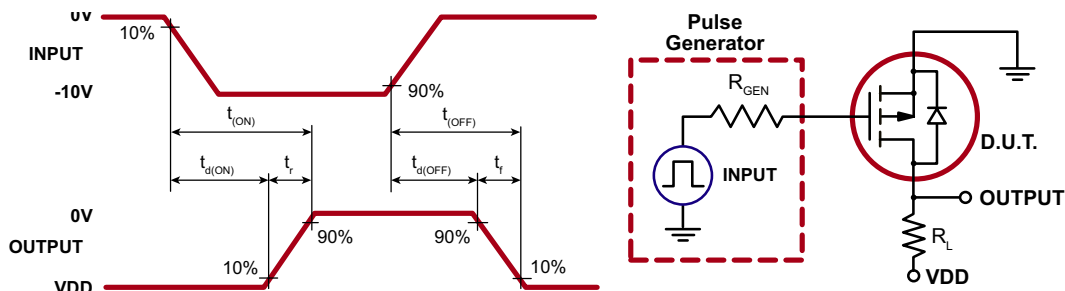
Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	-400	-	-	V	$V_{GS} = 0V, I_D = -2.0mA$
$V_{GS(th)}$	Gate threshold voltage	-0.8	-	-2.0	V	$V_{GS} = V_{DS}, I_D = -1.0mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-	5.0	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = -1.0mA$
I_{GSS}	Gate body leakage	-	-	-100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	-	-	-1.0	μA	$V_{GS} = 0V, V_{DS} = -100V$
				-10.0	μA	$V_{GS} = 0V, V_{DS} = \text{Max rating}$
				-1.0	mA	$V_{DS} = 0.8 \text{ Max Rating}, V_{GS} = 0V, T_A = 125^\circ\text{C}$
$I_{D(ON)}$	On-state drain current	-0.7	-	-	A	$V_{GS} = -10V, V_{DS} = -25V$
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	12	15	Ω	$V_{GS} = -2.5V, I_D = -20mA$
			11	15		$V_{GS} = -4.5V, I_D = -150mA$
			11	15		$V_{GS} = -10V, I_D = -300mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	0.75	%/ $^\circ\text{C}$	$V_{GS} = -10V, I_D = -300mA$
G_{FS}	Forward transconductance	200	-	-	mmho	$V_{DS} = -25V, I_D = -300mA$
C_{ISS}	Input capacitance	-	-	300	pF	$V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz$
C_{OSS}	Common source output capacitance	-	-	50		
C_{RSS}	Reverse transfer capacitance	-	-	12		
$t_{d(ON)}$	Turn-on delay time	-	-	10	ns	$V_{DD} = -25V, I_D = -300mA, R_{GEN} = 25\Omega$
t_r	Rise time	-	-	15		
$t_{d(OFF)}$	Turn-off delay time	-	-	60		
t_f	Fall time	-	-	40		
V_{SD}	Diode forward voltage drop	-	-	-1.8	V	$V_{GS} = 0V, I_{SD} = -200mA$
t_{rr}	Reverse recovery time	-	300	-	ns	$V_{GS} = 0V, I_{SD} = -200mA$

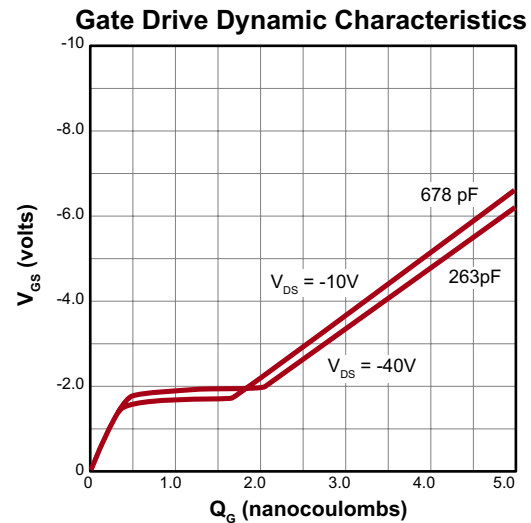
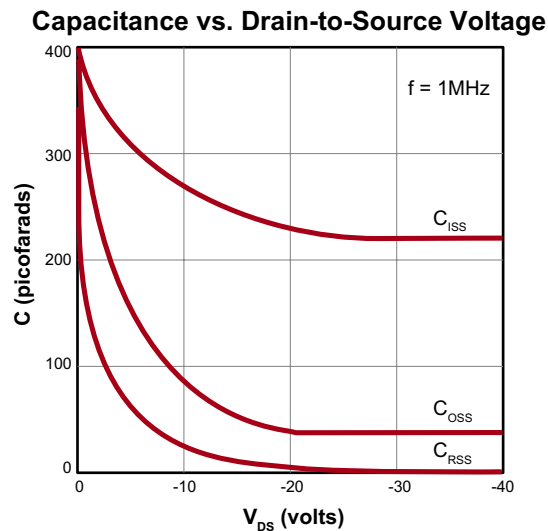
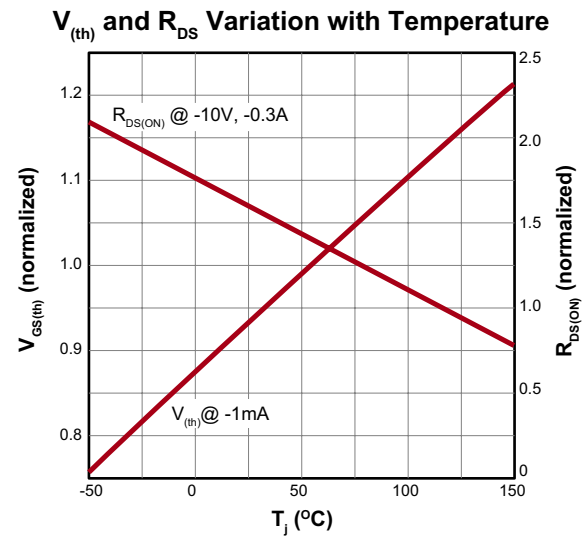
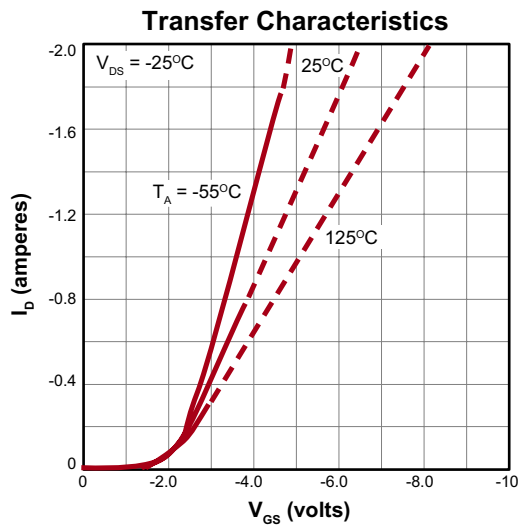
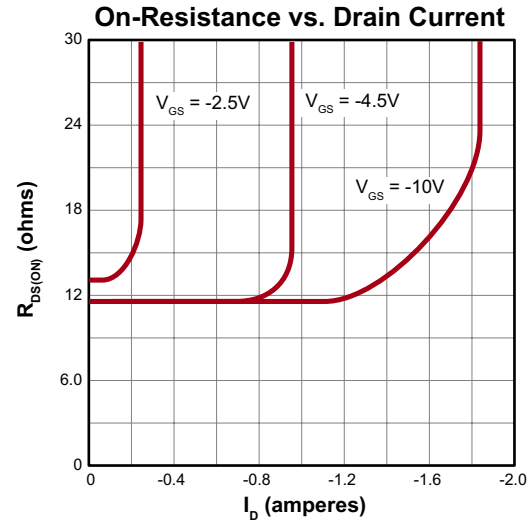
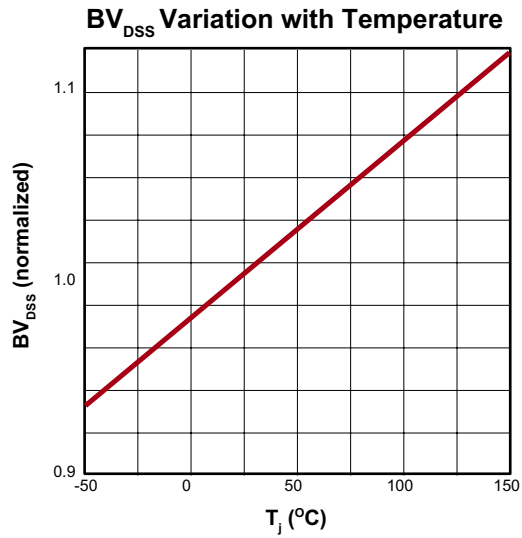
Notes:

1. All D.C. parameters 100% tested at 25C unless otherwise stated. (Pulse test: 300s pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

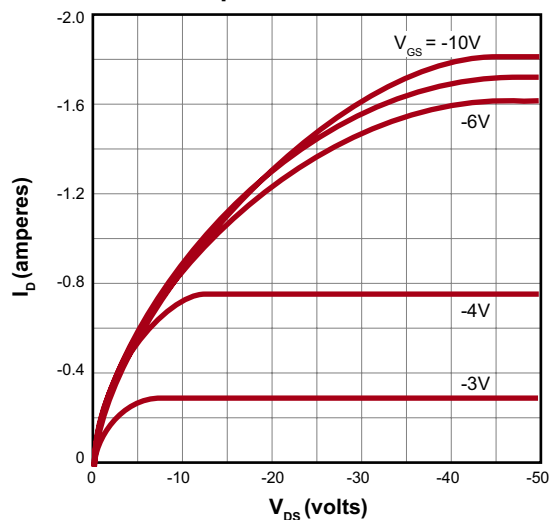


Typical Performance Curves

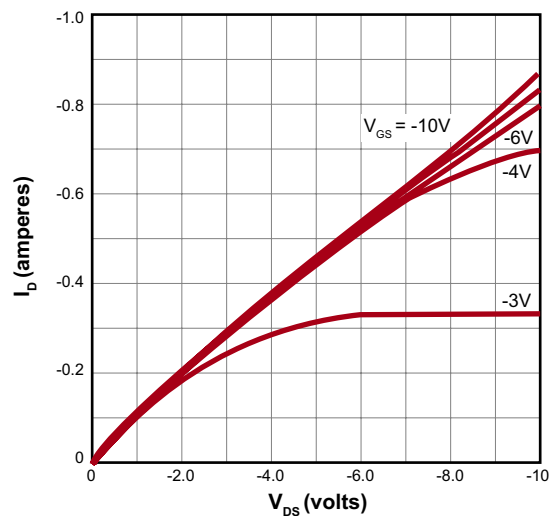


Typical Performance Curves (cont.)

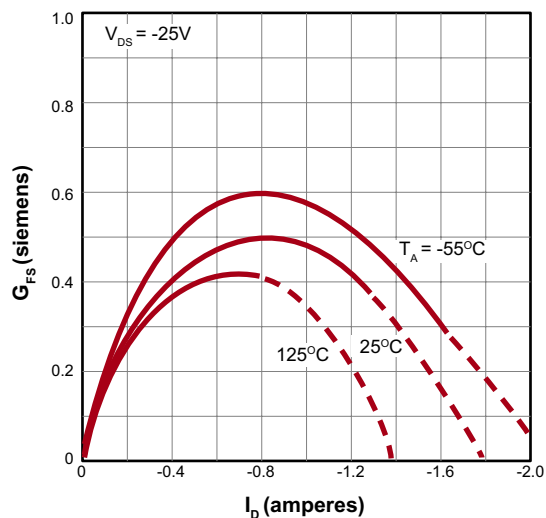
Output Characteristics



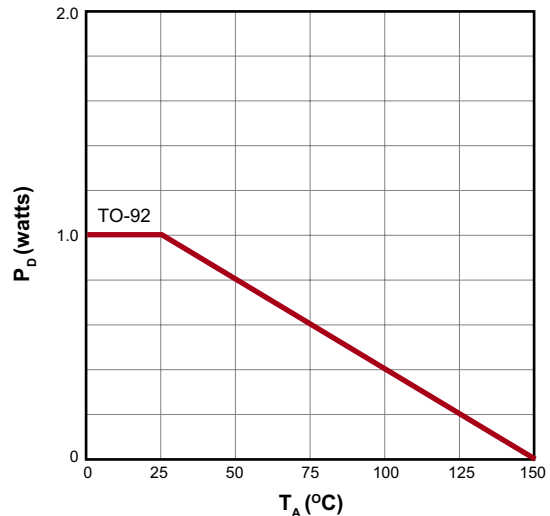
Saturation Characteristics



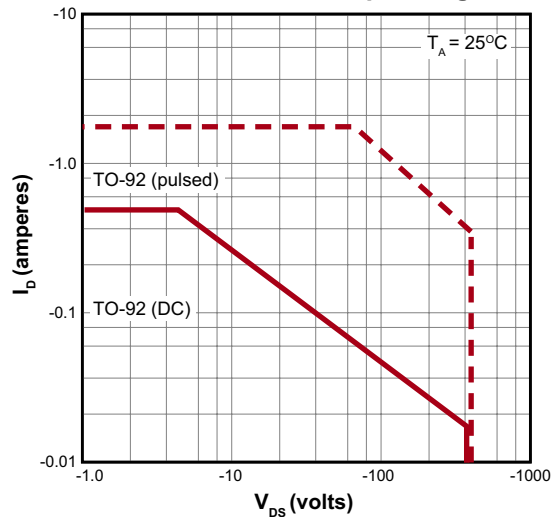
Transconductance vs. Drain Current



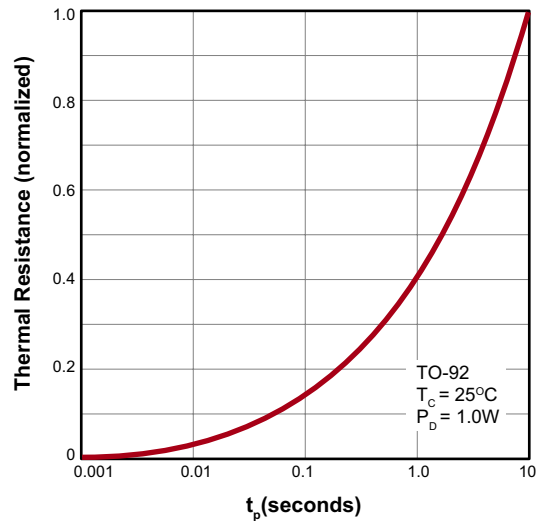
Power Dissipation vs. Temperature



Maximum Rated Safe Operating Area

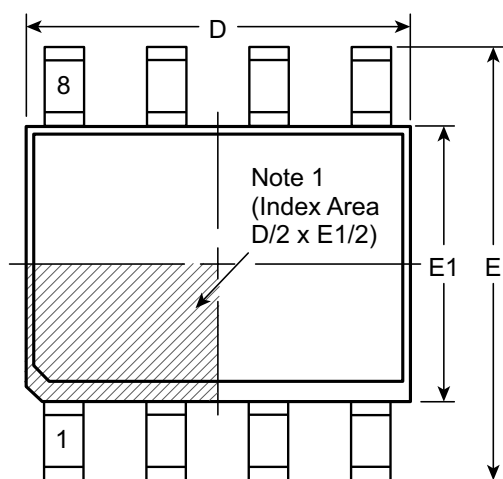


Thermal Response Characteristics

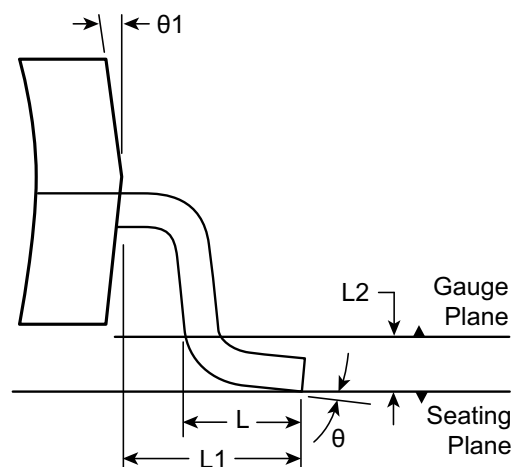


8-Lead SOIC (Narrow Body) Package Outline (LG)

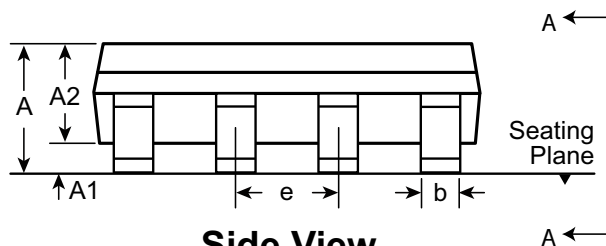
4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



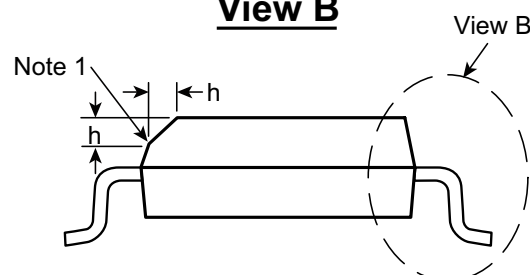
Top View



View B



Side View



View A-A

Note:

1. This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8°	15°

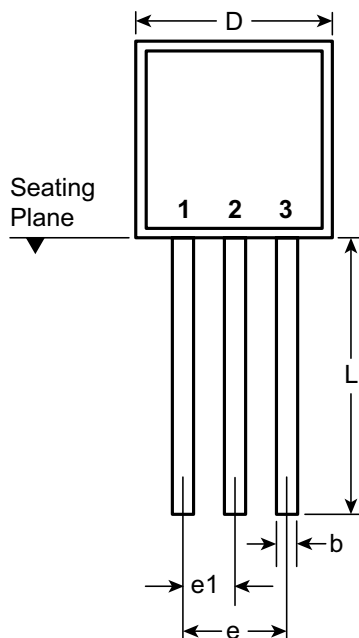
JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.

* This dimension is not specified in the JEDEC drawing.

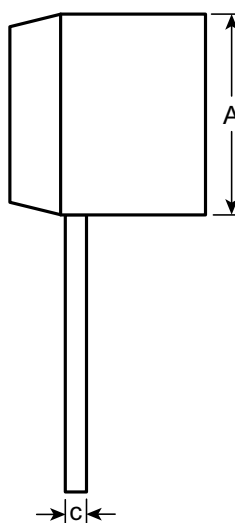
Drawings are not to scale.

Supertex Doc. #: DSPD-8SOLGTG, Version I041309.

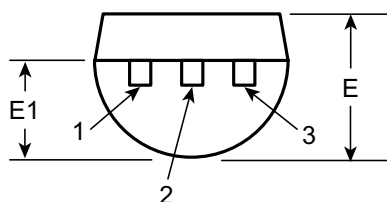
3-Lead TO-92 Package Outline (N3)



Front View



Side View



Bottom View

Symbol		A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014 [†]	.014 [†]	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022 [†]	.022 [†]	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.

* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

Supertex Doc.#: DSPD-3TO92N3, Version E041009.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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[P002](#) [TP2640N3-G P013](#)