Lead-Free Package Options Available!

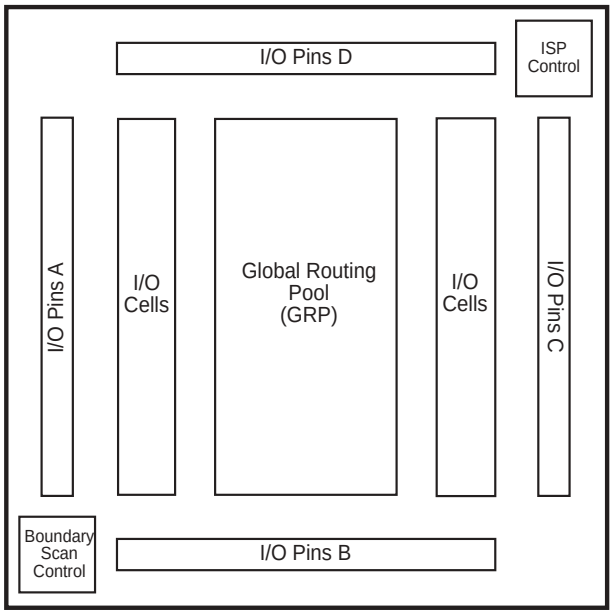
ispGDX®80VA

In-System Programmable 3.3V Generic Digital Crosspoint

Features

- **IN-SYSTEM PROGRAMMABLE GENERIC DIGITAL CROSSPOINT FAMILY**
  - **— Advanced Architecture Addresses Programmable PCB Interconnect, Bus Interface Integration and Jumper/Switch Replacement**
  - **— "Any Input to Any Output" Routing**
  - **— Fixed HIGH or LOW Output Option for Jumper/DIP Switch Emulation**
  - **— Space-Saving PQFP and BGA Packaging**
  - **— Dedicated IEEE 1149.1-Compliant Boundary Scan Test**
- **HIGH PERFORMANCE E^2CMOS® TECHNOLOGY**
  - **— 3.3V Core Power Supply**
  - **— 3.0ns Input-to-Output/3.0ns Clock-to-Output Delay**
  - **— 250MHz Maximum Clock Frequency**
  - **— TTL/3.3V/2.5V Compatible Input Thresholds and Output Levels (Individually Programmable)**
  - **— Low-Power: 16.5mA Quiescent Icc**
  - **— 24mA I_{OL} Drive with Programmable Slew Rate Control Option**
  - **— PCI Compatible Drive Capability**
  - **— Schmitt Trigger Inputs for Noise Immunity**
  - **— Electrically Erasable and Reprogrammable**
  - **— Non-Volatile E^2CMOS Technology**
- **ispGDXV OFFERS THE FOLLOWING ADVANTAGES**
  - **— 3.3V In-System Programmable Using Boundary Scan Test Access Port (TAP)**
  - **— Change Interconnects in Seconds**
- **FLEXIBLE ARCHITECTURE**
  - **— Combinatorial/Latched/Registered Inputs or Outputs**
  - **— Individual I/O Tri-state Control with Polarity Control**
  - **— Dedicated Clock/Clock Enable Input Pins (two) or Programmable Clocks/Clock Enables from I/O Pins (20)**
  - **— Single Level 4:1 Dynamic Path Selection (Tpd = 3.0ns)**
  - **— Programmable Wide-MUX Cascade Feature Supports up to 16:1 MUX**
  - **— Programmable Pull-ups, Bus Hold Latch and Open Drain on I/O Pins**
  - **— Outputs Tri-state During Power-up ("Live Insertion" Friendly)**
- **LEAD-FREE PACKAGE OPTIONS**

Functional Block Diagram



Description

The ispGDXVA architecture provides a family of fast, flexible programmable devices to address a variety of system-level digital signal routing and interface requirements including:

- Multi-Port Multiprocessor Interfaces
- Wide Data and Address Bus Multiplexing (e.g. 16:1 High-Speed Bus MUX)
- Programmable Control Signal Routing (e.g. Interrupts, DMAREQs, etc.)
- Board-Level PCB Signal Routing for Prototyping or Programmable Bus Interfaces

The devices feature fast operation, with input-to-output signal delays (Tpd) of 3.0ns and clock-to-output delays of 3.0ns.

The architecture of the devices consists of a series of programmable I/O cells interconnected by a Global Routing Pool (GRP). All I/O pin inputs enter the GRP directly or are registered or latched so they can be routed to the required I/O outputs. I/O pin inputs are defined as four sets (A,B,C,D) which have access to the four MUX inputs

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Description (Continued)

found in each I/O cell. Each output has individual, programmable I/O tri-state control (OE), output latch clock (CLK), clock enable (CLKEN), and two multiplexer control (MUX0 and MUX1) inputs. Polarity for these signals is programmable for each I/O cell. The MUX0 and MUX1 inputs control a fast 4:1 MUX, allowing dynamic selection of up to four signal sources for a given output. A wider 16:1 MUX can be implemented with the MUX expander feature of each I/O and a propagation delay increase of 2.0ns. OE, CLK, CLKEN, and MUX0 and MUX1 inputs can be driven directly from selected sets of I/O pins. Optional dedicated clock input pins give minimum clock-to-output delays. CLK and CLKEN share the same set of I/O pins. CLKEN disables the register clock when CLKEN = 0.

Through in-system programming, connections between I/O pins and architectural features (latched or registered inputs or outputs, output enable control, etc.) can be defined. In keeping with its data path application focus, the ispGDXVA devices contain no programmable logic arrays. All input pins include Schmitt trigger buffers for noise immunity. These connections are programmed into the device using non-volatile E^2CMOS technology. Non-volatile technology means the device configuration is saved even when the power is removed from the device.

In addition, there are no pin-to-pin routing constraints for 1:1 or 1:n signal routing. That is, *any* I/O pin configured as an input can drive one or more I/O pins configured as outputs.

The device pins also have the ability to set outputs to fixed HIGH or LOW logic levels (Jumper or DIP Switch mode). Device outputs are specified for 24mA sink and 12mA source current (at JEDEC LVTTL levels) and can be tied together in parallel for greater drive. On the ispGDXVA, each I/O pin is individually programmable for 3.3V or 2.5V output levels as described later. Programmable output slew rate control can be defined independently for each I/O pin to reduce overall ground bounce and switching noise.

All I/O pins are equipped with IEEE1149.1-compliant Boundary Scan Test circuitry for enhanced testability. In addition, in-system programming is supported through the Test Access Port via a special set of private commands.

The ispGDXVA I/Os are designed to withstand "live insertion" system environments. The I/O buffers are disabled during power-up and power-down cycles. When designing for "live insertion," absolute maximum rating conditions for the Vcc and I/O pins must still be met.

Table 1. ispGDXVA Family Members

	ispGDXV/VA Device		
	ispGDX80VA	ispGDX160V/VA	ispGDX240VA
I/O Pins	80	160	240
I/O-OE Inputs*	20	40	60
I/O-CLK / CLKEN Inputs*	20	40	60
I/O-MUXsel1 Inputs*	20	40	60
I/O-MUXsel2 Inputs*	20	40	60
Dedicated Clock Pins**	2	4	4
EPEN	1	1	1
TOE	1	1	1
BSCAN Interface	4	4	4
$\overline{\text{RESET}}$	1	1	1
Pin Count/Package	100-Pin TQFP	208-Pin PQFP 208-Ball fpBGA 272-Ball BGA	388-Ball fpBGA

* The CLK/CLK_EN, OE, MUX0 and MUX1 terminals on each I/O cell can each be assigned to 25% of the I/Os.

** Global clock pins Y0, Y1, Y2 and Y3 are multiplexed with CLKEN0, CLKEN1, CLKEN2 and CLKEN3 respectively in all devices.

Architecture

The ispGDXVA architecture is different from traditional PLD architectures, in keeping with its unique application focus. The block diagram is shown below. The programmable interconnect consists of a single Global Routing Pool (GRP). Unlike ispLSI® devices, there are no programmable logic arrays on the device. Control signals for OEs, Clocks/Clock Enables and MUX Controls must come from designated sets of I/O pins. The polarity of these signals can be independently programmed in each I/O cell.

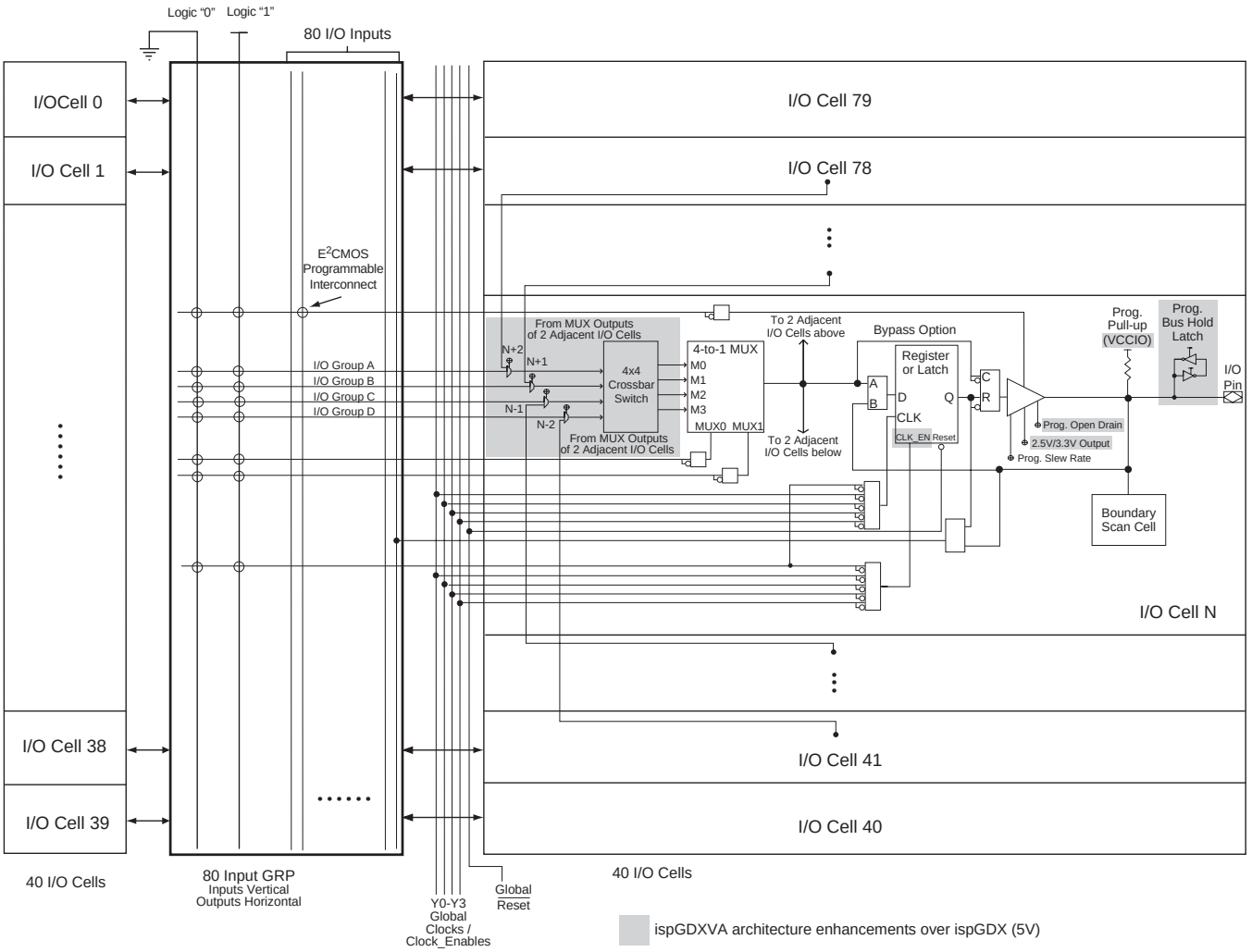
Each I/O cell drives a unique pin. The OE control for each I/O pin is independent and may be driven via the GRP by one of the designated I/O pins (I/O-OE set). The I/O-OE set consists of 25% of the total I/O pins. Boundary Scan test is supported by dedicated registers at each I/O pin. In-system programming is accomplished through the standard Boundary Scan protocol.

The various I/O pin sets are also shown in the block diagram below. The A, B, C, and D I/O pins are grouped together with one group per side.

I/O Architecture

Each I/O cell contains a 4:1 dynamic MUX controlled by two select lines as well as a 4x4 crossbar switch controlled by software for increased routing flexiability (Figure 1). The four data inputs to the MUX (called M0, M1, M2, and M3) come from I/O signals in the GRP and/or adjacent I/O cells. Each MUX data input can access one quarter of the total I/Os. For example, in an 80-I/O ispGDXVA, each data input can connect to one of 20 I/O pins. MUX0 and MUX1 can be driven by designated I/O pins called MUXsel1 and MUXsel2. Each MUXsel input covers 25% of the total I/O pins (e.g. 20 out of 80). MUX0 and MUX1 can be driven from either MUXsel1 or MUXsel2.

Figure 1. ispGDXVA I/O Cell and GRP Detail (80 I/O Device)



I/O MUX Operation

MUX1	MUX0	Data Input Selected
0	0	M0
0	1	M1
1	1	M2
1	0	M3

Flexible mapping of $MUXsel_X$ to MUX_X allows the user to change the MUX select assignment after the ispGDXVA device has been soldered to the board. Figure 1 shows that the I/O cell can accept (by programming the appropriate fuses) inputs from the MUX outputs of four adjacent I/O cells, two above and two below. This enables cascading of the MUXes to enable wider (up to 16:1) MUX implementations.

The I/O cell also includes a programmable flow-through latch or register that can be placed in the input or output path and bypassed for combinatorial outputs. As shown in Figure 1, when the input control MUX of the register/latch selects the "A" path, the register/latch gets its inputs from the 4:1 MUX and drives the I/O output. When selecting the "B" path, the register/latch is directly driven by the I/O input while its output feeds the GRP. The programmable polarity Clock to the latch or register can be connected to any I/O in the I/O-CLK/CLKEN set (one-quarter of total I/Os) or to one of the dedicated clock input pins (Y_X). The programmable polarity Clock Enable input to the register can be programmed to connect to any of the I/O-CLK/CLKEN input pin set or to the global clock enable inputs ($CLKEN_X$). Use of the dedicated clock inputs gives minimum clock-to-output delays and minimizes delay variation with fanout. Combinatorial output mode may be implemented by a dedicated architecture bit and bypass MUX. I/O cell output polarity can be programmed as active high or active low.

MUX Expander Using Adjacent I/O Cells

The ispGDXVA allows adjacent I/O cell MUXes to be cascaded to form wider input MUXes (up to 16 x 1) without incurring an additional full Tpd penalty. However, there are certain dependencies on the locality of the adjacent MUXes when used along with direct MUX inputs.

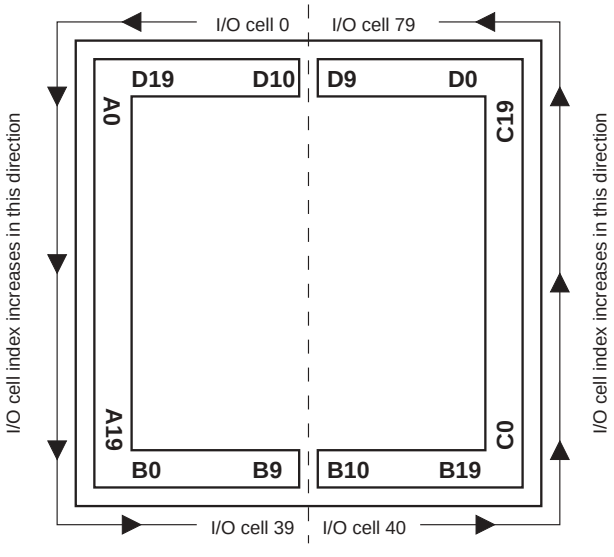
Adjacent I/O Cells

Expansion inputs MUXOUT[n-2], MUXOUT[n-1], MUXOUT[n+1], and MUXOUT[n+2] are fuse-selectable for each I/O cell MUX. These expansion inputs share the same path as the standard A, B, C and D MUX inputs, and allow adjacent I/O cell outputs to be directly connected without passing through the global routing pool. The relationship between the [N+i] adjacent cells and A, B, C and D inputs will vary depending on where the I/O cell is located on the physical die. The I/O cells can be grouped into "normal" and "reflected" I/O cells or I/O "hemispheres." These are defined as:

Device	Normal I/O Cells	Reflected I/O Cells
ispGDX80VA	B9-B0, A19-A0, D19-D10	B10-B19, C0-C19, D0-D9
ispGDX160VA	B19-B0, A39-A0, D39-D20	B20-B39, C0-C39, D0-D19
ispGDX240VA	B29-B0, A59-A0, D59-D30	B30-B59, C0-C59, D0-D29

Table 2 shows the relationship between adjacent I/O cells as well as their relationship to direct MUX inputs. Note that the MUX expansion is circular and that I/O cell B10, for example, draws on I/Os B9 and B8, as well as B11 and B12, even though they are in different hemispheres of the physical die. Table 2 shows some typical cases and all boundary cases. All other cells can be extrapolated from the pattern shown in the table.

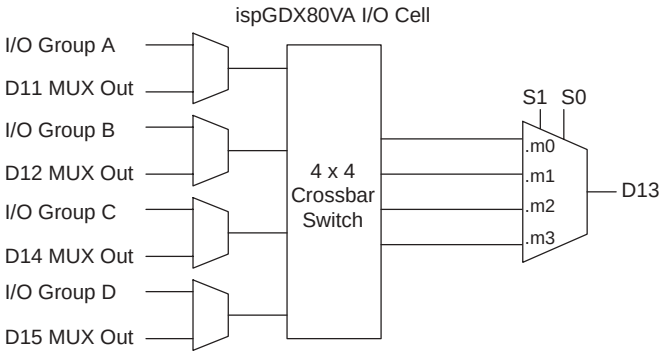
Figure 2. I/O Hemisphere Configuration of ispGDX80VA



Direct and Expander Input Routing

Table 2 also illustrates the routing of MUX direct inputs that are accessible when using adjacent I/O cells as inputs. Take I/O cell D13 as an example, which is also shown in Figure 3.

Figure 3. Adjacent I/O Cells vs. Direct Input Path for ispGDX80VA, I/O D13



It can be seen from Figure 3 that if the D11 adjacent I/O cell is used, the I/O group "A" input is no longer available as a direct MUX input.

The ispGDXVA can implement MUXes up to 16 bits wide in a single level of logic, but care must be taken when combining adjacent I/O cell outputs with direct MUX inputs. Any particular combination of adjacent I/O cells as MUX inputs will dictate what I/O groups (A, B, C or D) can be routed to the remaining inputs. By properly choosing the adjacent I/O cells, all of the MUX inputs can be utilized.

Table 2. Adjacent I/O Cells (Mapping of ispGDX80VA)

		Data A/ MUXOUT	Data B/ MUXOUT	Data C/ MUXOUT	Data D/ MUXOUT
Reflected I/O Cells	B10	B12	B11	B9	B8
	B11	B13	B12	B10	B9
	B12	B14	B13	B11	B10
	B13	B15	B14	B12	B11
	D6	D8	D7	D5	D4
	D7	D9	D8	D6	D5
	D8	D10	D9	D7	D6
	D9	D11	D10	D8	D7
Normal I/O Cells	D10	D8	D9	D11	D12
	D11	D9	D10	D12	D13
	D12	D10	D11	D13	D14
	D13	D11	D12	D14	D15
	B6	B4	B5	B7	B8
	B7	B5	B6	B8	B9
	B8	B6	B7	B9	B10
	B9	B7	B8	B10	B11

Special Features

Slew Rate Control

All output buffers contain a programmable slew rate control that provides software-selectable slew rate options.

Open Drain Control

All output buffers provide a programmable Open-Drain option which allows the user to drive system level reset, interrupt and enable/disable lines directly without the need for an off-chip Open-Drain or Open-Collector buffer. Wire-OR logic functions can be performed at the printed circuit board level.

Pull-up Resistor

All pins have a programmable active pull-up. A typical resistor value for the pull-up ranges from 50kΩ to 80kΩ.

Output Latch (Bus Hold)

All pins have a programmable circuit that weakly holds the previously driven state when all drivers connected to the pin (including the pin's output driver as well as any other devices connected to the pin by external bus) are tristated.

User-Programmable I/Os

The ispGDX80VA features user-programmable I/Os supporting either 3.3V or 2.5V output voltage level options. The ispGDX80VA uses a VCCIO pin to provide the 2.5V reference voltage when used.

PCI Compatible Drive Capability

The ispGDX80VA supports PCI compatible drive capability for all I/Os.

Applications

The ispGDXVA Family architecture has been developed to deliver an in-system programmable signal routing solution with high speed and high flexibility. The devices are targeted for three similar but distinct classes of end-system applications:

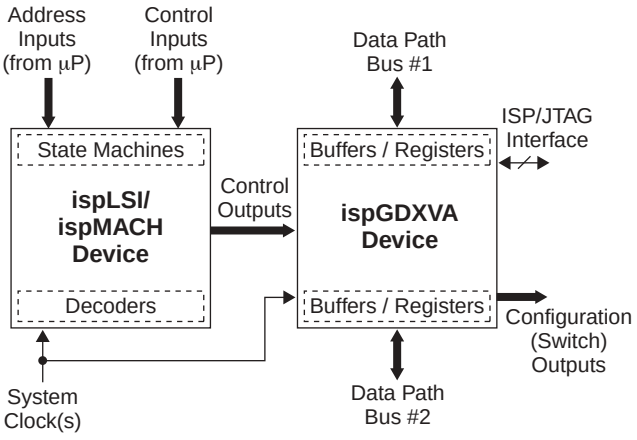
Programmable, Random Signal Interconnect (PRSI)

This class includes PCB-level programmable signal routing and may be used to provide arbitrary signal swapping between chips. It opens up the possibilities of programmable system hardware. It is characterized by the need to provide a large number of 1:1 pin connections which are statically configured, i.e., the pin-to-pin paths do not need to change dynamically in response to control inputs.

Programmable Data Path (PDP)

This application area includes system data path transceiver, MUX and latch functions. With today's 32- and 64-bit microprocessor buses, but standard data path glue components still relegated primarily to eight bits, PCBs are frequently crammed with a dozen or more data path glue chips that use valuable real estate. Many of these applications consist of "on-board" bus and memory interfaces that do not require the very high drive of standard glue functions but can benefit from higher integration. Therefore, there is a need for a flexible means to integrate these on-board data path functions in an analogous way to programmable logic's solution to control logic integration. Lattice's CPLDs make an ideal control logic complement to the ispGDXVA in-system programmable data path devices as shown below.

Figure 4. ispGDXVA Complements Lattice CPLDs



Programmable Switch Replacement (PSR)

Includes solid-state replacement and integration of mechanical DIP Switch and jumper functions. Through in-system programming, pins of the ispGDXVA devices can be driven to HIGH or LOW logic levels to emulate the traditional device outputs. PSR functions do not require any input pin connections.

These applications actually require somewhat different silicon features. PRSI functions require that the device support arbitrary signal routing on-chip between any two pins with no routing restrictions. The routing connections are static (determined at programming time) and each input-to-output path operates independently. As a result, there is little need for dynamic signal controls (OE, clocks, etc.). Because the ispGDXVA device will interface with control logic outputs from other components (such as ispLSI or ispMACH™) on the board (which frequently change late in the design process as control logic is finalized), there must be no restrictions on pin-to-pin signal routing for this type of application.

PDP functions, on the other hand, require the ability to dynamically switch signal routing (MUXing) as well as latch and tri-state output signals. As a result, the programmable interconnect is used to define *possible* signal routes that are then selected dynamically by control signals from an external MPU or control logic. These functions are usually formulated early in the conceptual design of a product. The data path requirements are driven by the microprocessor, bus and memory architecture defined for the system. This part of the design is the earliest portion of the system design frozen, and will not usually change late in the design because the result would be total system and PCB redesign. As a result, the ability to accommodate *arbitrary* any pin-to-any pin rerouting is not a strong requirement as long as the designer has the ability to define his functions with a reasonable degree of freedom initially.

As a result, the ispGDXVA architecture has been defined to support PSR and PRSI applications (including bidirectional paths) with no restrictions, while PDP applications (using dynamic MUXing) are supported with a minimal number of restrictions as described below. In this way, speed and cost can be optimized and the devices can still support the system designer's needs.

The following diagrams illustrate several ispGDXVA applications.

Applications (Continued)

Figure 5. Address Demultiplex/Data Buffering

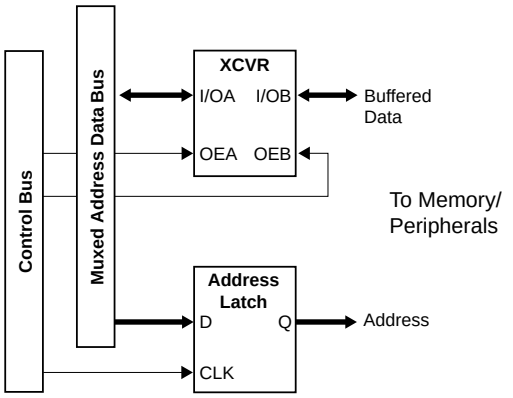


Figure 6. Data Bus Byte Swapper

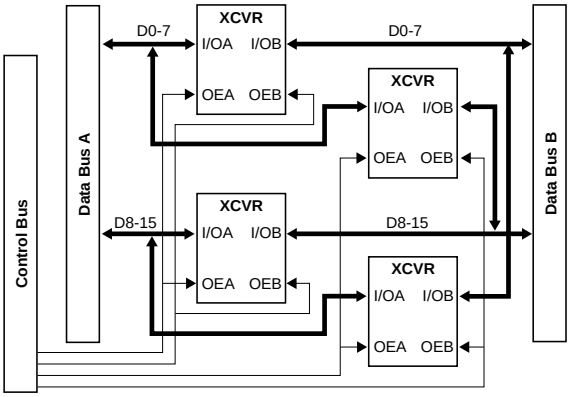
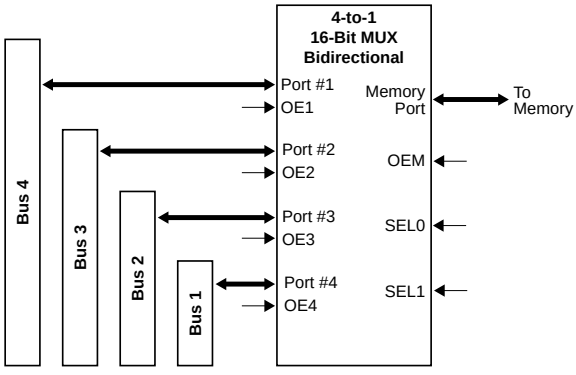


Figure 7. Four-Port Memory Interface



Note: All OE and SEL lines driven by external arbiter logic (not shown).

Designing with the ispGDXVA

As mentioned earlier, this architecture satisfies the PRSI class of applications without restrictions: any I/O pin as a single input or bidirectional can drive any other I/O pin as output.

For the case of PDP applications, the designer does have to take into consideration the limitations on pins that can be used as control (MUX0, MUX1, OE, CLK) or data (MUXA-D) inputs. The restrictions on control inputs are not likely to cause any major design issues because the input possibilities span 25% of the total pins.

The MUXA-D input partitioning requires that designers consciously assign pinouts so that MUX inputs are in the appropriate, disjoint groups. For example, since the MUXA group includes I/O A0-A19 (80 I/O device), it is not possible to use I/O A0 and I/O A9 in the same MUX function. As previously discussed, data path functions will be assigned early in the design process and these restrictions are reasonable in order to optimize speed and cost.

User Electronic Signature

The ispGDXVA Family includes dedicated User Electronic Signature (UES) E^2CMOS storage to allow users to code design-specific information into the devices to identify particular manufacturing dates, code revisions, or the like. The UES information is accessible through the boundary scan programming port via a specific command. This information can be read even when the security cell is programmed.

Security

The ispGDXVA Family includes a security feature that prevents reading the device program once set. Even when set, it does not inhibit reading the UES or device ID code. It can be erased only via a device bulk erase.

Absolute Maximum Ratings [1,2]

Supply Voltage V_{cc} ..... -0.5 to +5.4V

Input Voltage Applied ..... -0.5 to +5.6V

Off-State Output Voltage Applied ..... -0.5 to +5.6V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied ... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).
2. Compliance with the Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM is a requirement.

DC Recommended Operating Conditions

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial	T_A = 0°C to +70°C	3.00	3.60	V
		Industrial	T_A = -40°C to +85°C	3.00	3.60	V
V_{CCIO}	I/O Reference Voltage			2.3	3.60	V

Table 2-0005/gdxva

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	PACKAGE TYPE	TYPICAL	UNITS	TEST CONDITIONS
C_1	I/O Capacitance	TQFP	7	pf	V_{CC} = 3.3V, $V_{I/O}$ = 2.0V
C_2	Dedicated Clock Capacitance	TQFP	8	pf	V_{CC} = 3.3V, V_Y = 2.0V

Table 2-0006/gdxva

Erase/Reprogram Specifications

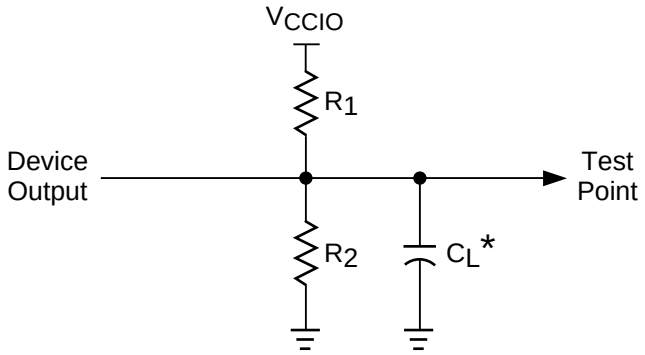
PARAMETER	MINIMUM	MAXIMUM	UNITS
Erase/Reprogram Cycles	10,000	—	Cycles

Switching Test Conditions

Input Pulse Levels	GND to $V_{CCIO(MIN)}$
Input Rise and Fall Time	≤ 1.5ns 10% to 90%
Input Timing Reference Levels	$V_{CCIO(MIN)}/2$
Output Timing Reference Levels	$V_{CCIO(MIN)}/2$
Output Load	See Figure 8

3-state levels are measured 0.5V from steady-state active level.

Figure 8. Test Load



*C_L includes Test Fixture and Probe Capacitance.

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Output Load Conditions (See Figure 8)

		3.3V		2.5V		
TEST CONDITION		**R1**	**R2**	**R1**	**R2**	**CL**
A		153Ω	134Ω	156Ω	144Ω	35pF
B	Active High	∞	134Ω	∞	144Ω	35pF
	Active Low	153Ω	∞	156Ω	∞	35pF
C	Active High to Z at V_{OH}-0.5V	∞	134Ω	∞	144Ω	5pF
	Active Low to Z at V_{OL}+0.5V	153Ω	∞	156Ω	∞	5pF
D	Slow Slew	∞	∞	∞	∞	35pF

Table 2-0004A/gdxva

DC Electrical Characteristics for 3.3V Range

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[1]	MAX.	UNITS
V_{CCIO}	I/O Reference Voltage	–		3.0	–	3.6	V
V_{IL}	Input Low Voltage	$V_{OH} \le V_{OUT}$ or $V_{OUT} \le V_{OL\ (MAX)}$		-0.3	–	0.8	V
V_{IH}	Input High Voltage	$V_{OH} \le V_{OUT}$ or $V_{OUT} \le V_{OL(MAX)}$		2.0	–	5.25	V
V_{OL}	Output Low Voltage	$V_{CC} = V_{CC\ (MIN)}$	I_{OL} = +100µA	–	–	0.2	V
			I_{OL} = +24mA	–	–	0.55	V
V_{OH}	Output High Voltage	$V_{CC} = V_{CC\ (MIN)}$	I_{OH} = -100µA	2.8	–	–	V
			I_{OH} = -12mA	2.4	–	–	V

1. Typical values are at V_{CC} = 3.3V and T_A = 25°C.

Table 2-0007/gdxva

DC Electrical Characteristics for 2.5V Range

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{CCIO}	I/O Reference Voltage	–	2.3	–	2.7	V
V_{IL}	Input Low Voltage	$V_{OH(MIN)} \le V_{OUT}$ or $V_{OUT} \le V_{OL(MAX)}$	-0.3	–	0.7	V
V_{IH}	Input High Voltage	$V_{OH(MIN)} \le V_{OUT}$ or $V_{OUT} \le V_{OL(MAX)}$	1.7	–	5.25	V
V_{OL}	Output Low Voltage	$V_{CCIO=MIN}$, I_{OL} = 100µA	–	–	0.2	V
		$V_{CCIO=MIN}$, I_{OL} = 8mA	–	–	0.6	V
V_{OH}	Output High Voltage	$V_{CCIO=MIN}$, I_{OH} = -100µA	2.1	–	–	V
		$V_{CCIO=MIN}$, I_{OH} = -8mA	1.8	–	–	V

2.5V/gdxva

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[2]	MAX.	UNITS
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL\ (MAX)}$	–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	$(V_{CCIO}-0.2) \le V_{IN} \le V_{CCIO}$	–	–	10	µA
		$V_{CCIO} \le V_{IN} \le 5.25V$	–	–	50	µA
I_{PU}	I/O Active Pullup Current	$0V \le V_{IN} \le V_{IL\ (MAX)}$	–	–	-200	µA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL\ (MAX)}$	40	–	–	µA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = V_{IH\ (MIN)}$	-40	–	–	µA
I_{BHLO}	Bus Hold Low Overdrive Current	$0V \le V_{IN} \le V_{CCIO}$	–	–	550	µA
I_{BHHO}	Bus Hold High Overdrive Current	$0V \le V_{IN} \le V_{CCIO}$	–	–	-550	µA
I_{BHT}	Bus Hold Trip Points		V_{IL}	–	V_{IH}	V
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 3.3V, V_{OUT} = 0.5V, T_A = 25°C	–	–	-250	mA
I_{CCQ}[4]	Quiescent Power Supply Current	V_{IL} = 0.5V, $V_{IH} = V_{CC}$	–	12	–	mA
I_{CC}	Dynamic Power Supply Current per Input Switching	One input toggling at 50% duty cycle, outputs open.	–	See Note 3	–	mA/ MHz
I_{CONT}[5]	Maximum Continuous I/O Pin Sink Current Through Any GND Pin	–	–	–	160	mA

DC Char_gdx80va

1. One output at a time for a maximum of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Characterized, but not 100% tested.
2. Typical values are at V_{CC} = 3.3V and T_A = 25°C.
3. I_{CC} / MHz = (0.002 x I/O cell fanout) + 0.022.
   e.g. An input driving four I/O cells at 40MHz results in a dynamic I_{CC} of approximately ((0.002 x 4) + 0.022) x 40 = 1.20mA.
4. For a typical application with 50% of I/O pins used as inputs, 50% used as outputs or bi-directionals.
5. This parameter limits the total current sinking of I/O pins surrounding the nearest GND pin.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST[1] COND.	#	DESCRIPTION	-3[3]		-3		-5		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tpd[2]	A	1	Data Prop. Delay: Any I/O Pin to Any I/O Pin (4:1 MUX)	–	3.0	–	3.5	–	5.0	ns
tsel[2]	A	2	Data Prop. Delay: MUXsel Inputs to Any Output (4:1 MUX)	–	3.2	–	3.5	–	5.0	ns
fmax (Tog.)	–	3	Clk. Frequency, Max. Toggle	250	–	250	–	143	–	MHz
fmax (Ext.)	–	4	Clk. Frequency with External Feedback ($\frac{1}{tsu3+tgco1}$)	208.3	–	166.7	–	111	–	MHz
tsu1	–	5	Input Latch or Reg. Setup Time Before Y_x	2.2	–	3.0	–	4.0	–	ns
tsu2	–	6	Input Latch or Reg. Setup Time Before I/O Clk.	1.8	–	2.5	–	3.0	–	ns
tsu3	–	7	Output Latch or Reg. Setup Time Before Y_x	1.8	–	2.5	–	4.0	–	ns
tsu4	–	8	Output Latch or Reg. Setup Time Before I/O Clk.	1.5	–	2.0	–	3.0	–	ns
tsuce1	–	9	Global Clk. Enable Setup Time Before Y_x	1.8	–	2.5	–	2.5	–	ns
tsuce2	–	10	Global Clk. Enable Setup Time Before I/O Clk.	1.5	–	1.5	–	1.5	–	ns
tsuce3	–	11	I/O Clk. Enable Setup Time Before Y_x	2.5	–	3.0	–	4.5	–	ns
th1	–	12	Input Latch or Reg. Hold Time (Y_x)	0.0	–	0.0	–	0.0	–	ns
th2	–	13	Input Latch or Reg. Hold Time (I/O Clk.)	0.5	–	0.5	–	1.5	–	ns
th3	–	14	Output Latch or Reg. Hold Time (Y_x)	0.0	–	0.0	–	0.0	–	ns
th4	–	15	Output Latch or Reg. Hold Time (I/O Clk.)	0.5	–	1.0	–	1.5	–	ns
thce1	–	16	Global Clk. Enable Hold Time (Y_x)	0.0	–	0.0	–	0.0	–	ns
thce2	–	17	Global Clk. Enable Hold Time (I/O Clk.)	1.0	–	1.0	–	1.5	–	ns
thce3	–	18	I/O Clk. Enable Hold Time (Y_x)	0.0	–	0.0	–	0.0	–	ns
tgco1[2]	A	19	Output Latch or Reg. Clk. (from Y_x) to Output Delay	–	3.0	–	3.5	–	5.0	ns
tgco2[2]	A	20	Input Latch or Register Clk. (from Y_x) to Output Delay	–	5.5	–	6.0	–	8.5	ns
tco1[2]	A	21	Output Latch or Reg. Clk. (from I/O pin) to Output Delay	–	3.5	–	4.0	–	6.0	ns
tco2[2]	A	22	Input Latch or Reg. Clk. (from I/O pin) to Output Delay	–	6.0	–	7.0	–	9.5	ns
ten[2]	B	23	Input to Output Enable	–	4.0	–	5.0	–	6.0	ns
tdis[2]	C	24	Input to Output Disable	–	4.0	–	5.0	–	6.0	ns
ttoeen[2]	B	25	Test OE Output Enable	–	5.5	–	6.0	–	6.0	ns
ttoedis[2]	C	26	Test OE Output Disable	–	5.5	–	6.0	–	6.0	ns
twh	–	27	Clock Pulse Duration, High	2.0	–	2.0	–	3.5	–	ns
twl	–	28	Clock Pulse Duration, Low	2.0	–	2.0	–	3.5	–	ns
trst	–	29	Register Reset Delay from RESET Low	–	7.0	–	8.0	–	14.0	ns
trw	–	30	Reset Pulse Width	4.5	–	5.0	–	10.0	–	ns
tsl	D	31	Output Delay Adder for Output Timings Using Slow Slew Rate	–	3.0	–	3.5	–	5.0	ns
tsk	A	32	Output Skew (tgco1 Across Chip)	–	0.5	–	0.5	–	0.5	ns

1. All timings measured with one output switching, fast output slew rate setting, except tsl.
2. The delay parameters are measured with Vcc as I/O voltage reference. An additional 0.5ns delay is incurred when Vccio is used as I/O voltage reference.
3. The new "-3" speed grade (tpd = 3.0ns) will be effective starting with date code A113xxxx. Devices with topside date codes prior to A113xxxx adhere to the shaded "-3" speed grade (tpd = 3.5ns).

External Timing Parameters

Over Recommended Operating Conditions

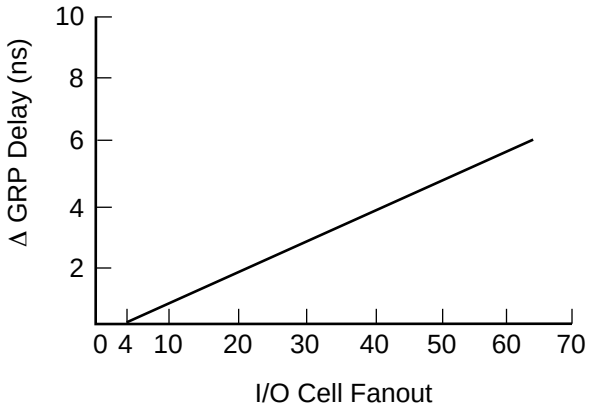
PARAMETER	TEST[1] COND.	#	DESCRIPTION	-7		-9		UNITS
				MIN.	MAX.	MIN.	MAX.	
tpd[2]	A	1	Data Prop. Delay: Any I/O pin to Any I/O Pin (4:1 MUX)	–	7.0	–	9.0	ns
tsel[2]	A	2	Data Prop. Delay: MUXsel Inputs to Any Output (4:1 MUX)	–	7.0	–	9.0	ns
fmax (Tog.)	–	3	Clk. Frequency, Max. Toggle	100	–	83	–	MHz
fmax (Ext.)	–	4	Clk. Frequency with External Feedback($\frac{1}{tsu3+tgco1}$)	80	–	62.5	–	MHz
tsu1	–	5	Input Latch or Reg. Setup Time Before Y_x	5.5	–	7.0	–	ns
tsu2	–	6	Input Latch or Reg. Setup Time Before I/O Clock	4.5	–	6.0	–	ns
tsu3	–	7	Output Latch or Reg. Setup Time Before Y_x	5.5	–	7.0	–	ns
tsu4	–	8	Output Latch or Reg. Setup Time Before I/O Clk.	4.5	–	6.0	–	ns
tsuce1	–	9	Global Clk. Enable Setup Time Before Y_x	3.5	–	4.0	–	ns
tsuce2	–	10	Global Clk. Enable Setup Time Before I/O Clk.	2.5	–	3.0	–	ns
tsuce3	–	11	I/O Clk. Enable Setup Time Before Y_x	6.5	–	8.5	–	ns
th1	–	12	Input Latch or Reg. Hold Time (Y_x)	0.0	–	0.0	–	ns
th2	–	13	Input Latch or Reg. Hold Time (I/O Clk.)	2.5	–	3.0	–	ns
th3	–	14	Output Latch or Reg. Hold Time (Y_x)	0.0	–	0.0	–	ns
th4	–	15	Output Latch or Reg. Hold Time (I/O Clk.)	2.5	–	3.0	–	ns
thce1	–	16	Global Clk. Enable Hold Time (Y_x)	0.0	–	0.0	–	ns
thce2	–	17	Global Clk. Enable Hold Time (I/O Clk.)	2.5	–	3.0	–	ns
thce3	–	18	I/O Clk. Enable Hold Time (Y_x)	0.0	–	0.0	–	ns
tgco1[2]	A	19	Output Latch or Reg. Clk. (from Y_x) to Output Delay	–	7.0	–	9.0	ns
tgco2[2]	A	20	Input Latch or Reg. Clk. (from Y_x) to Output Delay	–	11.0	–	13.5	ns
tco1[2]	A	21	Output Latch or Reg. Clk. (from I/O pin) to Output Delay	–	9.0	–	11.5	ns
tco2[2]	A	22	Input Latch or Reg. Clock (from I/O pin) to Output Delay	–	13.0	–	15.7	ns
ten[2]	B	23	Input to Output Enable	–	8.5	–	10.5	ns
tdis[2]	C	24	Input to Output Disable	–	8.5	–	10.5	ns
ttoeen[2]	B	25	Test OE Output Enable	–	8.5	–	10.5	ns
ttoedis[2]	C	26	Test OE Output Disable	–	8.5	–	10.5	ns
twh	–	27	Clk. Pulse Duration, High	5.0	–	6.0	–	ns
twl	–	28	Clk. Pulse Duration, Low	5.0	–	6.0	–	ns
trst	–	29	Reg. Reset Delay from RESET Low	–	18.0	–	22.0	ns
trw	–	30	Reset Pulse Width	14.0	–	18.0	–	ns
tsl	D	31	Output Delay Adder for Output Timings Using Slow Slew Rate	–	7.0	–	9.0	ns
tsk	A	32	Output Skew (tgco1 Across Chip)	–	0.5	–	1.0	ns

1. All timings measured with one output switching, fast output slew rate setting, except tsl.
2. The delay parameters are measured with Vcc as I/O voltage reference. An additional 0.5ns delay is incurred when Vccio is used as I/O voltage reference.

External Timing Parameters (Continued)

ispGDX80VA timings are specified with a GRP load (fanout) of four I/O cells. The figure below shows the Δ GRP Delay with increased GRP loads. These deltas apply to any signal path traversing the GRP (MUXA-D, OE, CLK/CLKEN, MUXsel0-1). Global Clock signals which do not use the GRP have no fanout delay adder.

ispGDX80VA Maximum Δ GRP Delay vs. I/O Cell Fanout



Internal Timing Parameters

Over Recommended Operating Conditions

PARAMETER	#	DESCRIPTION[1]	-3[2]		-3		-5		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Inputs									
t_{io}	32	Input Buffer Delay	—	0.3	—	0.4	—	0.9	ns
GRP									
t_{grp}	33	GRP Delay	—	1.1	—	1.1	—	1.1	ns
MUX									
t_{muxd}	34	I/O Cell MUX A/B/C/D Data Delay	—	0.8	—	1.0	—	1.5	ns
t_{muxexp}	35	I/O Cell MUX A/B/C/D Expander Delay	—	1.3	—	1.5	—	2.0	ns
t_{muxs}	36	I/O Cell Data Select	—	1.0	—	1.0	—	1.5	ns
t_{muxsio}	37	I/O Cell Data Select (I/O Clock)	—	1.5	—	1.5	—	3.0	ns
t_{muxsg}	38	I/O Cell Data Select (Yx Clock)	—	1.5	—	1.5	—	2.0	ns
$t_{muxselexp}$	39	I/O Cell MUX Data Select Expander Delay	—	1.5	—	1.5	—	2.0	ns
Register									
t_{iolat}	40	I/O Latch Delay	—	1.0	—	1.0	—	1.0	ns
t_{iosu}	41	I/O Register Setup Time Before Clock	—	0.4	—	0.8	—	2.0	ns
t_{ioh}	42	I/O Register Hold Time After Clock	—	1.4	—	1.7	—	1.5	ns
t_{ioco}	43	I/O Register Clock to Output Delay	—	0.9	—	1.2	—	0.5	ns
t_{ior}	44	I/O Reset to Output Delay	—	1.0	—	1.0	—	1.5	ns
t_{cesu}	45	I/O Clock Enable Setup Time Before Clock	—	0.6	—	1.3	—	2.0	ns
t_{ceh}	46	I/O Clock Enable Hold Time After Clock	—	1.2	—	1.2	—	0.5	ns
Data Path									
t_{fdbk}	47	I/O Register Feedback Delay	—	0.4	—	0.4	—	0.9	ns
t_{iobp}	48	I/O Register Bypass Delay	—	0.0	—	0.0	—	0.0	ns
t_{ioob}	49	I/O Register Output Buffer Delay	—	0.0	—	0.0	—	0.0	ns
t_{muxcg}	50	I/O Register A/B/C/D Data Input MUX Delay (Yx Clock)	—	1.3	—	1.5	—	2.0	ns
t_{muxcio}	51	I/O Register A/B/C/D Data Input MUX Delay (I/O Clock)	—	1.3	—	1.5	—	3.0	ns
t_{iodg}	52	I/O Register I/O MUX Delay (Yx Clock)	—	3.1	—	3.5	—	4.0	ns
t_{iodio}	53	I/O Register I/O MUX Delay (I/O Clock)	—	3.1	—	3.5	—	5.0	ns
Outputs									
t_{ob}	54	Output Buffer Delay	—	0.8	—	1.0	—	1.5	ns
t_{obs}	55	Output Buffer Delay (Slow Slew Option)	—	3.8	—	4.5	—	6.5	ns
t_{oeen}	56	I/O Cell OE to Output Enable	—	2.6	—	3.5	—	4.0	ns
t_{oedis}	57	I/O Cell OE to Output Disable	—	2.6	—	3.5	—	4.0	ns
t_{goe}	58	GRP Output Enable and Disable Delay	—	0.0	—	0.0	—	0.0	ns
t_{toe}	59	Test OE Enable and Disable Delay	—	2.5	—	2.5	—	2.0	ns
Clocks									
t_{ioclk}	60	I/O Clock Delay	—	0.3	—	0.3	—	2.0	ns
t_{gclk}	61	Global Clock Delay	—	1.3	—	1.3	—	2.0	ns
$t_{gclkeng}$	62	Global Clock Enable (Yx Clock)	—	2.5	—	2.5	—	2.5	ns
$t_{gclkenio}$	63	Global Clock Enable (I/O Clock)	—	2.0	—	2.0	—	3.5	ns
$t_{ioclkeng}$	64	I/O Clock Enable (Yx Clock)	—	1.5	—	1.5	—	2.5	ns
Global Reset									
t_{gr}	65	Global Reset to I/O Register Latch	—	5.2	—	6.0	—	11.0	ns

1. Internal Timing Parameters are not tested and are for reference only.

Timing Rev. 2.9

2. The new “-3” speed grade (tpd = 3.0ns) will be effective starting with date code A113xxxx. Devices with topside date codes prior to A113xxxx adhere to the shaded “-3” speed grade (tpd = 3.5ns).

Internal Timing Parameters[1]

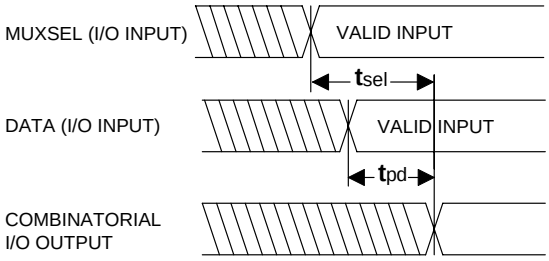
Over Recommended Operating Conditions

PARAMETER	#	DESCRIPTION[1]	-7		-9		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t_{io}	32	Input Buffer Delay	—	1.4	—	1.9	ns
GRP							
t_{grp}	33	GRP Delay	—	1.1	—	1.1	ns
MUX							
t_{muxd}	34	I/O Cell MUX A/B/C/D Data Delay	—	2.0	—	2.5	ns
t_{muxexp}	35	I/O Cell MUX A/B/C/D Expander Delay	—	2.5	—	3.0	ns
t_{muxs}	36	I/O Cell Data Select	—	2.0	—	2.5	ns
t_{muxsio}	37	I/O Cell Data Select (I/O Clock)	—	4.5	—	6.0	ns
t_{muxsg}	38	I/O Cell Data Select (Yx Clock)	—	2.5	—	3.0	ns
$t_{muxselexp}$	39	I/O Cell MUX Data Select Expander Delay	—	2.5	—	3.0	ns
Register							
t_{iolat}	40	I/O Latch Delay	—	1.0	—	1.0	ns
t_{iosu}	41	I/O Register Setup Time Before Clock	—	3.2	—	4.4	ns
t_{ioh}	42	I/O Register Hold Time After Clock	—	2.3	—	2.6	ns
t_{ioco}	43	I/O Register Clock to Output Delay	—	0.5	—	0.5	ns
t_{ior}	44	I/O Reset to Output Delay	—	1.5	—	1.5	ns
t_{cesu}	45	I/O Clock Enable Setup Time Before Clock	—	2.5	—	2.0	ns
t_{ceh}	46	I/O Clock Enable Hold Time After Clock	—	1.0	—	2.0	ns
Data Path							
t_{fdbk}	47	I/O Register Feedback Delay	—	1.2	—	1.3	ns
t_{iobp}	48	I/O Register Bypass Delay	—	0.3	—	0.6	ns
t_{ioob}	49	I/O Register Output Buffer Delay	—	0.6	—	0.7	ns
t_{muxcg}	50	I/O Register A/B/C/D Data Input MUX Delay (Yx Clock)	—	2.5	—	3.0	ns
t_{muxcio}	51	I/O Register A/B/C/D Data Input MUX Delay (I/O Clock)	—	4.5	—	6.0	ns
t_{iodg}	52	I/O Register I/O MUX Delay (Yx Clock)	—	5.0	—	6.0	ns
t_{iodio}	53	I/O Register I/O MUX Delay (I/O Clock)	—	7.0	—	9.0	ns
Outputs							
t_{ob}	54	Output Buffer Delay	—	2.2	—	2.9	ns
t_{obs}	55	Output Buffer Delay (Slow Slew Option)	—	9.2	—	11.9	ns
t_{oeen}	56	I/O Cell OE to Output Enable	—	6.0	—	7.5	ns
t_{oedis}	57	I/O Cell OE to Output Disable	—	6.0	—	7.5	ns
t_{goe}	58	GRP Output Enable and Disable Delay	—	0.0	—	0.0	ns
t_{toe}	59	Test OE Enable and Disable Delay	—	2.5	—	3.0	ns
Clocks							
t_{ioclk}	60	I/O Clock Delay	—	3.2	—	4.4	ns
t_{gclk}	61	Global Clock Delay	—	2.7	—	3.4	ns
$t_{gclkeng}$	62	Global Clock Enable (Yx Clock)	—	3.7	—	5.4	ns
$t_{gclkenio}$	63	Global Clock Enable (I/O Clock)	—	5.7	—	8.4	ns
$t_{ioclkeng}$	64	I/O Clock Enable (Yx Clock)	—	4.2	—	6.4	ns
Global Reset							
t_{gr}	65	Global Reset to I/O Register Latch	—	13.7	—	16.4	ns

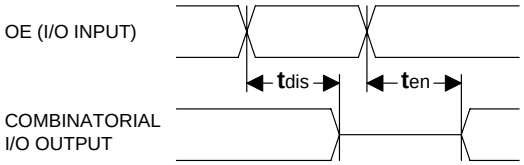
1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to the Timing Model in this data sheet for further details.

Timing Rev. 2.9

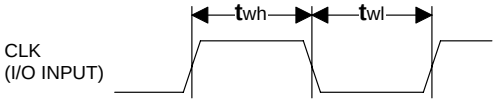
Switching Waveforms



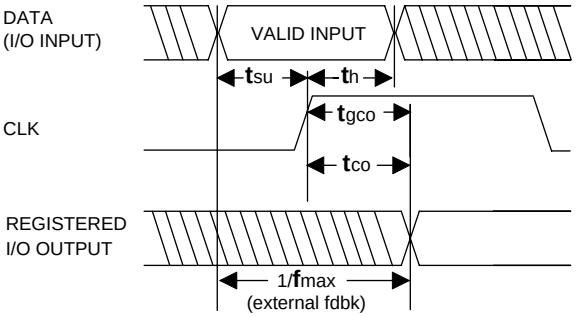
Combinatorial Output

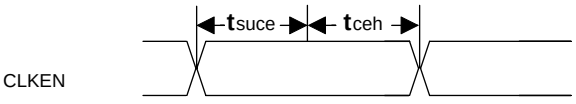


I/O Output Enable/Disable

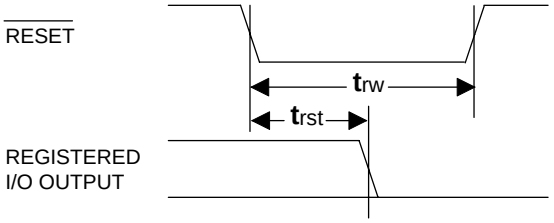


Clock Width



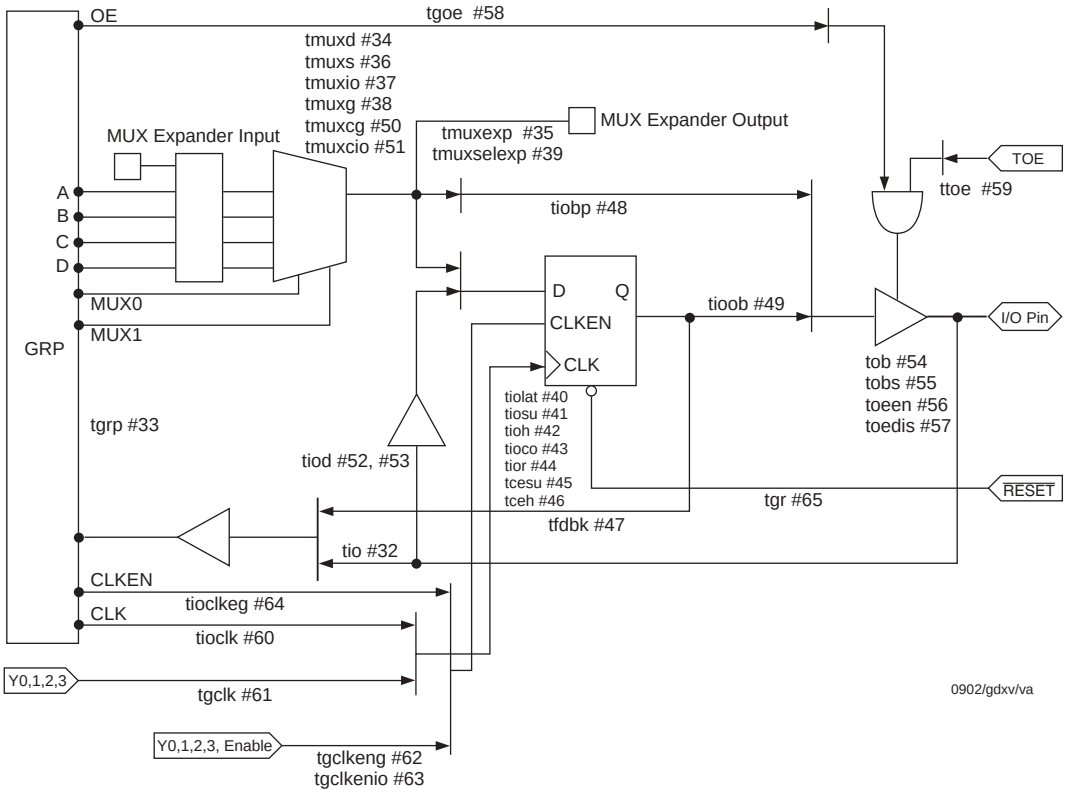


Registered Output



Reset

ispGDXVA Timing Model



ispLEVER Development System

The ispLEVER Development System supports ispGDX design using a VHDL or Verilog language syntax. From creation to in-system programming, the ispLEVER system is an easy-to-use, self-contained design tool.

Features

- VHDL and Verilog Synthesis Support Available
- ispGDX Design Compiler
  - Design Rule Checker
  - I/O Connectivity Checker
  - Automatic Compiler Function
- Industry Standard JEDEC File for Programming
- Min/Max Timing Report
- Interfaces To Popular Timing Simulators
- User Electronic Signature (UES) Support
- Detailed Log and Report Files For Easy Design Debug
- On-line Help
- Windows® XP, Windows 2000, Windows 98 and Windows NT® Compatible
- Solaris® and HP-UX Versions Available

In-System Programmability

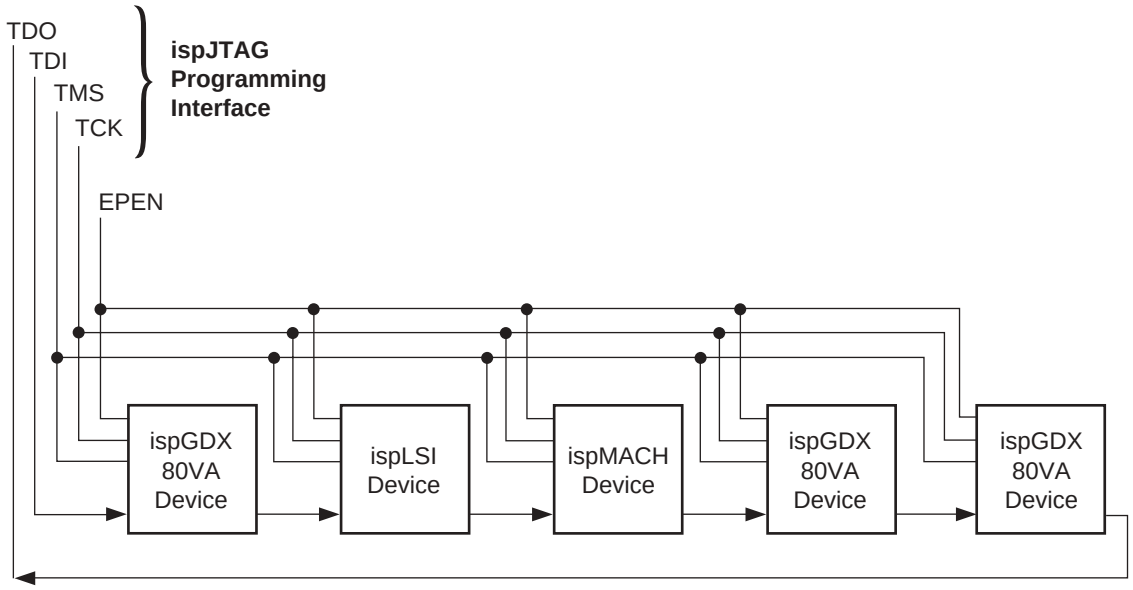
All necessary programming of the ispGDXVA is done via four TTL level logic interface signals. These four signals are fed into the on-chip programming circuitry where a state machine controls the programming.

On-chip programming can be accomplished using an IEEE 1149.1 boundary scan protocol. The IEEE 1149.1-compliant interface signals are Test Data In (TDI), Test Data Out (TDO), Test Clock (TCK) and Test Mode Select (TMS) control. The EPEN pin is also used to enable or disable the JTAG port.

The embedded controller port enable pin (EPEN) is used to enable the JTAG tap controller and in that regard has similar functionality to a TRST pin. When the pin is driven high, the JTAG TAP controller is enabled. This is also true when the pin is left unconnected, in which case the pin is pulled high by the permanent internal pullup. This allows ISP programming and BSCAN testing to take place as specified by the Instruction Table.

When the pin is driven low, the JTAG TAP controller is driven to a reset state asynchronously. It stays there while the pin is held low. After pulling the pin high the JTAG controller becomes active. The intent of this feature is to allow the JTAG interface to be directly controlled by the data bus of an embedded controller (hence the name Embedded Port Enable). The EPEN signal is used as a “device select” to prevent spurious programming and/or testing from occuring due to random bit patterns on the data bus. Figure 9 illustrates the block diagram for the ispJTAG™ interface.

Figure 9. ispJTAG Device Programming Interface



Boundary Scan

The ispGDXVA devices provide IEEE1149.1a test capability and ISP programming through a standard Boundary Scan Test Access Port (TAP) interface.

The boundary scan circuitry on the ispGDXVA Family operates independently of the programmed pattern. This allows customers using boundary scan test to have full test capability with only a single BSDL file.

The ispGDXVA devices are identified by the 32-bit JTAG IDCODE register. The device ID assignments are listed in Table 4.

Figure 10. Boundary Scan Register Circuit for I/O Pins

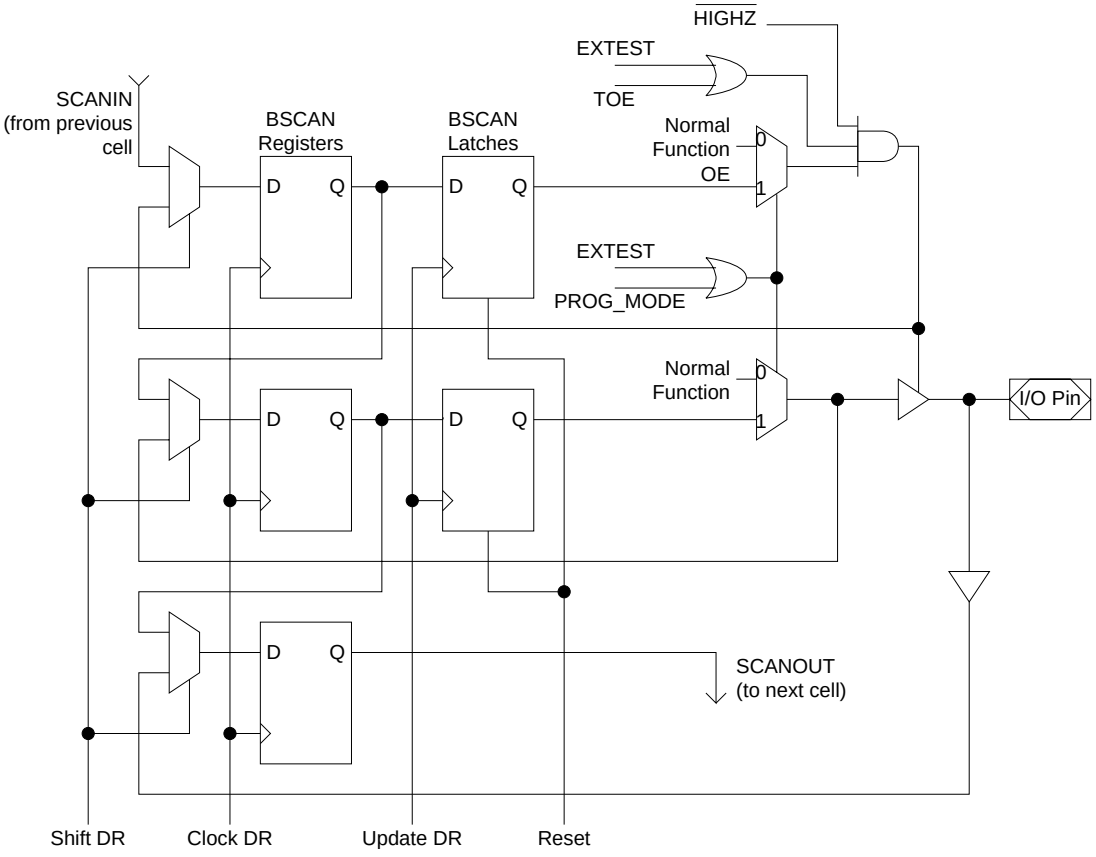


Table 3. I/O Shift Register Order

DEVICE	I/O SHIFT REGISTER ORDER
ispGDX80VA	TDI, TOE, $\overline{\text{RESET}}$, Y1, Y0, I/O B10 .. B19, I/O C0 .. C19, I/O D0 .. D9, I/O B9 .. B0, I/O A19.. A0, I/O D19 .. D10, TDO

I/O Shift Reg Order/ispGDXVA

Table 4. ispGDX80VA Device ID Codes

DEVICE	32-BIT BOUNDARY SCAN ID CODE
ispGDX80VA	0001, 0000, 0011, 0101, 0000, 0000, 0100, 0011

ID Code/GDX80VA

Boundary Scan (Continued)

The ispJTAG programming is accomplished by executing Lattice private instructions under the Boundary Scan State Machine.

Details of the programming sequence are transparent to the user and are handled by Lattice ISP Daisy Chain Downlowad software, ispCODE 'C' routines or any third-party programmers. Contact Lattice Technical Support to obtain more detailed programming information.

Figure 11. Boundary Scan Register Circuit for Input-Only Pins

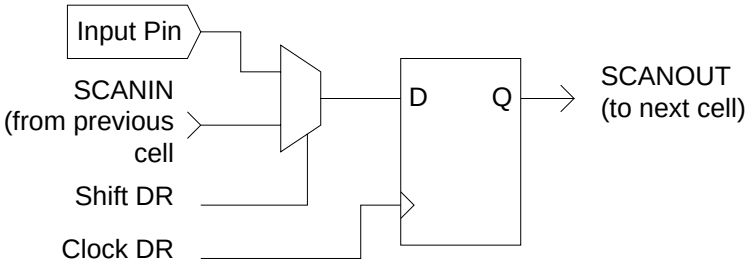
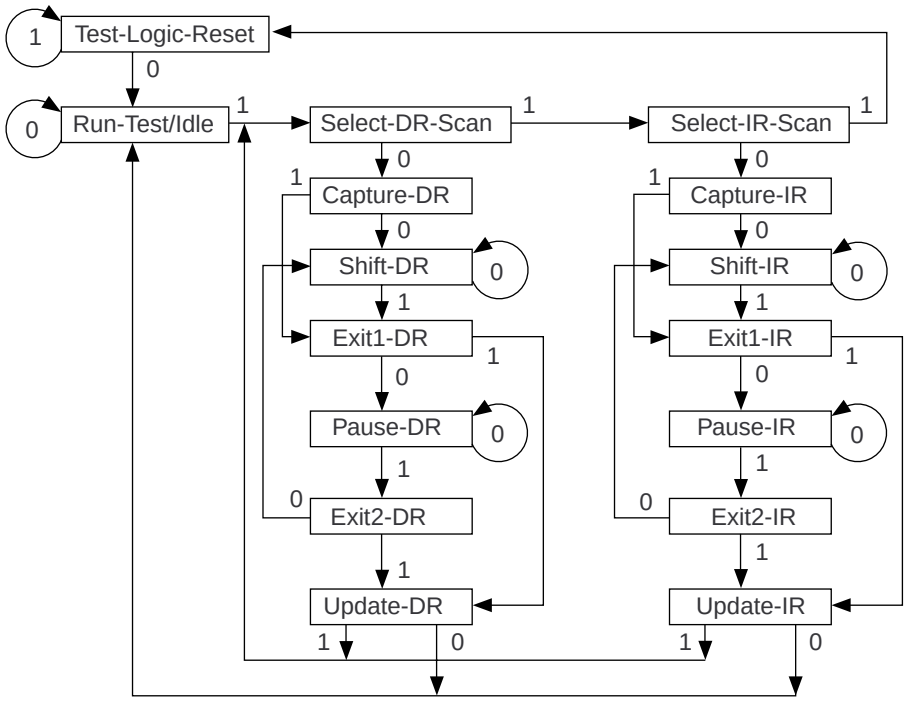
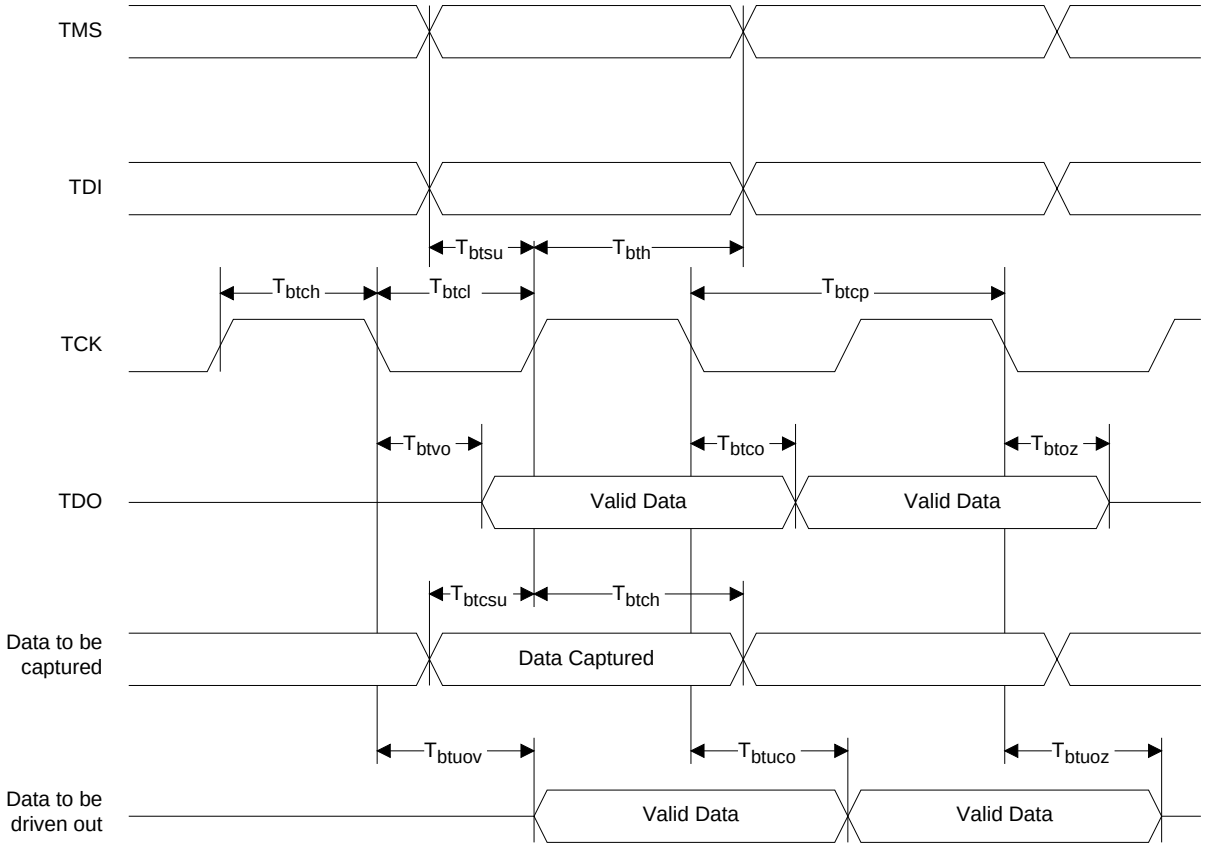


Figure 12. Boundary Scan State Machine



Boundary Scan (Continued)

Figure 13. Boundary Scan Waveforms and Timing Specifications



Symbol	Parameter	Min	Max	Units
t_{btcp}	TCK [BSCAN test] clock pulse width	100	–	ns
t_{btch}	TCK [BSCAN test] pulse width high	50	–	ns
t_{btcl}	TCK [BSCAN test] pulse width low	50	–	ns
t_{btsu}	TCK [BSCAN test] setup time	20	–	ns
t_{bth}	TCK [BSCAN test] hold time	25	–	ns
t_{rf}	TCK [BSCAN test] rise and fall time	50	–	mV/ns
t_{btco}	TAP controller falling edge of clock to valid output	–	25	ns
t_{btoz}	TAP controller falling edge of clock to data output disable	–	25	ns
t_{btvo}	TAP controller falling edge of clock to data output enable	–	25	ns
t_{btcpsu}	BSCAN test Capture register setup time	20	–	ns
t_{btcph}	BSCAN test Capture register hold time	25	–	ns
t_{btuco}	BSCAN test Update reg, falling edge of clock to valid output	–	50	ns
t_{btuoz}	BSCAN test Update reg, falling edge of clock to output disable	–	50	ns
t_{btuov}	BSCAN test Update reg, falling edge of clock to output enable	–	50	ns

Signal Descriptions

Signal Name	Description
I/O	Input/Output Pins – These are the general purpose bidirectional data pins. When used as outputs, each may be independently latched, registered or tristated. They can also each assume one other control function (OE, CLK/CLKEN, and MUXsel as described in the text).
$\overline{\text{RESET}}$ / I/O D10	This pin can be configured by the user through software to act as a $\overline{\text{RESET}}$ pin or as an I/O (I/O D10) The default is $\overline{\text{RESET}}$. If programmed to act as $\overline{\text{RESET}}$, this pin is an active LOW Input Pin and resets all I/O Register outputs when LOW.
Y1/CLKEN1/TOE, Y0/CLKEN0	Input Pins – These can be either Global Clocks or Clock Enables. In addition, Y1 is multiplexed with TOE. Each pin can drive any or all I/O cell registers. The Test Output Enable (TOE) pin tristates all I/O pins when LOW
EPEN	Input Pin – JTAG TAP Controller Enable Pin. When high, JTAG operation is enabled. When low, JTAG TAP controller is driven to reset.
TDI	Input Pin – Serial data input during ISP programming or Boundary Scan mode.
TCK	Input Pin – Serial data clock during ISP programming or Boundary Scan mode.
TMS	Input Pin – Control input during ISP programming or Boundary Scan mode.
TDO	Output Pin – Serial data output during ISP programming or Boundary Scan mode.
GND	Ground (GND)
VCC	Vcc – Supply voltage (3.3V).
VCCIO	Input – This pin is used if optional 2.5V output is to be used. Every I/O can independently select either 3.3V or the optional voltage as its output level. If the optional output voltage is not required, this pin must be connected to the VCC supply. Programmable pull-up resistors and bus-hold latches only draw current from this supply.

Signal Locations: ispGDX80VA

Signal	100-Pin TQFP
$\overline{\text{RESET}}$ /I/O D10	90
Y0/CLKEN0	38
Y1/CLKEN1/TOE	87
EPEN	35
TDI	39
TCK	36
TMS	86
TDO	85
GND	6, 18, 29, 45, 56, 68, 79, 95
VCC	12, 37, 62, 88
VCCIO	89

I/O Locations: ispGDX80VA

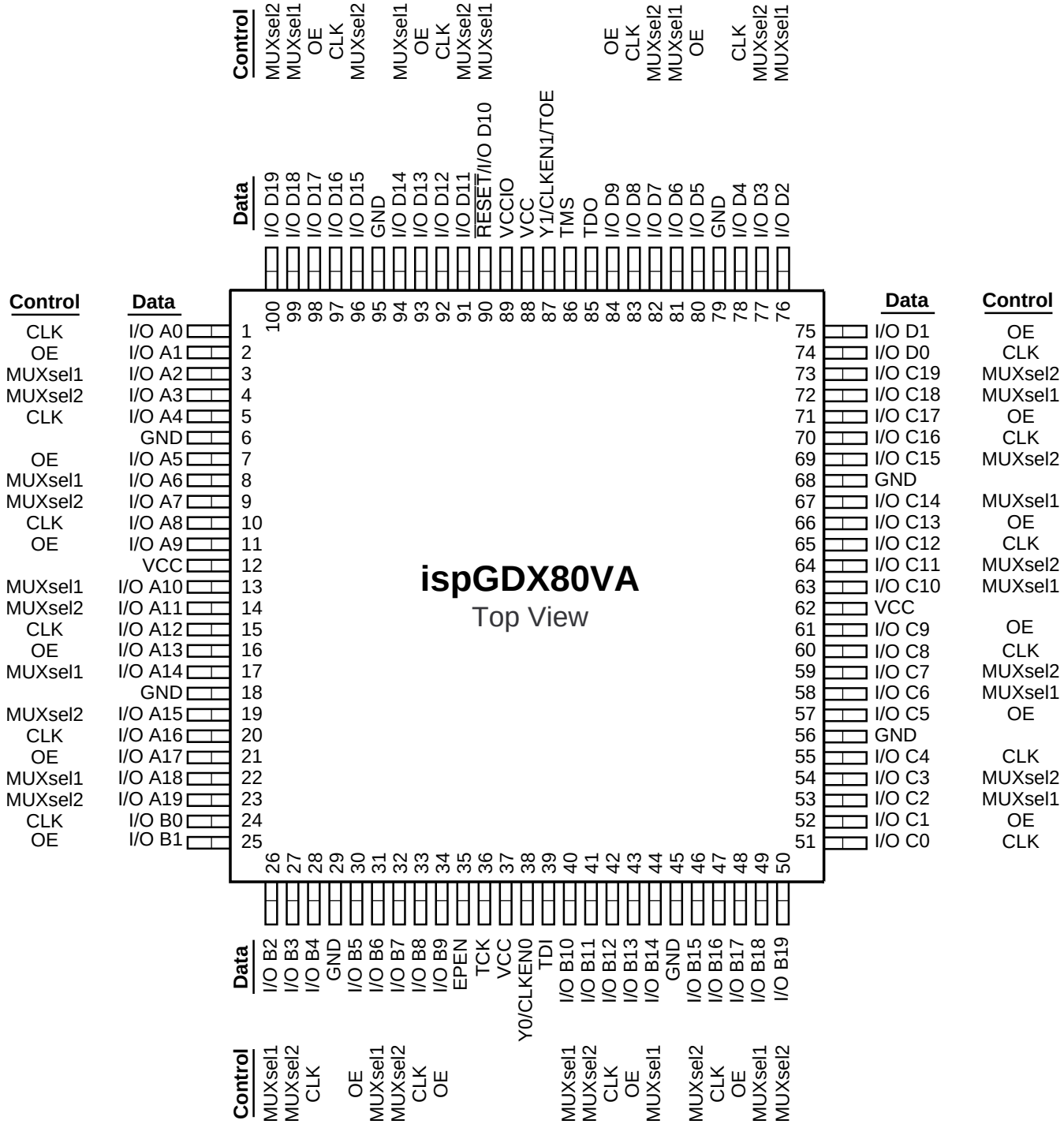
I/O Signal	Control Signal	100 TQFP	I/O Signal	Control Signal	100 TQFP	I/O Signal	Control Signal	100 TQFP	I/O Signal	Control Signal	100 TQFP
I/O A0	CLK	1	I/O B1	OE	25	I/O C2	MUXsel1	53	I/O D3	MUXsel2	77
I/O A1	OE	2	I/O B2	MUXsel1	26	I/O C3	MUXsel2	54	I/O D4	CLK	78
I/O A2	MUXsel1	3	I/O B3	MUXsel2	27	I/O C4	CLK	55	GND		
I/O A3	MUXsel2	4	I/O B4	CLK	28	GND			I/O D5	OE	80
I/O A4	CLK	5	GND			I/O C5	OE	57	I/O D6	MUXsel1	81
GND			I/O B5	OE	30	I/O C6	MUXsel1	58	I/O D7	MUXsel2	82
I/O A5	OE	7	I/O B6	MUXsel1	31	I/O C7	MUXsel2	59	I/O D8	CLK	83
I/O A6	MUXsel1	8	I/O B7	MUXsel2	32	I/O C8	CLK	60	I/O D9	OE	84
I/O A7	MUXsel2	9	I/O B8	CLK	33	I/O C9	OE	61	VCC		
I/O A8	CLK	10	I/O B9	OE	34	VCC			VCCIO		
I/O A9	OE	11	VCC			I/O C10	MUXsel1	63	I/O D10*	MUXsel1	90
VCC			I/O B10	MUXsel1	40	I/O C11	MUXsel2	64	I/O D11	MUXsel2	91
I/O A10	MUXsel1	13	I/O B11	MUXsel2	41	I/O C12	CLK	65	I/O D12	CLK	92
I/O A11	MUXsel2	14	I/O B12	CLK	42	I/O C13	OE	66	I/O D13	OE	93
I/O A12	CLK	15	I/O B13	OE	43	I/O C14	MUXsel1	67	I/O D14	MUXsel1	94
I/O A13	OE	16	I/O B14	MUXsel1	44	GND			GND		
I/O A14	MUXsel1	17	GND			I/O C15	MUXsel2	69	I/O D15	MUXsel2	96
GND			I/O B15	MUXsel2	46	I/O C16	CLK	70	I/O D16	CLK	97
I/O A15	MUXsel2	19	I/O B16	CLK	47	I/O C17	OE	71	I/O D17	OE	98
I/O A16	CLK	20	I/O B17	OE	48	I/O C18	MUXsel1	72	I/O D18	MUXsel1	99
I/O A17	OE	21	I/O B18	MUXsel1	49	I/O C19	MUXsel2	73	I/O D19	MUXsel2	100
I/O A18	MUXsel1	22	I/O B19	MUXsel2	50	I/O D0	CLK	74			
I/O A19	MUXsel2	23	I/O C0	CLK	51	I/O D1	OE	75			
I/O B0	CLK	24	I/O C1	OE	52	I/O D2	MUXsel1	76			

*I/O D10 is multiplexed with $\overline{\text{RESET}}$. The functionality is programmable and selected through software.

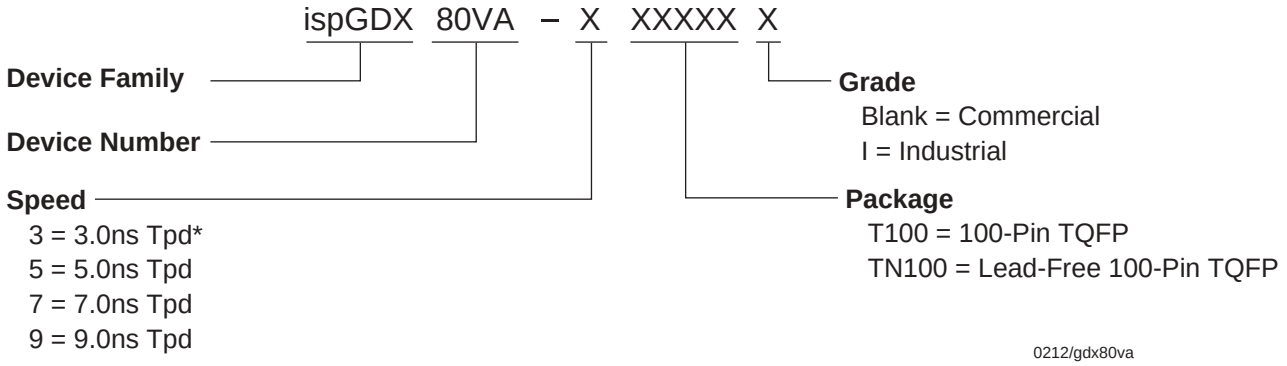
Note: VCC and GND Pads Shown for Reference

Pin Configuration: ispGDX80VA

ispGDX80VA 100-Pin TQFP Pinout Diagram



Part Number Description



Ordering Information

Conventional Packaging

COMMERCIAL

FAMILY	tpd (ns)	ORDERING NUMBER	PACKAGE
ispGDXVA	3.0*	ispGDX80VA-3T100	100-Pin TQFP
	5.0	ispGDX80VA-5T100	100-Pin TQFP
	7.0	ispGDX80VA-7T100	100-Pin TQFP

INDUSTRIAL

FAMILY	tpd (ns)	ORDERING NUMBER	PACKAGE
ispGDXVA	5.0	ispGDX80VA-5T100I	100-Pin TQFP
	7.0	ispGDX80VA-7T100I	100-Pin TQFP
	9.0	ispGDX80VA-9T100I	100-Pin TQFP

Note: The ispGDX80VA devices are dual-marked with both Commercial and Industrial grades. The Commercial speed grade is faster, e.g. ispGDX80VA-3T100-5I.

*The new "-3" speed grade (tpd = 3.0ns) will be effective starting with date code A113xxxx.

Lead-Free Packaging

COMMERCIAL

FAMILY	tpd (ns)	ORDERING NUMBER	PACKAGE
ispGDXVA	3.0*	ispGDX80VA-3TN100	Lead-Free 100-Pin TQFP
	5.0	ispGDX80VA-5TN100	Lead-Free 100-Pin TQFP
	7.0	ispGDX80VA-7TN100	Lead-Free 100-Pin TQFP

INDUSTRIAL

FAMILY	tpd (ns)	ORDERING NUMBER	PACKAGE
ispGDXVA	5.0	ispGDX80VA-5TN100I	Lead- Free 100-Pin TQFP
	7.0	ispGDX80VA-7TN100I	Lead- Free 100-Pin TQFP
	9.0	ispGDX80VA-9TN100I	Lead- Free 100-Pin TQFP

Note: The ispGDX80VA devices are dual-marked with both Commercial and Industrial grades. The Commercial speed grade is faster, e.g. ispGDX80VA-3T100-5I.

*The new "-3" speed grade (t_{PD} = 3.0ns) will be effective starting with date code A113xxxx.

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