International
IOR Rectifier

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IRS2158D(S)

Advanced Information

Features

- Ballast control and half-bridge driver in one IC
- Programmable half-bridge over-current protection
- Programmable preheat frequency
- Programmable preheat time
- Programmable ignition ramp
- Programmable run frequency
- Closed-loop ignition current regulation
- Voltage-controlled oscillator (VCO)
- Programmable deadtime
- End-of-life window comparator pin
- Internal 60-event current sense up/down fault counter
- Lamp removal/auto-restart shutdown pin
- Brownout protection
- Low offset op amp
- Internal bootstrap MOSFET
- Internal 15.6 V zener clamp diode on Vcc
- Micropower startup (250 µA)
- Latch immunity and ESD protection

Typical Applications

- Fluorescent lamp ballast dimming (<5%)

Product Summary

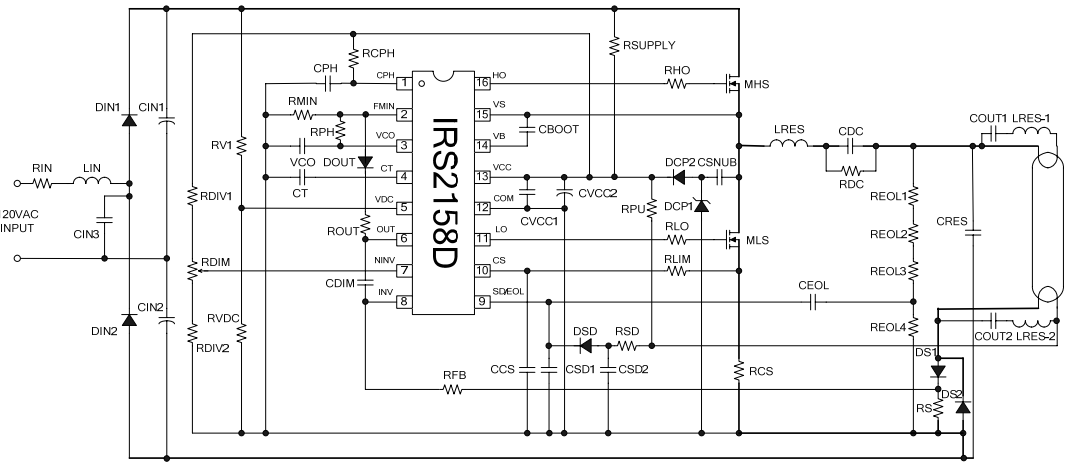
Topology	Half-Bridge
V_{OFFSET}	600 V
Vio (typical)	0V
I_{o+} & I_{o-} (typical)	180 mA & 260 mA
Start-up current (typical)	250 µA

Package Options

PDIP16

SOICN16

Typical Connection Diagram



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Description

The IRS2158D is a fully integrated, fully protected 600V ballast control IC designed to drive all types of fluorescent lamps. The IRS2158D features include programmable preheat and run frequencies, programmable preheat time, closed-loop half-bridge ignition current regulation, programmable end-of-life protection, brownout protection and low input offset op amp. The op amp can be used for dimming, current or power control. Comprehensive protection features such as protection from failure of a lamp to strike, filament failures, end-of-life protection, have been included in the design. The IRS2158D is available in both 16-pin PDIP and 16-pin narrow body SOIC packages.

Qualification Information†

Qualification Level		Industrial††	
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level		SOIC16N	MSL2†† 260°C (per IPC/JEDEC J-STD-020)
		PDIP16	Not applicable (non-surface mount package style)
ESD	Machine Model	Class B (per JEDEC standard JESD22-A115)	
	Human Body Model	Class 3A (per EIA/JEDEC standard EIA/JESD22-A114)	
IC Latch-Up Test		Class I, Level A (per JESD78)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_B	VB Pin High-Side Floating Supply Voltage	-0.3	625	V
V_S	VS Pin High-Side Floating Supply Offset Voltage	V_B – 25	V_B + 0.3	
V_{HO}	HO Pin High-Side Floating Output Voltage	V_S - 0.3	V_B + 0.3	
V_{LO}	LO Pin Low-Side Output Voltage	-0.3	V_{CC} + 0.3	
I_{OMAX}	Maximum allowable output current (HO, LO) due to external power transistor miller effect	-500	500	mA
V_{CPH}	CPH Pin Voltage	-0.3	V_{CC} + 0.3	V
I_{VCO}	VCO Pin Current	-5	5	mA
I_{FMIN}	FMIN Pin Current			
V_{VCO}	VCO Pin Voltage	-0.3	V_{CC} + 0.3	V
V_{NINV}	NINV pin voltage			
V_{INV}	INV pin voltage			
V_{OUT}	OUT pin voltage			
V_{CT}	CT Pin Voltage			
I_{CT}	CT Pin Current	-5	5	mA
V_{DC}	VDC Pin Voltage	-0.3	V_{CC} + 0.3	V
I_{DC}	VDC Pin Current	-5	5	mA
$V_{SD/EOL}$	SD/EOL Pin Voltage	-0.3	V_{CC} + 0.3	V
$I_{SD/EOL}$	SD/EOL Pin Current	-5	5	mA
V_{CS}	CS Pin Voltage	-0.3	V_{CC} + 0.3	V
I_{CS}	CS Pin Current	-5	5	mA
dV/dt	Allowable VS Pin Offset Voltage Slew Rate	-50	50	V/ns
P_D	Package Power Dissipation @ TA ≤ +25ºC (16-Pin DIP)	---	1.3	W
	$P_D = (T_{JMAX}-T_A)/R_{\theta JA}$ (16-Pin SOIC)	---	1.4	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (16-Pin DIP)	---	70	ºC/W
	(16-Pin SOIC)	---	82	
T_J	Junction Temperature	-55	150	ºC
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (soldering, 10 seconds)	---	300	

† This IC contains a zener clamp structure between the chip VCC and COM which has a nominal breakdown voltage of 15.6V. This supply pin should not be driven by a DC, low impedance power source greater than the VCLAMP specified in the Electrical Characteristics section.

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
V_{B}-V_{S}	High Side Floating Supply Voltage	V_{BUV+}	V_{CLAMP}	V
V_{S}	Steady State High-side Floating Supply Offset	-1	600	
V_{CC}	Supply Voltage	V_{CCUV+}	V_{CLAMP}	
I_{CC}	V_{CC} Supply Current	††	10	mA
$I_{SD/EOL}$	SD/EOL Pin Current	-1	1	
I_{CS}	CS Pin Current			
V_{VCO}	VCO Pin Voltage	0	5	V
R_{FMIN}	FMIN Pin Programming Resistor	10	300	kΩ
T_{J}	Junction Temperature	-40	125	ºC

†† Enough current should be supplied into the VCC pin to keep the internal 15.6V zener clamp diode on this pin regulated at its voltage, V_{CLAMP}.

Recommended Component Values

Symbol	Component	Min.	Max.	Units
RFMIN	R_{FMIN} Pin Resistor Value	10	---	kΩ
CT	CT Pin Capacitor Value	330	---	pF

Electrical Characteristics

V_{CC} = V_{BS} = V_{BIAS}=14V +/- 0.25V, C_{LO} = C_{HO} = 1000pF, CT = 1000pF, RFMIN = 15kΩ,
V_{CPH} = V_{VCO} = 0V, $V_{SD/EOL}$ = 0V, V_{CS} = 0V, T_A=25 °C unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Supply Characteristics						
V_{CCUV+}	V_{CC} Supply Under-voltage Positive Going Threshold	11.5	12.5	13.5	V	V_{CC} rising from 0V
V_{CCUV-}	V_{CC} Supply Under-voltage Negative Going Threshold	9.5	10.5	11.5		V_{CC} falling from 14V
V_{UVHYS}	V_{CC} Supply Under-voltage Lockout Hysteresis	1.0	2.0	3.0		
I_{QCCUV}	UVLO Mode V_{CC} Quiescent Current	---	250	500	µA	V_{CC} = 8V
I_{QCCFLT}	FAULT Mode VCC Quiescent Current	---	350	700		MODE=FAULT
I_{CC}	V_{CC} Supply Current	---	3.5	---	mA	MODE = RUN, V_{VCO} = 5V
V_{CLAMP}	V_{CC} Zener Clamp Voltage	14.6	15.6	16.6	V	I_{CC} = 5mA
Floating Supply Characteristics						
I_{BS}	VBS Supply Current	---	1.0	---	mA	MODE = RUN
I_{QBSUV}	UVLO Mode VBS Quiescent Current	---	---	50	µA	V_{BS} = 6V
V_{BSUV+}	V_{BS} Supply Under-voltage Positive Going Threshold	9.0	10.0	11.0	V	V_{BS} rising from 0V
V_{BSUV-}	V_{BS} Supply Under-voltage Negative Going Threshold	8.0	9.0	10.0		V_{BS} falling from 14V
I_{LKVS}	VS Offset Supply Leakage Current	---	---	50	µA	V_B = V_S = 650V, V_{CC} = 8V
Ballast Control Preheat, Ignition and Run Mode Characteristics						
$V_{CPHEOP+}$	CPH Pin End Of Preheat Rising Threshold Voltage	8.8	9.3	9.8	V	
$V_{CPHSOI-}$	CPH Pin Start Of Ignition Falling Threshold Voltage	4.4	4.7	5.0		
V_{VCOPH}	VCO Pin Preheat Mode Voltage	---	0	---		MODE = PREHEAT
V_{VCOIGN}	VCO Pin Ignition Mode Voltage	---	0.65	---		MODE = IGNITION, V_{CS} = 1.5V, RPH = 22.1kΩ
I_{VCOIGN}	VCO Pin Ignition Regulation Discharge Current	---	215	---	µA	MODE = IGNITION, V_{VCO} = V_{VCOIGN}, V_{CS} = 1.5V
$V_{CPHRUN+}$	CPH Pin Run Mode Rising Threshold Voltage	8.8	9.3	9.8	V	MODE = IGNITION
V_{VCORUN}	VCO Pin Run Mode Voltage	---	OPEN	---		MODE = RUN

Electrical Characteristics (cont'd)

V_{CC} = V_{BS} = V_{BIAS}=14V +/- 0.25V, C_{LO} = C_{HO} = 1000pF, CT = 1000pF, RFMIN = 15kΩ, V_{CPH} = V_{VCO} = 0V, $V_{SD/EOL}$ = 0V, V_{CS} = 0V, T_A= °C unless otherwise specified.

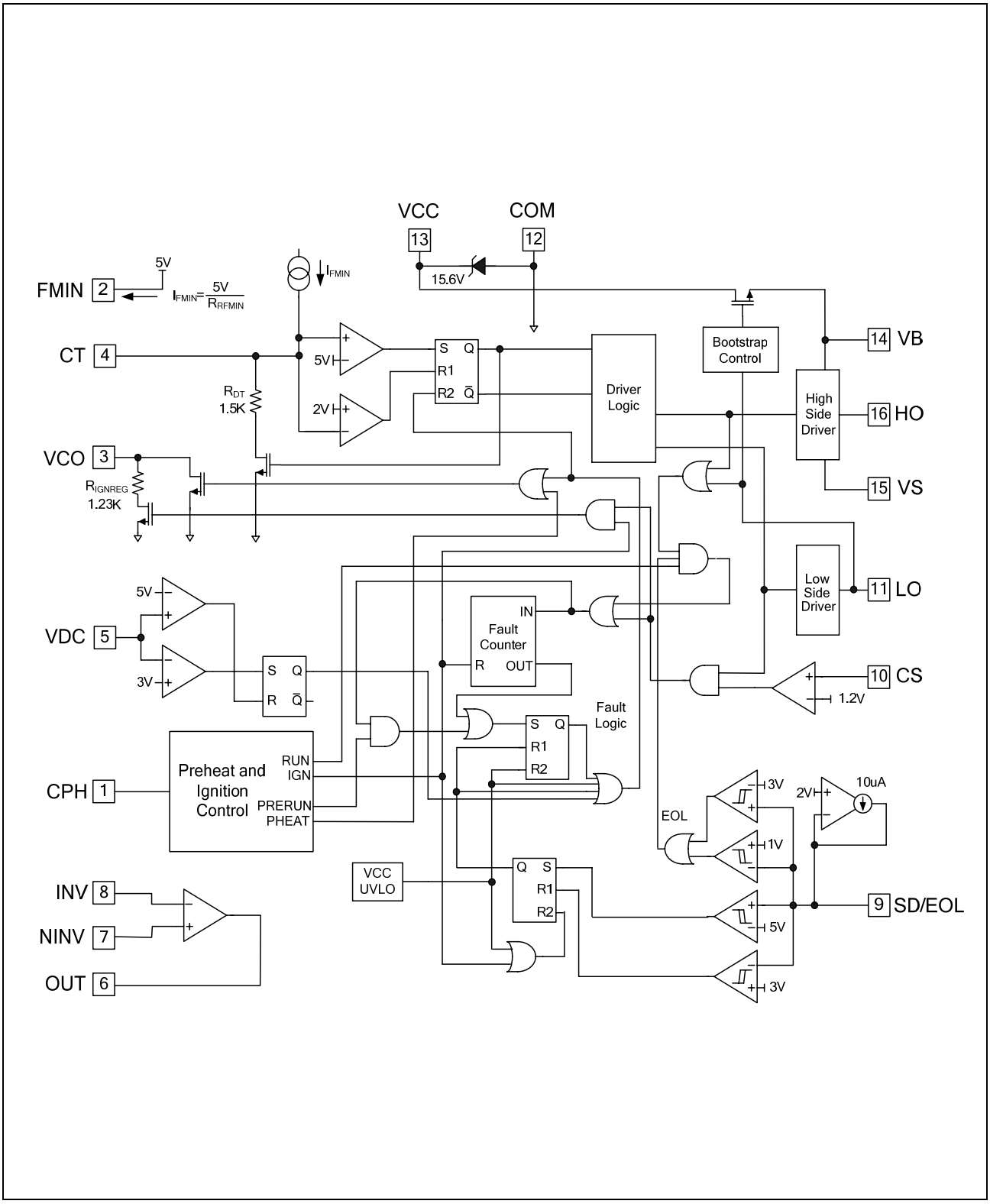
Ballast Control Protection Circuitry Characteristics						
V_{CSTH+}	CS Pin Over-current Sense Threshold	1	1.2	1.4	V	
n_{EVENTS}	CS and EOL Fault Counter No. of Events	---	60	---	Events	MODE = PREHEAT or RUN
V_{SDTH+}	SD Pin Rising Non-latched Shutdown Threshold Voltage	4.5	5.0	5.5	V	
V_{SDTH-}	SD Pin Falling Reset Threshold Voltage	2.7	3.0	3.3		
$V_{EOLBIAS}$	EOL Pin Internal Bias Voltage	1.8	2.0	2.2		
V_{EOLTH+}	EOL Pin Rising Latched Shutdown Threshold Voltage	2.7	3.0	3.3		MODE = RUN
V_{EOLTH-}	EOL Pin Falling Latched Shutdown Threshold Voltage	0.9	1.0	1.1		MODE = RUN
V_{DC+}	VDC Pin Enable	4.5	5.0	5.5		ALL MODES
V_{DC-}	VDC Pin Disable	2.7	3.0	3.4		
$I_{EOLSOURCE}$	EOL Pin OTA Output Sourcing Current	---	10	---	µA	MODE = PREHEAT V_{EOL} = 1.5V
$I_{EOLSINK}$	EOL Pin OTA Output Sinking Current	---	-10	---		MODE = PREHEAT V_{EOL} = 2.5V
V_{CPHFLT}	CPH Pin Fault Mode Voltage	---	0	---	V	MODE = FAULT
V_{VCOFLT}	VCO Pin Fault Mode Voltage					
$V_{FMINFLT}$	FMIN Pin Fault Mode Voltage					
Ballast Control Oscillator Characteristics						
f_{RUN}	Half-bridge Oscillator Run Frequency	42.5	45.5	48.5	kHz	MODE = RUN
f_{PH}	Half-bridge Oscillator Preheat Frequency	63	68	73	kHz	RPH = 22.1kΩ, MODE = PREHEAT
V_{CT+}	Upper CT Ramp Voltage Threshold	---	5.0	---	V	MODE = RUN
V_{CT-}	L CT Ramp Voltage Threshold	---	2.0	---		MODE = RUN
d	Oscillator duty cycle	---	50	---	%	MODE = RUN, td_{LO} and td_{HO} removed
td_{LO}	LO Output Deadtime	---	1.5	---	µs	
td_{HO}	HO Output Deadtime	---	1.5	---		
V_{FMIN}	FMIN Pin Voltage	4.6	5.0	5.4	V	VCC = 14.0V

Electrical Characteristics (cont'd)

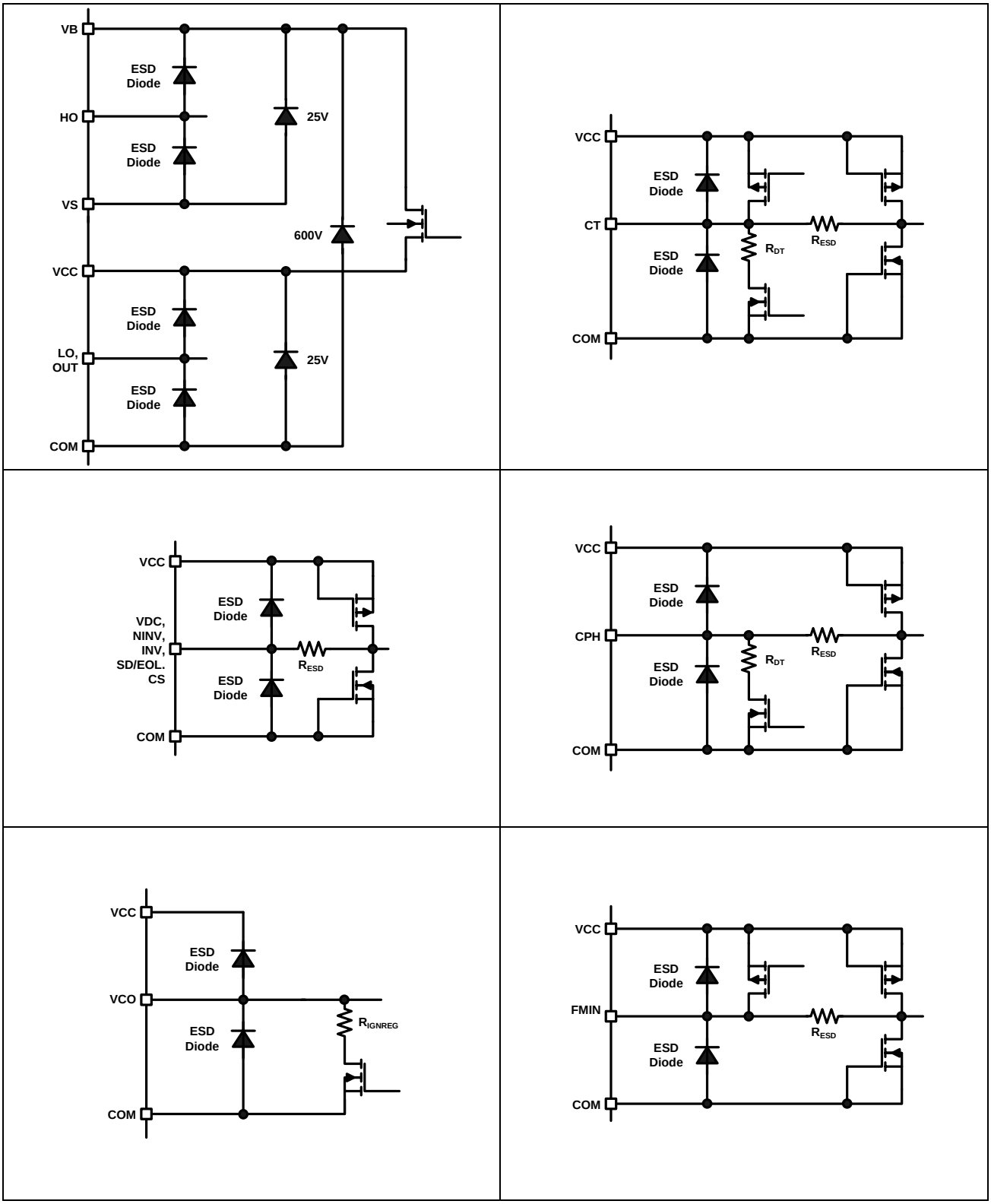
V_{CC} = V_{BS} = V_{BIAS}=14V +/- 0.25V, C_{LO} = C_{HO} = 1000pF, CT = 1000pF, RFMIN = 15kΩ,
V_{CPH} = V_{VCO} = 0V, $V_{SD/EOL}$ = 0V, V_{CS} = 0V, T_A=25 °C unless otherwise specified.

Gate Driver Output Characteristics (HO, LO)						
V_{OL}	Low-Level Output Voltage	---	0	100	mV	IO = 0
V_{OH}	High-Level Output Voltage	---	0	100		V_{BIAS} - V_O , I_O = 0
t_r	Turn-On Rise Time	---	120	180	ns	C_{HO}=C_{LO}= 1nF
t_f	Turn-Off Fall Time	---	50	100		
I_{0+}	Source Current	---	180	---	mA	
I_{0-}	Sink Current	---	260	---		
Bootstrap FET Characteristics						
VB_{ON}	VB when the bootstrap FET is on	13.7	14.0	---	V	
IB_{CAP}	VB source current when FET is on	30	55	---	mA	VB = COM
IB_{10V}	VB source current when FET is on	8	12	---		VB=10V
Op Amp Characteristics						
I_{ib}	NINV and INV pin Input bias current	---	---	0.1	µA	
V_{io}	Input Offset Voltage	-10	0	10	mV	
I_{OUT+}	OUT pin Sink Output Current	---	12	---	mA	INV=7V, NINV=0V
I_{OUT-}	OUT pin Source Output Current	---	14	---		INV=7V, NINV=14V
Vic	Common Mode Input Range	0	---	11.5	V	
Unity Gain BW	Operational Amplifier Band Width	---	2.0	---	MHz	Guaranteed By Design
G_{DC}	DC Open Loop Gain	---	110	---	dB	

Functional Block Diagram



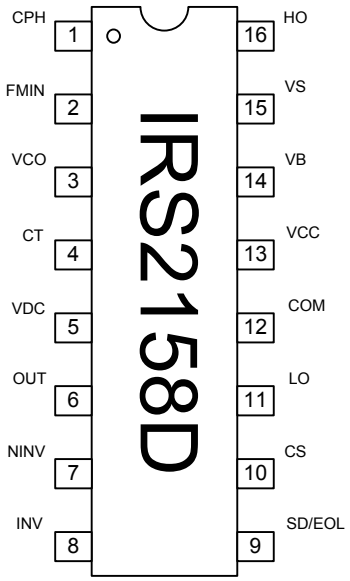
Input/Output Pin Equivalent Circuit Diagrams



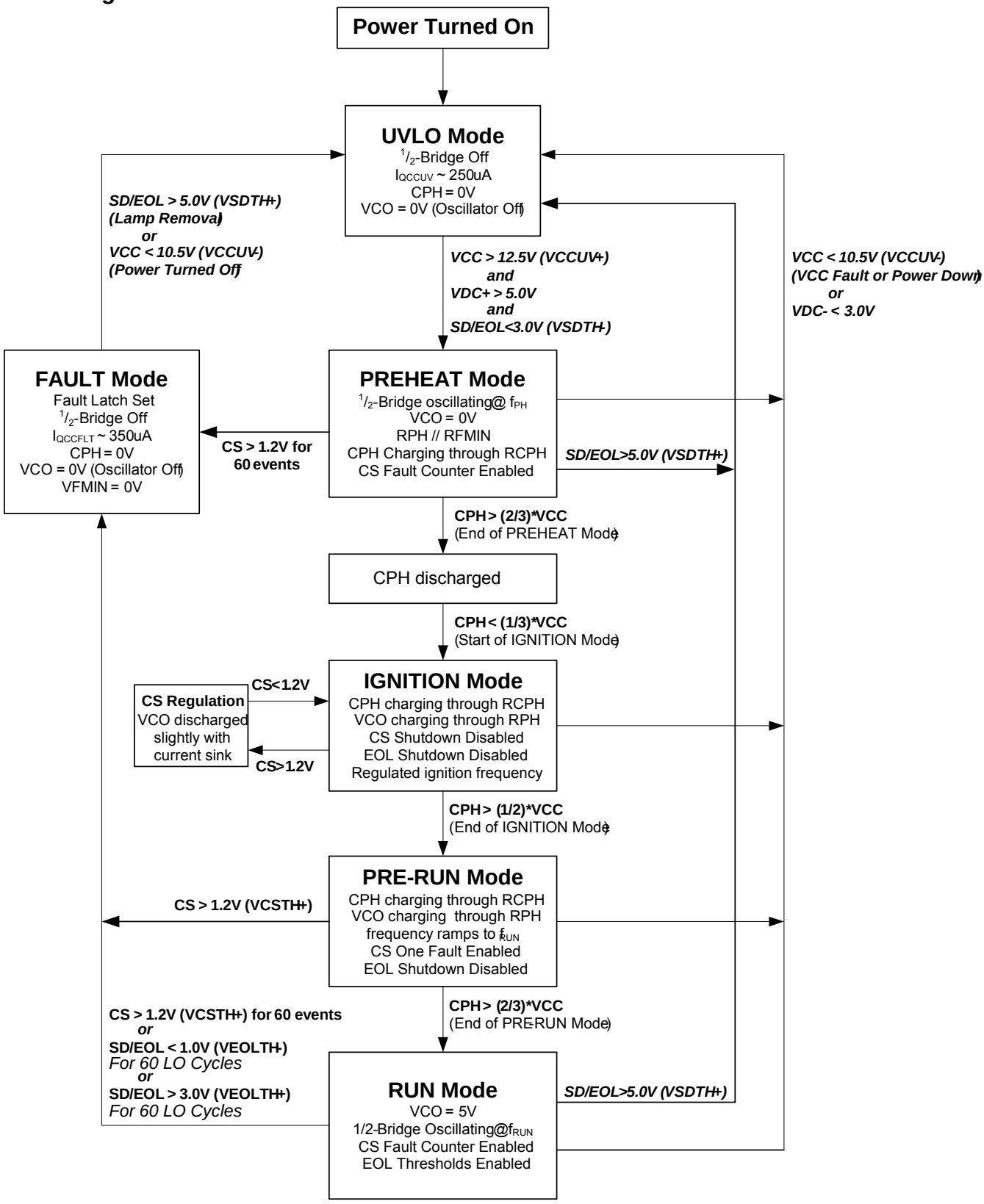
Lead Definitions

Pin#	Symbol	Description
1	CPH	Preheat Timing Input
2	FMIN	Oscillator Minimum Frequency Setting
3	VCO	Voltage Controlled Oscillator / Ignition Ramp Input
4	CT	Oscillator timing capacitor input
5	VDC	DC Bus monitoring / Brownout protection
6	OUT	Dimming OpAmp Output
7	NINV	Non-inverting pin of Dimming OpAmp
8	INV	Inverting pin of Dimming OpAmp
9	SD/EOL	Shut-Down / End of Life Sensing Input
10	CS	Half-Bridge Current Sensing Input
11	LO	Low-Side Gate Driver Output
12	COM	IC Power & Signal Ground
13	VCC	Logic & Low-Side Gate Driver Supply
14	VB	High-Side Gate Driver Floating Supply
15	VS	High Voltage Floating Return
16	HO	High-Side Gate Driver Output

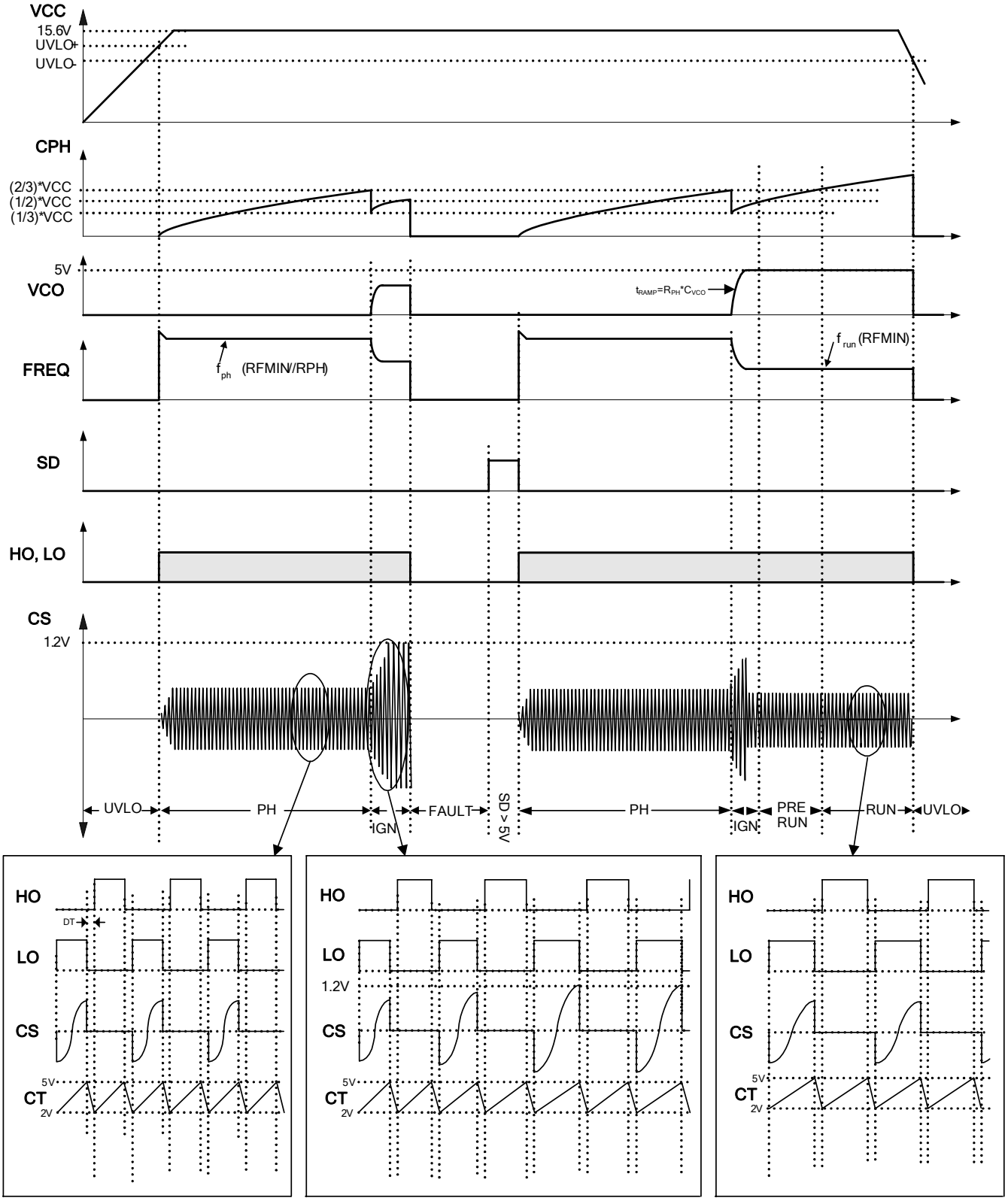
Lead Assignments

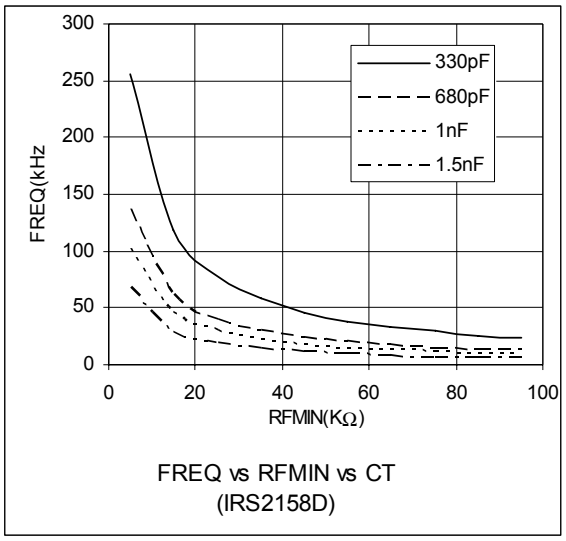


State Diagram

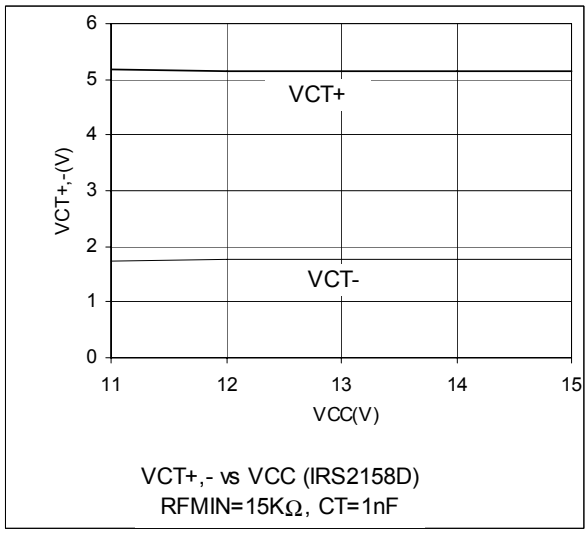


Timing Diagram Ballast Section

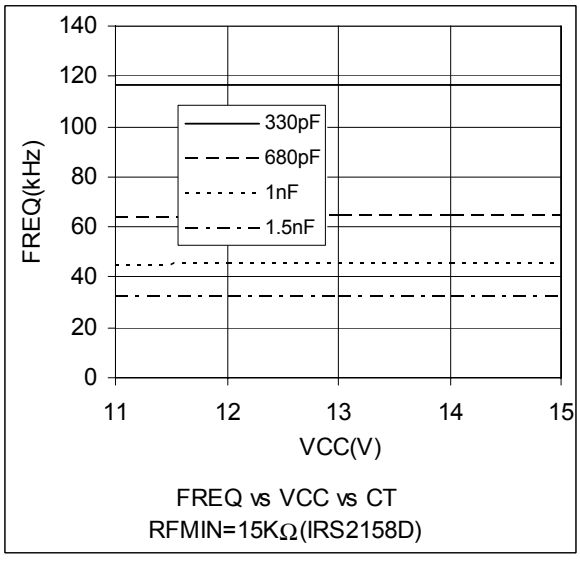




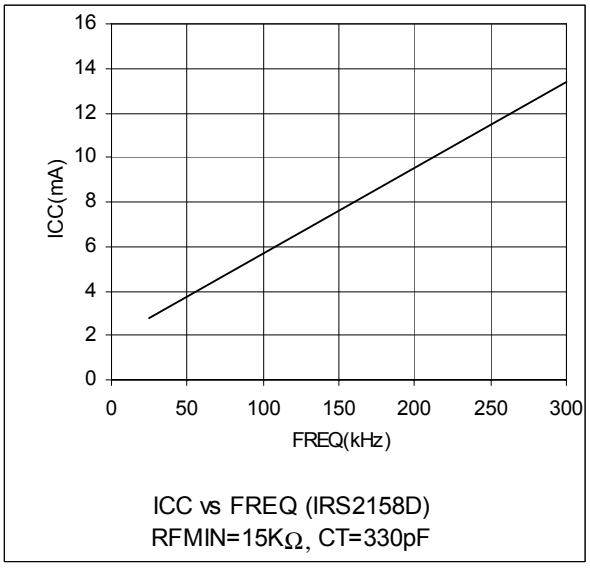
Graph 1. Run Frequency vs RFMIN and CT



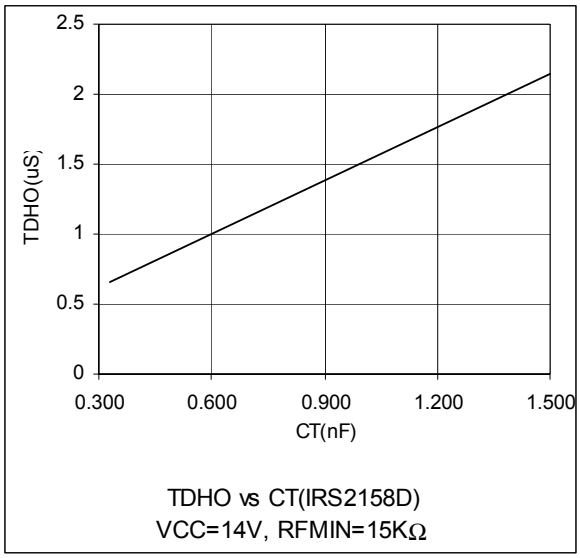
Graph 2. CT voltage thresholds vs VCC



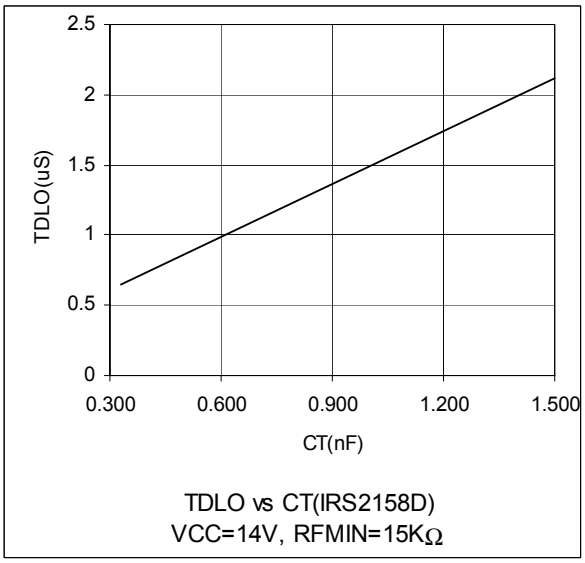
Graph 3. Run Frequency vs VCC and CT



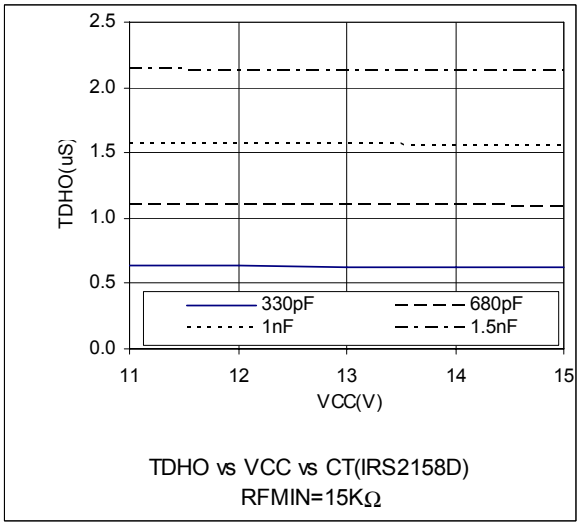
Graph 4. ICC vs Frequency



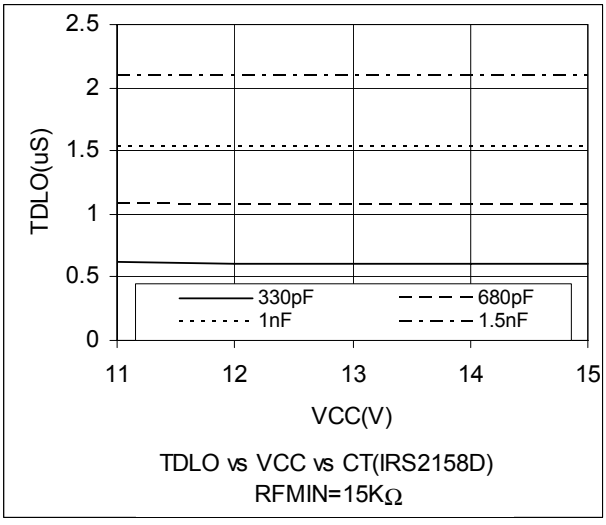
Graph 5. Dead Time TDHO vs CT



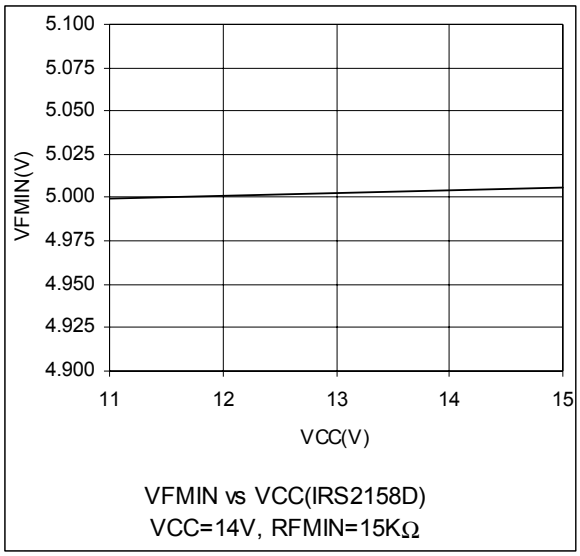
Graph 6. Dead Time TDLO vs CT



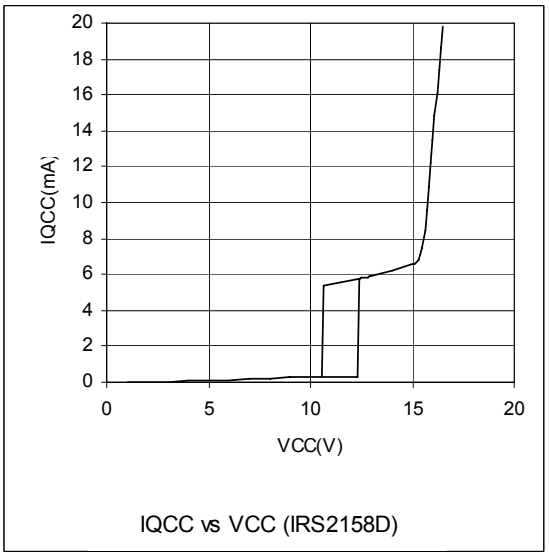
Graph 7. Dead Time TDHO vs VCC



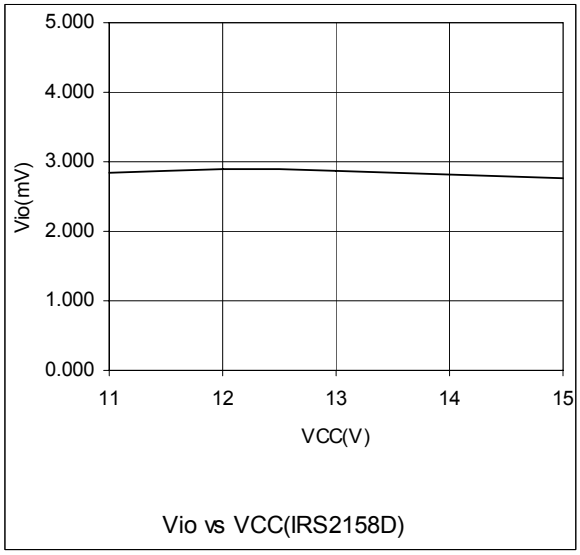
Graph 8. Dead Time TDLO vs VCC



Graph 9. VFMIN vs VCC



Graph 10. IQCC vs VCC



Graph 11. Vio vs VCC

Application Information and Additional Details

Information regarding the following topics is included as subsections within this section of the datasheet:

- Under-Voltage Lock-Out (UVLO) Mode and IC Supply Circuitry
- Preheat Mode (PH)
- Ignition Mode (IGN)
- Pre-Run Mode
- Run Mode (RUN)
- Dimming
- SD/EOL and CS Fault Mode
- Brown-out protection
- Component Selection
- Vcc double filter
- PCB Layout Guidelines

Under-voltage Lock-Out Mode (UVLO) Mode and IC Supply Circuitry

The under-voltage lock-out mode (UVLO) is defined as the state the IC is in when VCC is below the turn-on threshold of the IC. To identify the different modes of the IC, refer to the State Diagram shown on page 14 of this document. The IRS2158D undervoltage lock-out is designed to maintain an ultra low supply current of less than 500 µA, and to guarantee the IC is fully functional before the high- and low-side output drivers are activated. Figure 1 shows an efficient supply voltage using the micro-power start-up current of the IRS2158D together with a snubber charge pump from the half-bridge output (R_{VCC}, C_{VCC1}, C_{VCC2}, C_{SNUB}, D_{CP1} and D_{CP2}).

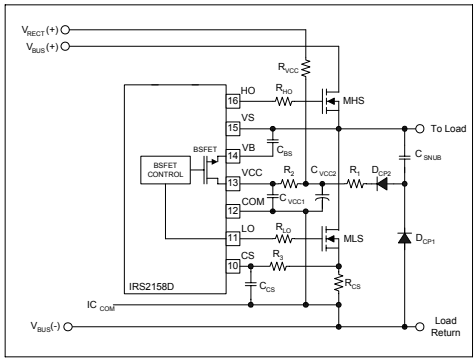


Figure 1: Start-up and supply circuitry.

The VCC capacitors (C_{VCC1} and C_{VCC2}) are charged by the current through supply resistor (R_{VCC}) minus the start-up current drawn by the IC. This resistor is chosen to set the desired AC line input voltage turn-on threshold for the ballast. When the voltage at VCC exceeds the IC start-up threshold (VCCUV+) and the VDC pin is above 5 V and the SD pin is below 3 V, the IC turns on and LO begins to oscillate. The capacitors at VCC begin to discharge due to the increase in IC operating current (Figure 2). The high-side supply voltage, VB-VS, begins to increase as capacitor C_{BS} is charged through the internal bootstrap MOSFET during the LO on-time of each LO switching cycle. When the VB-VS voltage exceeds the high-side start-up threshold (VBSUV+), HO then begins to oscillate. This may take several cycles of LO to charge VB-VS above VBSUV+ due to RDSon of the internal bootstrap MOSFET.

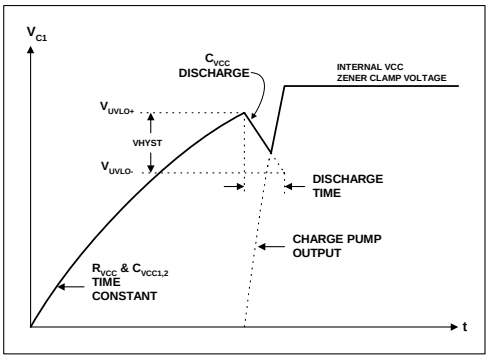


Figure 2: VCC supply voltage.

When LO and HO are both oscillating, the external MOSFETs (MHS and MLS) are turned on and off with a 50% duty cycle and a non-overlapping deadtime of 1.5 µs. The half-bridge output (pin VS) begins to switch between the DC bus voltage and COM. During the deadtime between the turn-off of LO and the turn-on of HO, the half-bridge output voltage transitions from COM to the DC bus voltage at a dv/dt rate determined by the snubber capacitor (C_{SNUB}). As the snubber capacitor charges, current will flow through the charge pump diode (D_{CP2}) to VCC. After several switching cycles of the half-bridge output, the charge pump and the internal 15.6 V zener clamp of the IC take over as the supply voltage. Capacitor C_{VCC2} supplies the IC current during the VCC discharge time and should be large enough such that VCC does not decrease below VCCUV- before the charge pump takes over. Capacitor C_{VCC1} is required for noise filtering and must be placed as close as possible and directly between VCC and COM, and should not be lower than 0.1uF. Additional resistors are recommended for limiting high currents that can flow to VCC from the charge pump during hard-switching of the half-bridge or during lamp ignition. In the application circuit shown above, DCP2 is a 17 V zener diode, which serves to limit the voltage transients that are supplied to VCC through the charge pump, under these conditions. The IC may not operate correctly if steps are not taken to prevent overdriving VCC through the charge pump.

The internal bootstrap MOSFET and supply capacitor (C_{BS}) comprise the supply voltage for the high side driver circuitry. During UVLO mode, the high- and low-side driver outputs HO and LO are both low, the internal oscillator is disabled, and pin CPH is connected internally to COM for resetting the preheat time.

Preheat Mode (PH)

The IRS2158D enters preheat mode when VCC exceeds the UVLO positive-going threshold (VCCUV+) and the VDC pin voltage is above the 5 V threshold. The internal MOSFET that connects pin CPH to COM is turned off and an external resistor (Figure 3) begins to charge the external preheat timing capacitor (CPH). LO and HO begin to oscillate at a higher soft-start frequency and ramp down quickly to the preheat frequency. The VCO pin is connected to COM through an internal

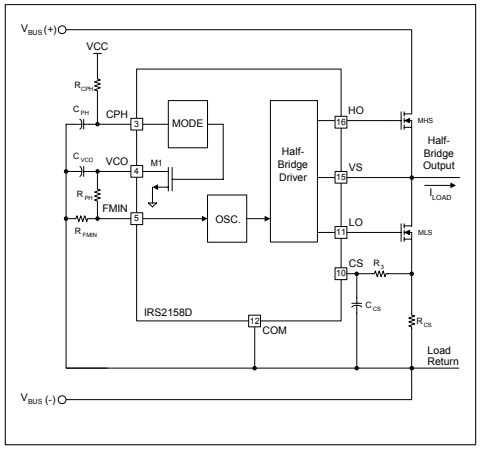


Figure 3: Preheat circuitry.

MOSFET so the preheat frequency is determined by the equivalent resistance at the FMIN pin formed by the parallel combination of resistors RMIN and RPH. The frequency remains at the preheat frequency until the voltage on pin CPH exceeds 2/3*VCC (VCPHEOP) and the IC enters Ignition Mode. During preheat mode, the over-current protection on pin CS (VCSTH+) and the 60-cycle consecutive over-current fault counter (nEVENTS) are both enabled.

Ignition Mode (IGN)

The IRS2158D ignition mode is defined by the second time CPH charges from 1/3*VCC (VCPHSOI-) to 1/2*VCC (VCHPRUN). When the voltage on pin CPH exceeds 2/3*VCC (VCPHEOP) for the first time, pin CPH is discharged quickly through an internal MOSFET down to 1/3*VCC (VCPHSOI-) (see Figures 4 and 5). The internal MOSFET turns off and the voltage on pin CPH begins to increase again. The internal MOSFET at pin VCO turns off and resistor RPH is disconnected from COM. The equivalent resistance at the FMIN pin increases from the parallel combination (RPH//RMIN) to RMIN at a rate programmed by the external capacitor at pin VCO (CVCO) and resistor RPH. This causes the operating frequency to ramp down smoothly from the preheat frequency through the ignition frequency to the final run frequency. During this ignition ramp, the frequency sweeps towards the resonance frequency of the lamp output stage to ignite the lamp.

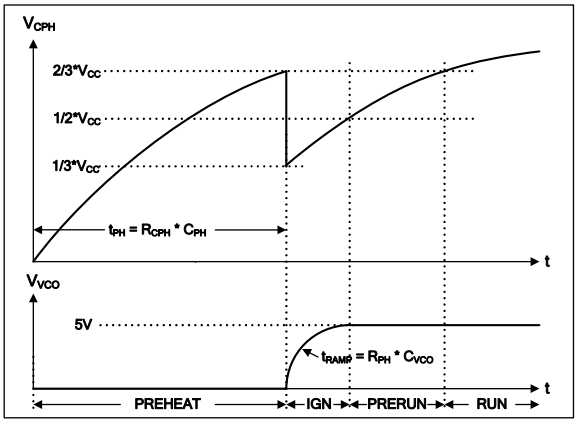


Figure 4: CPH and VCO timing diagram.

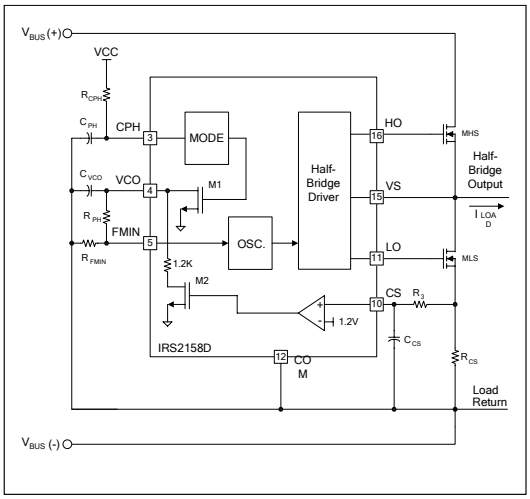


Figure 5: Ignition circuitry.

The over-current threshold on pin CS (VCSTH+) will protect the ballast against a non-strike or open-filament lamp fault condition. The voltage on pin CS is defined by the lower half-bridge MOSFET current flowing through the external current sensing resistor RCS. This resistor programs the maximum peak ignition current (and therefore peak ignition voltage) of the ballast output stage. Should this voltage exceed the internal VCSTH+ threshold of 1.2 V, the ignition regulation circuit discharges the VCO voltage slightly to increase the frequency slightly (see Figure 6). This cycle-by-cycle feedback from the CS pin to the VCO pin will adjust the frequency each cycle to limit the amplitude of the current for the entire duration of ignition mode.

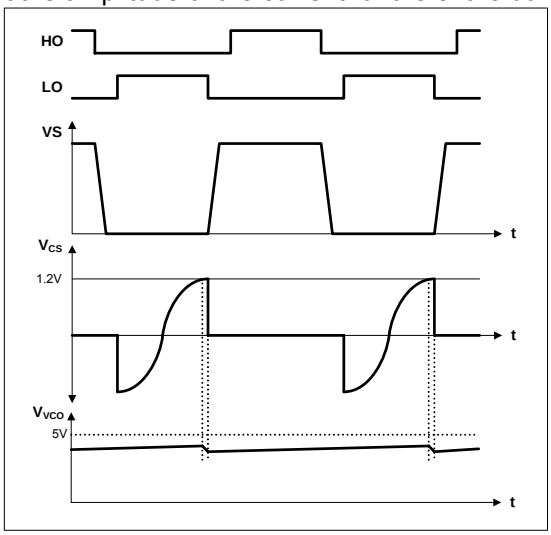


Figure 6: Ignition regulation timing diagram.

The IRS2158D remains in IGNITION mode until the voltage at CPH reaches 1/2*VCC at which point it will switch into PRE-RUN mode.

Pre-Run Mode

In PRE-RUN mode the fault counter is disables so that the IRS2158D will enter FAULT mode if a single event occurs where VCS>1.2 V (VCSTH+). This allows the ballast to shut down if the resonant inductor saturates during ignition.

When CPH exceeds 2/3*VCC (VCPHRUN+) for the second time, the IC enters run mode and the fault counter becomes enabled. The ignition regulation is not active in run mode but the IC will enter fault mode after 60 consecutive over-current faults and gate driver outputs HO and LO will be latched low.

Run Mode (RUN)

Once VCPH has exceeded 2/3*VCC for the second time (VCPHRUN), the IC enters run mode. CPH continues to charge up to VCC. The operating frequency is at the minimum frequency (after the ignition ramp) and is programmed by the external resistor (RMIN) at the FMIN pin. Should hard-switching occur at the half-bridge at any time (open-filament, lamp removal, etc.), the voltage across the current sensing resistor (RCS) will exceed the internal VCSTH+ threshold of 1.2 V and the fault counter will begin counting (see Figure 5). Should the number of consecutive over-current faults exceed 60 (nEVENTS), the IC will enter fault mode and the HO and LO gate driver outputs will be latched low. During run mode, the end-of-life (EOL) window comparator and the DC bus under-voltage reset are both enabled.

Dimming

The application diagram shows how the operational amplifier can be configured with the ballast control pins of the IRS2158 to realize a dimming ballast system, which regulates the lamp arc current. The opamp in this IC is left uncommitted, so that the designer can utilize it in whatever way they require for the particular application, for example it could be used to create a non-dimming ballast with regulated lamp power or a more sophisticated end of lamp life detection circuit.

In this example the lamp arc current is compared with a DC control voltage to produce an error voltage that steers the frequency by sinking current from the FMIN pin.

SD/EOL and CS Fault Mode

Should the voltage at the SD/EOL pin exceed 3 V or decrease below 1V (VEOLTH-) during run mode, an end-of-life (EOL) fault condition has occurred. The end of life fault must remain for approximately 60 cycles of LO before the IC enters fault mode. This is to prevent possible false tripping of the end of life shutdown circuit caused by surges or transients at the AC line input. LO and HO gate driver outputs are all latched off in the 'low' state. CPH is discharged to COM for resetting the preheat time and VCO is discharged to COM for resetting the frequency. To exit fault mode, VCC can be decreased below VCCUV- (ballast power off) or the SD pin can be increased above 5 V (VSDTH+) (lamp removal). Either of these will force the IC to enter UVLO mode (see State Diagram, page 13). Once VCC is above VCCUV+ (ballast power on) and SD is pulled above 5 V (VSDTH+) and back below 3 V (VSDTH-) (lamp re-insertion), the IC will enter preheat mode and begin oscillating again.

The current sense function will force the IC to enter fault mode only after the voltage at the CS pin has been greater than 1.2 V (VCSTH+) for 60 (nEVENTS) consecutive cycles of LO. The voltage at the CS pin is AND-ed with LO (see Figure 7) so it will work with pulses that occur during the LO on-time or DC. If the over-current faults are not consecutive, then the internal fault counter will count down each cycle when there is no fault. Should an over-current fault occur only for a few cycles and then not occur again, the counter will eventually reset to zero. The over-current fault counter is enabled during preheat and run modes and disabled during ignition mode.

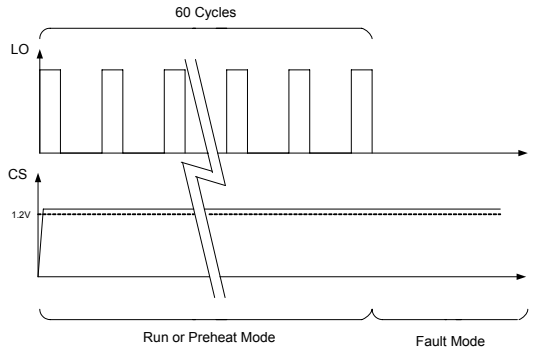


Figure 7: Fault counter timing diagram.

Brown-out protection

The DC pin senses the voltage on the DC bus by means of an external resistor divider and an internal comparator with hysterisis. When power is first supplied to the IC at system startup, 3 conditions are required before oscillation is initiated: 1.) the voltage on the VCC pin must exceed the rising undervoltage lockout threshold (VCCUV+), 2.) the voltage at the VDC pin must exceed VDC+, 3.) the voltage at the SD/EOL pin must be below 3 V. If a low DC bus condition occurs during normal operation, or if power to the ballast is shut off, the DC bus will collapse prior to the VCC of the chip (assuming the VCC is derived from a charge pump off of the output of the half-bridge). In this case, the voltage on the VDC pin will drop below the VDC- threshold and shut the oscillator off, thereby protecting the power transistors from potentially hazardous hard switching. Approximately 2 V of hysterisis has been designed into the internal comparator sensing the VDC pin, in order to account for variations in the DC bus voltage under varying load conditions. When the DC bus recovers, the chip restarts from the beginning of the control sequence, as shown in timing diagram Figure 8 below.

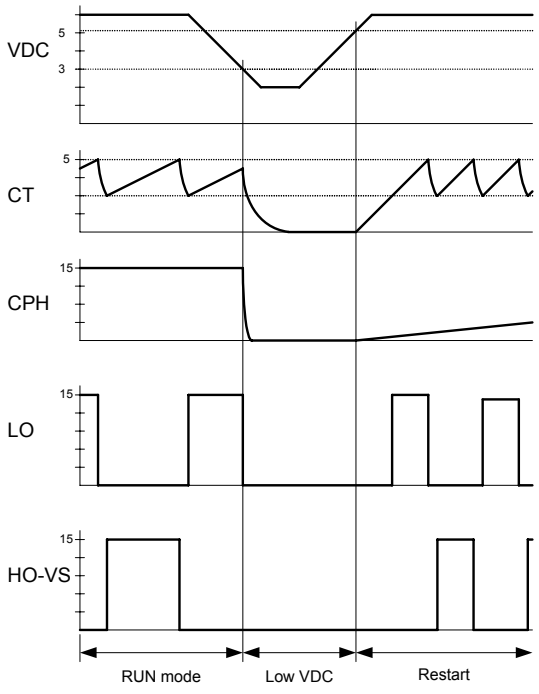


Figure 8: VDC pin fault and auto restart

Ballast Design Equations

Note: The results from the following design equations can differ slightly from actual measurements due to IC tolerances, component tolerances, and oscillator over- and under-shoot due to internal comparator response time.

Step 1: Program Deadtime

The deadtime is programmed with the timing resistor RDT at the DT pin. The deadtime is given by:

$$t_{DT} = 1500 \cdot C_T \quad \text{[Seconds]} \quad (1)$$

$$C_T = \frac{t_{DT}}{1500} \quad \text{[Farads]} \quad \textbf{(2)}$$

Step 2: Program Run Frequency

The run frequency is programmed with the timing resistor RMIN at the FMIN pin. The run frequency is given as:

$$f_{OSCRUN} = \frac{1}{2.15 \cdot C_T \cdot \left(\frac{3}{5} \cdot R_{MIN} + 1500\right)}$$

[Hz] (3)

$$R_{MIN} = \frac{5}{3} \cdot \left(\frac{1}{(2.15 \cdot f_{OSCRUN} \cdot C_T)} - 1500\right)$$

[Ohms] (4)

Step 3: Program Preheat Frequency

The preheat frequency is programmed with timing resistors RMIN and RPH. The timing resistors are connected in parallel for the duration of the preheat time. The preheat frequency is therefore given as:

$$f_{OSCPH} = \frac{1}{2.15 \cdot C_T \cdot \left(\frac{3}{5} \cdot \frac{(R_{MIN} \cdot R_{PH})}{(R_{MIN} + R_{PH})} + 1500\right)}$$

[Hertz] (5)

Step 4: Program Preheat Time

The preheat time is defined by the time it takes for the external capacitor on pin CPH to charge up to 2/3*VCC. An external resistor (RCPH) connected to VCC charges capacitor CPH. The preheat time is therefore given as:

$$t_{PH} = R_{CPH} \cdot C_{PH} \quad \text{[Seconds]} \quad (6)$$

or

$$C_{PH} = \frac{t_{PH}}{R_{CPH}} \qquad \text{[Farads]} \quad (7)$$

Step 5: Program Ignition Ramp Time

The preheat time is defined by the time it takes for the external capacitor on pin VCO to charge up to 5V. The external timing resistor (RPH) connected to FMIN charges capacitor CVCO. The ignition ramp time is therefore given as:

$$t_{RAMP} = R_{PH} \cdot C_{VCO} \qquad \text{[Seconds]} \ (8)$$

or

$$C_{VCO} = \frac{t_{RAMP}}{R_{PH}} \qquad \text{[Farads]} \quad (9)$$

Step 6: Program Maximum Ignition Current

The maximum ignition current is programmed with the external resistor RCS and an internal threshold of 1.2V. This threshold determines the over-current limit of the ballast, which will be reached when the frequency ramps down towards resonance during ignition and the lamp does not ignite. The maximum ignition current is given as:

$$I_{IGN} = \frac{1.2}{R_{CS}} \qquad \text{[Amps Peak]} \quad (10)$$

or

$$R_{CS} = \frac{1.2}{I_{IGN}} \qquad \text{[Ohms]} \quad (11)$$

VCC Double Filter

It is recommended to utilize a double filter arrangement from the charge pump (CSNUB, DCP1 and DCP2) to VCC as shown in the schematic of Figure 9. This circuit is designed to protect the VCC supply pin of the IRS2158D from high peak currents that occur when the MOSFET MHS switches VS from COM to VBUS. DCP2 should be an 18 V rated zener diode and RSUPPLY should connect to the cathode of DCP2. This is to protect the VCC input of the IRS2158D from possible surges and transient voltages.

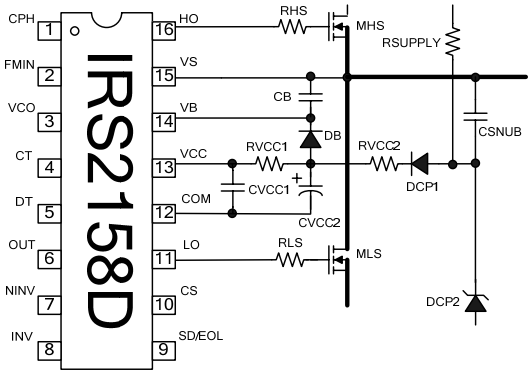


Figure 9: VCC Double Filter Arrangement

PCB Layout Considerations

In order to successfully utilize the IRS2158D in a ballast design, it is necessary to follow the following PCB layout guidelines. This can avoid possible interference and ground loop issues that can occur in the ballast circuit. These connection techniques also prevent high current ground loops from interfering with sensitive timing component operation and allow the entire control circuit to reject common-mode noise due to output switching.
Figure 10 and Figure 11 show the control section of typical ballast designed around the IRS2158D, where the IC is located in the center. In this design all SMD devices are mounted under the PCB with discrete devices on top.

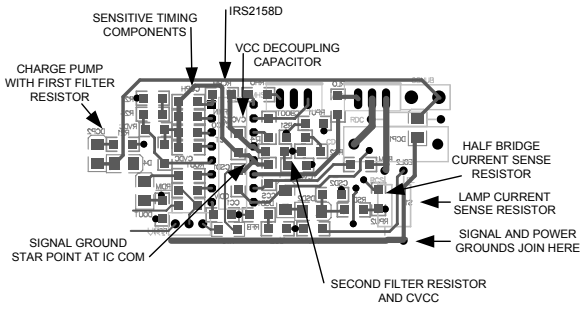


Figure 10: Critical traces on the bottom side of the PCB

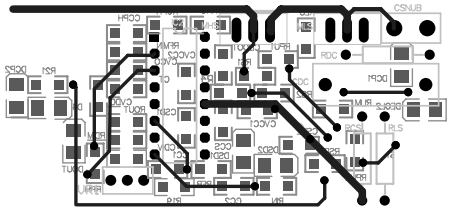
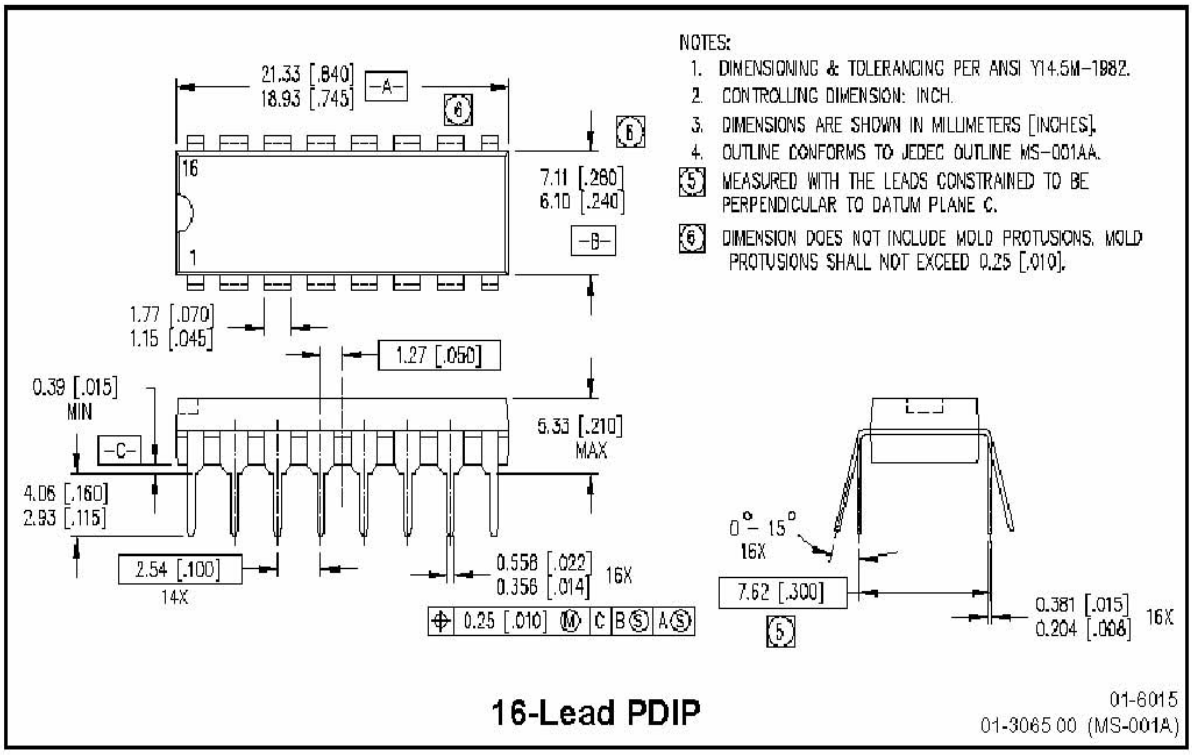
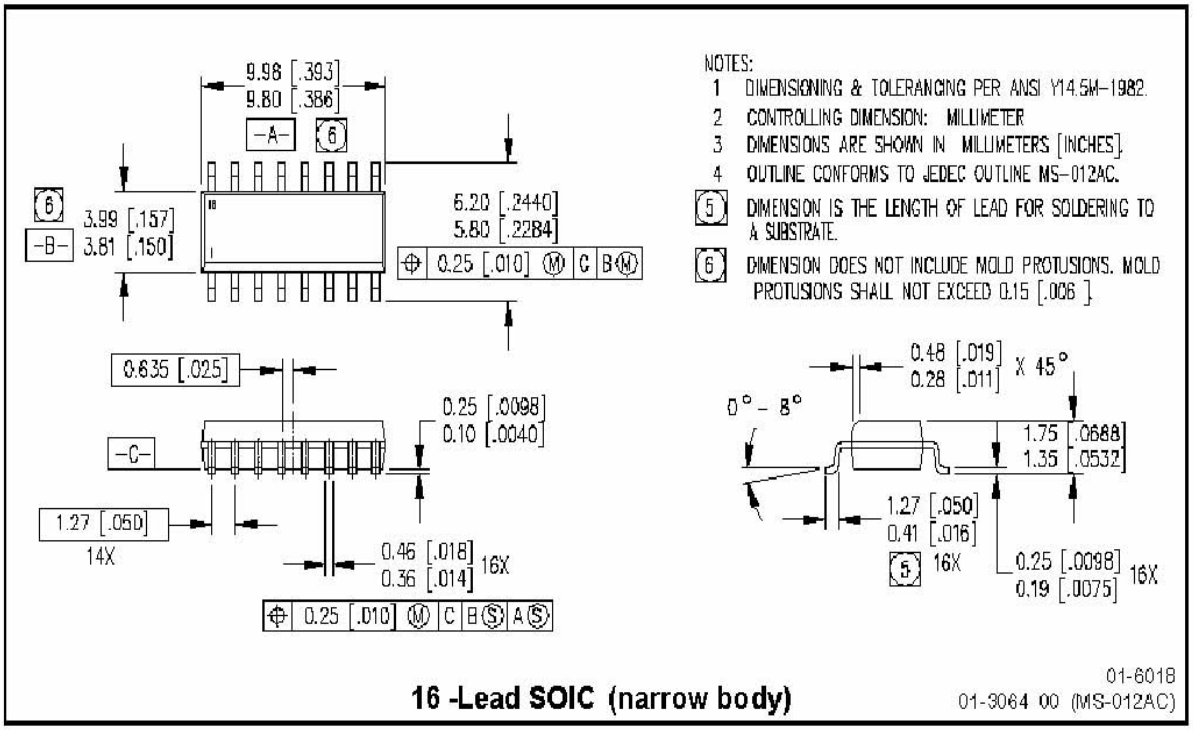


Figure 11: Critical traces on the top side of the PCB

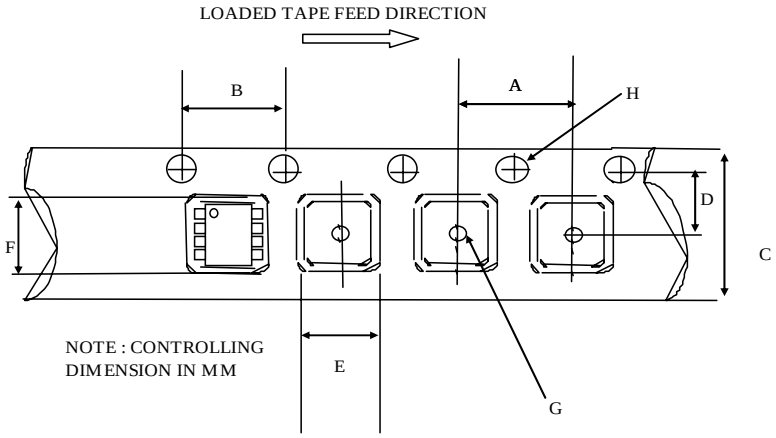
1) The signal ground (pin 12) should only be connected to the power ground at one single point to prevent ground loops from forming.
2) The point described in (1) should be where the grounds of the current sense resistors for both the half bridge MOSFETs and the lamp current feedback both meet.
3) The VCC decoupling capacitor should be placed as close to the IRS2158D VCC (pin 13) and COM (pin 12) as possible with the shortest possible traces.
4) The devices; CPH, RMIN, CVCO, CT and CCS should all be located as close to the IRS2158D as possible with traces to the relevant pins being as short as possible.
5) The ground connections from the devices listed in (4) should be connected back to the COM pin of the IRS2158D through the shortest possible traces. These should be connected back to the COM pin of the IC without joining the power ground trace at any point. In the example shown above the power ground trace runs along the lower side of the board on the bottom Copper layer
6) The charge pump diode connection to ground should be made to the power ground not the signal ground.
7) The power factor correction section (if used) should be kept apart from the ballast control as shown in the example above. the power factor correction section is at the left side of the PCB.

Package Details: PDIP16 and SOIC16N



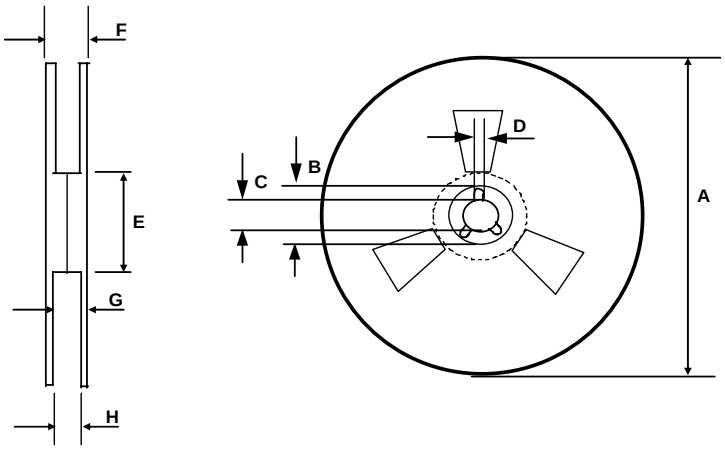


Package Details: SOIC16N, Tape and Reel



CARRIER TAPE DIMENSION FOR 16SOICN

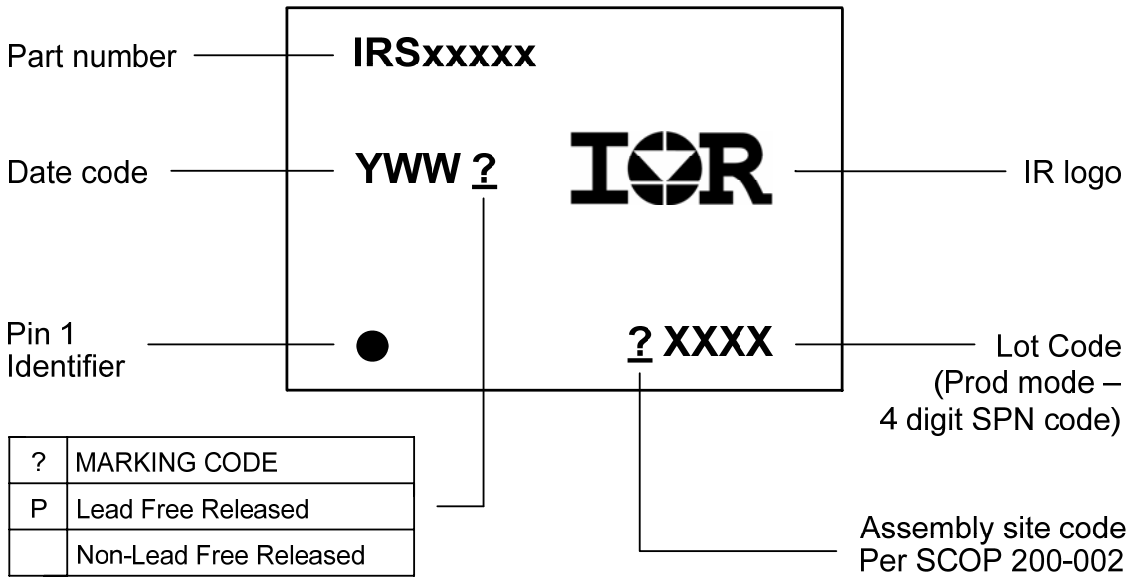
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	6.40	6.60	0.252	0.260
F	10.20	10.40	0.402	0.409
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 16SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
H	16.40	18.40	0.645	0.724

Part Marking Information



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

Ordering information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IRS2158D	PDIP16	Tube/Bulk	25	IRS2158DPBF
	SOIC16N	Tube/Bulk	45	IRS2158DSPBF
		Tape and Reel	2500	IRS2158DSTRPBF

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