

#### **AUTOMOTIVE GRADE**

# AUIRFR1018E

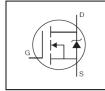
HEXFET® Power MOSFET

#### **Features**

- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Timax

fast switching speed and improved repetitive avalanche rating .

- Lead-Free, RoHS Compliant
- Automotive Qualified \*



V <sub>DSS</sub>		60V
R <sub>DS(on)</sub>	typ.	7.1m $\Omega$
	max.	8.4m $\Omega$
ID (Silicon Lim	nited)	79A①
I <sub>D (Package Li</sub>	imited)	56A

# Description Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to D-Pak achieve extremely low on-resistance per silicon area. Additional AUIRFR1018E features of this design are a 175°C junction operating temperature,

These features combine to make this design an extremely efficient	G	D	S
and reliable device for use in Automotive applications and a wide	0-4-	D	0
variety of other applications.	Gate	Drain	Source

Page part number	Paakaga Typa	Standard Pack		Orderable Part Number
Base part number	Package Type	Form	Quantity	Orderable Part Nulliber
ALUDED1010E	D. Dok	Tube	75	AUIRFR1018E
AUIRFR1018E	D-Pak	Tape and Reel Left	3000	AUIRFR1018ETRL

# **Absolute Maximum Ratings**

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Silicon Limited)	79①	
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Silicon Limited)	56①	
$I_D$ @ $T_C$ = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Package Limited)	56	A
I <sub>DM</sub>	Pulsed Drain Current ②	315	
P <sub>D</sub> @T <sub>C</sub> = 25°C	Maximum Power Dissipation	110	W
	Linear Derating Factor	0.76	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 20	V
E <sub>AS</sub>	Single Pulse Avalanche Energy (Thermally Limited) ③	88	mJ
I <sub>AR</sub>	Avalanche Current ②	47	Α
E <sub>AR</sub>	Repetitive Avalanche Energy ②	11	mJ
dv/dt	Pead Diode Recovery dv/dt⊕	21	V/ns
$T_J$	Operating Junction and	-55 to + 175	
T <sub>STG</sub>	Storage Temperature Range		°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

#### Thermal Resistance

Symbol	Symbol Parameter		Max.	Units
$R_{\theta JC}$	Junction-to-Case		1.32	
$R_{\theta JA}$	Junction-to-Ambient ( PCB Mount) ®		50	°C/W
$R_{\theta JA}$	Junction-to-Ambient ®		110	

HEXFET® is a registered trademark of Infineon.

2015-11-19

<sup>\*</sup>Qualification standards can be found at www.infineon.com



# Static @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Тур.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60			V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient		0.073		V/°C	Reference to 25°C, I <sub>D</sub> = 5mA ②
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance		7.1	8.4	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 47A ⑤
$V_{GS(th)}$	Gate Threshold Voltage	2.0		4.0	V	$V_{DS} = V_{GS}$ , $I_D = 100 \mu A$
gfs	Forward Trans conductance	110			S	$V_{DS} = 50V, I_{D} = 47A$
$R_{G(Int)}$	Internal Gate Resistance		0.73		Ω	
ı	Drain-to-Source Leakage Current			20	μA	$V_{DS} = 60V, V_{GS} = 0V$ $V_{DS} = 48V, V_{GS} = 0V, T_{J} = 125^{\circ}C$
I <sub>DSS</sub>	Diam-to-Source Leakage Current	_		250	μΑ	$V_{DS} = 48V, V_{GS} = 0V, T_{J} = 125^{\circ}C$
	Gate-to-Source Forward Leakage			100	nA	$V_{GS} = 20V$
I <sub>GSS</sub>	Gate-to-Source Reverse Leakage			-100	ПА	$V_{GS} = -20V$

## Dynamic Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

•	•	•	•		
$Q_g$	Total Gate Charge	 46	69		I <sub>D</sub> = 47A
$Q_{gs}$	Gate-to-Source Charge	 10		nC	$V_{DS} = 30V$
$\overline{Q_gd}$	Gate-to-Drain Charge	 12		110	V <sub>GS</sub> = 10V <sup>⑤</sup>
Q <sub>sync</sub>	Total Gate Charge Sync. (Q <sub>g</sub> - Q <sub>gd</sub> )	 34			
$t_{d(on)}$	Turn-On Delay Time	 13			V <sub>DD</sub> = 39V
t <sub>r</sub>	Rise Time	 35		200	$I_D = 47A$
$t_{d(off)}$	Turn-Off Delay Time	 55		ns	$R_G = 10\Omega$
t <sub>f</sub>	Fall Time	 46			V <sub>GS</sub> = 10V <sup>⑤</sup>
C <sub>iss</sub>	Input Capacitance	 2290			$V_{GS} = 0V$
Coss	Output Capacitance	 270			$V_{DS} = 50V$
$C_{rss}$	Reverse Transfer Capacitance	 130		pF	f = 1.0 MHz
C <sub>oss eff.</sub> (ER)	Effective Output Capacitance (Energy Related)	 390			$V_{GS} = 0V$ , $V_{DS} = 0V$ to 48V $\bigcirc$
C <sub>oss eff.</sub> (TR)	Effective Output Capacitance (Time Related)	 630			$V_{GS} = 0V, V_{DS} = 0V \text{ to } 48V $

#### **Diode Characteristics**

Diode 0	Stode Characteristics						
	Parameter	Min.	Typ.	Max.	Units	C	onditions
I <sub>S</sub>	Continuous Source Current (Body Diode)			<b>79</b> ①		MOSFET syr showing the	( ) )
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①			315		integral rever p-n junction o	rse 🔍
$V_{SD}$	Diode Forward Voltage			1.3	V	$T_J = 25^{\circ}C, I_S =$	= 47A,V <sub>GS</sub> = 0V ⑤
t <sub>rr</sub>	Reverse Recovery Time		26	39		T <sub>J</sub> = 25°C	
			31	47	ns	T <sub>J</sub> = 125°C	$V_{R} = 51V$ ,
$Q_{rr}$	Reverse Recovery Charge		24	36	nC	T <sub>J</sub> = 25°C	I <sub>F</sub> = 47A
			35	53	IIC	T <sub>J</sub> = 125°C	di/dt = 100A/µs ⑤
			1.8		Α	$T_J = 25^{\circ}C$	-
t <sub>on</sub>	Forward Turn-On Time	Intrinsio	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

#### Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 56A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- 3 Limited by  $T_{Jmax}$ , starting  $T_J = 25$ °C, L = 0.08mH,  $R_G = 25\Omega$ ,  $I_{AS} = 47$ A,  $V_{GS} = 10$ V. Part not recommended for use above this value.
- ⑤ Pulse width  $\leq 400\mu s$ ; duty cycle  $\leq 2\%$ .
- © C<sub>oss eff.</sub> (TR) is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- $\odot$  C<sub>oss eff</sub>. (ER) is a fixed capacitance that gives the same energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994
- 9  $R_{\theta}$  is measured at  $T_{J}$  approximately 90°C.



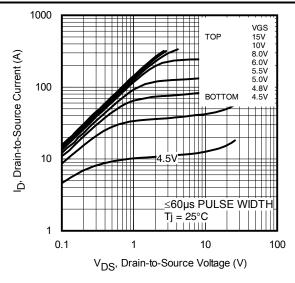


Fig. 1 Typical Output Characteristics

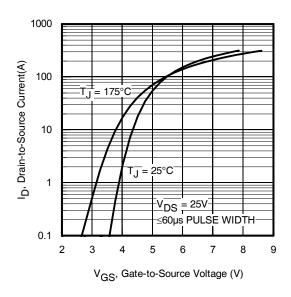


Fig. 3 Typical Transfer Characteristics

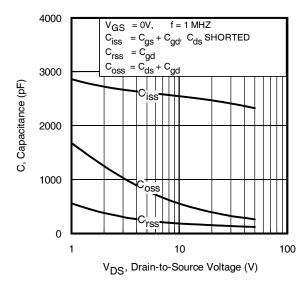


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

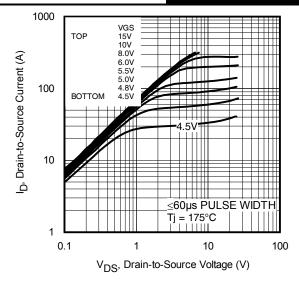


Fig. 2 Typical Output Characteristics

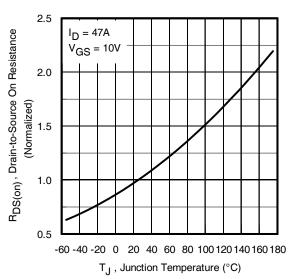


Fig. 4 Normalized On-Resistance vs. Temperature

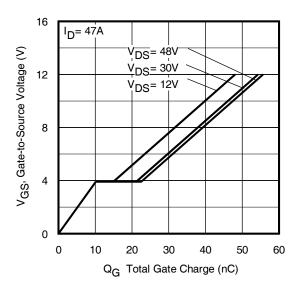
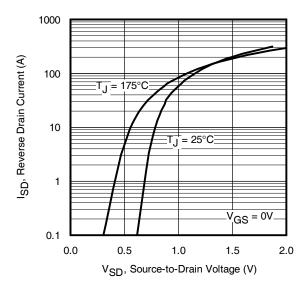


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage





10000

OPERATION IN THIS AREA

LIMITED BY RIDS(on)

100

LIMITED BY PACKAGE

100

TC = 25°C

Tj = 175°C

Single Pulse

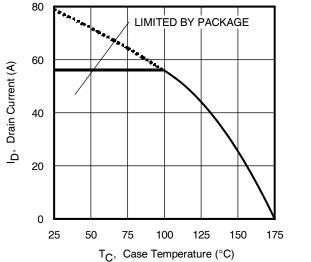
0.1

0.1

1 1 10 100

VDS, Drain-toSource Voltage (V)

Fig. 7 Typical Source-to-Drain Diode Forward Voltage



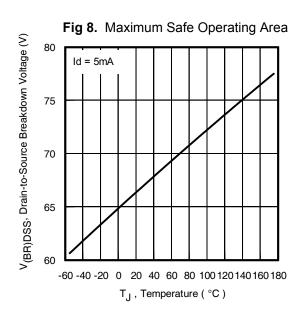


Fig. 9 Maximum Drain Current vs. Case Temperature

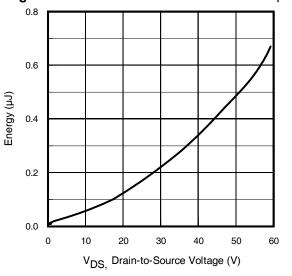


Fig 10. Drain-to-Source Breakdown Voltage

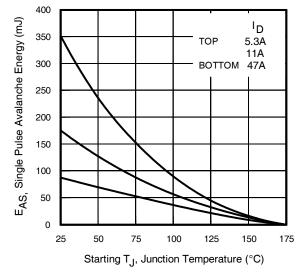


Fig. 11 Typical Coss Stored Energy

Fig 12. Maximum Avalanche Energy vs. Drain Current

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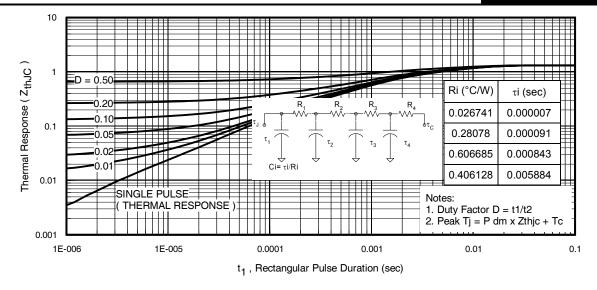


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

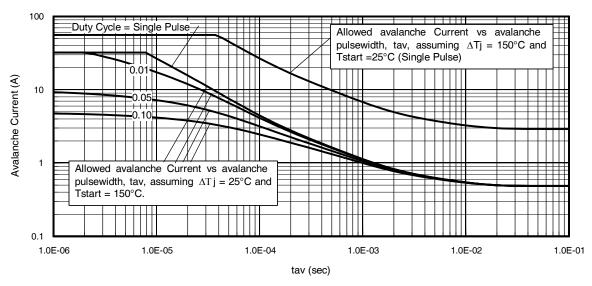


Fig 14. Typical Avalanche Current Vs. Pulse width

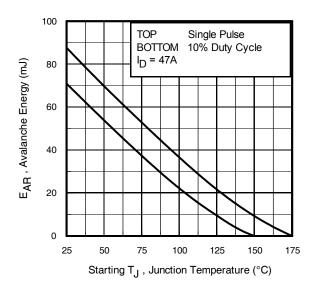


Fig 15. Maximum Avalanche Energy Vs. Temperature

# Notes on Repetitive Avalanche Curves, Figures 14, 15: (For further info, see AN-1005 at www.infineon.com)

- Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T<sub>jmax</sub>. This is validated for every part type.
- 2. Safe operation in Avalanche is allowed as long as Tjmax is not exceeded.
- 3. Equation below based on circuit and waveforms shown in Figures 22a, 22b.
- 4. PD (ave) = Average power dissipation per single avalanche pulse.
- BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
- 6. lav = Allowable avalanche current.
- 7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 13, 14).

tav = Average time in avalanche.

D = Duty cycle in avalanche = tav ·f

ZthJC(D, tav) = Transient thermal resistance, see Figures 13)

$$\begin{split} P_{D \text{ (ave)}} &= 1/2 \text{ ( } 1.3 \cdot \text{BV} \cdot \text{I}_{av} \text{)} = \Delta \text{T} / \text{Z}_{thJC} \\ I_{av} &= 2\Delta \text{T} / \text{ [ } 1.3 \cdot \text{BV} \cdot \text{Z}_{th} \text{]} \\ E_{AS \text{ (AR)}} &= P_{D \text{ (ave)}} \cdot t_{av} \end{split}$$



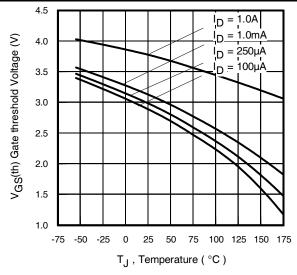


Fig 16. Threshold Voltage vs. Temperature

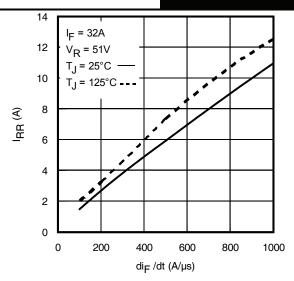
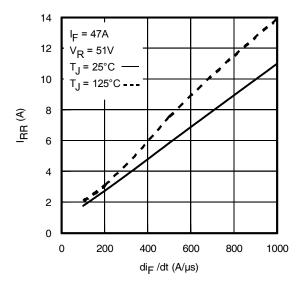


Fig. 17 - Typical Recovery Current vs. dif/dt



 $I_{F} = 32A$ 280 V<sub>R</sub> = 51V  $T_J = 25^{\circ}C$ 240 T<sub>J</sub> = 125°C --200 Q<sub>RR</sub> (nC) 160 120 80 40 0 200 400 600 800 1000 0 di<sub>F</sub> /dt (A/µs)

320

Fig. 18 - Typical Recovery Current vs. dif/dt

Fig. 19 - Typical Stored Charge vs. dif/dt

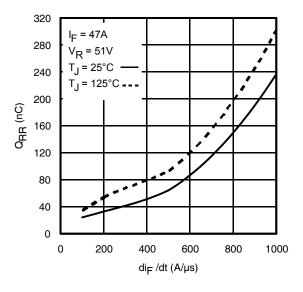


Fig. 20 - Typical Stored Charge vs. dif/dt



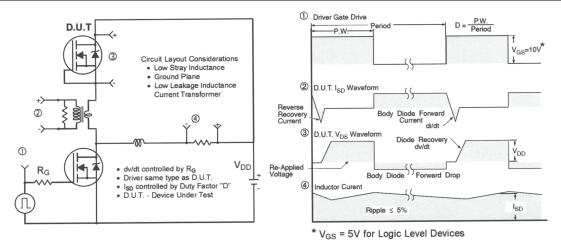


Fig 20. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

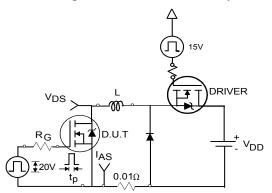


Fig 21a. Unclamped Inductive Test Circuit

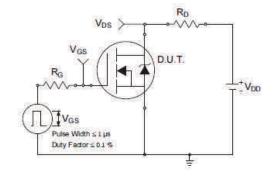


Fig 22a. Switching Time Test Circuit

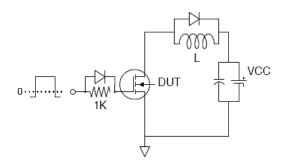


Fig 23a. Gate Charge Test Circuit

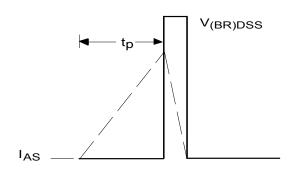


Fig 21b. Unclamped Inductive Waveforms

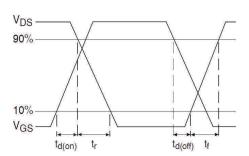


Fig 22b. Switching Time Waveforms

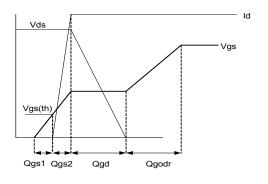
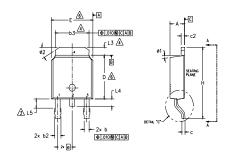


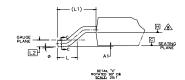
Fig 23b. Gate Charge Waveform

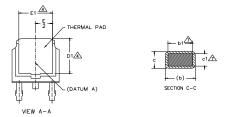


# D-Pak (TO-252AA) Package Outline (Dimensions are shown in millimeters (inches))









#### NOTES:

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].
- 1 LEAD DIMENSION UNCONTROLLED IN L5.
- A- DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.— SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
- bildension D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- A- DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
- ♠ DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

S		N			
M B O	MILLIM	ETERS	INC	HES	O T
O L	MIN.	MAX.	MIN.	MAX.	E S
Α	2.18	2.39	.086	.094	
A1	-	0.13	-	.005	
b	0.64	0.89	.025	.035	
ь1	0.65	0.79	.025	.031	7
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	4
С	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	7
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	-	.205	-	4
Ε	6.35	6.73	.250	.265	6
E1	4.32	-	.170	-	4
е	2.29	BSC	.090 BSC		
Н	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74	2.74 BSC		REF.	
L2	0.51	BSC	.020	BSC	
L3	0.89	1.27	.035	.050	4
L4	-	1.02	-	.040	
L5	1.14	1.52	.045	.060	3
ø	0,	10*	0,	10°	
ø1	0.	15*	0,	15*	
ø2	25*	35*	25*	35*	

#### LEAD ASSIGNMENTS

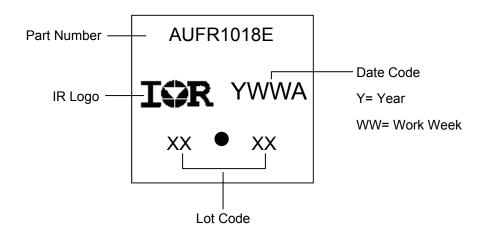
## **HEXFET**

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

#### IGBT & CoPAK

- 1.- GATE
- 2.- COLLECTOR 3.- EMITTER
- 4. COLLECTOR

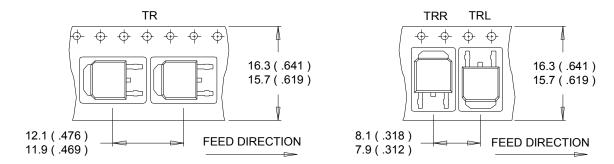
## D-Pak (TO-252AA) Part Marking Information



Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

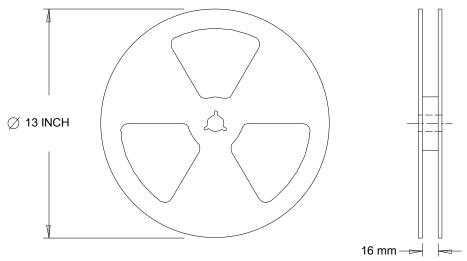


# D-Pak (TO-252AA) Tape & Reel Information (Dimensions are shown in millimeters (inches))



#### NOTES:

- 1. CONTROLLING DIMENSION: MILLIMETER.
- 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
- 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



### NOTES:

1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawing please refer to IR website at <a href="http://www.irf.com/package/">http://www.irf.com/package/</a>



#### **Qualification Information**

			Automotive			
		(per AEC-Q101)				
Qualificat	ion Level	Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.				
Moisture	Sensitivity Level	D-Pak	MSL1			
			Class M4 (+/- 600V) <sup>†</sup>			
	Machine Model	AEC-Q101-002				
FOD	Lluman Dady Madal	Class H1C (+/- 1500V) <sup>†</sup>				
ESD	Human Body Model	AEC-Q101-001				
	Clearned Davise Medal	Class C4 (+/- 1000V) <sup>†</sup>				
Charged Device Model		AEC-Q101-005				
RoHS Compliant		Yes				

<sup>†</sup> Highest passing voltage.

### **Revision History**

Date	Comments				
	Updated datasheet with corporate template				
11/19/2015	Corrected ordering table on page 1.				
11/19/2015	<ul> <li>Corrected typo on test condition Coss eff. V<sub>DS</sub> from "60V" to "48V" on page 2.</li> </ul>				
	<ul> <li>Updated typo on the fig.19 and fig.20, unit of y-axis from "A" to "nC" on page 6.</li> </ul>				

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