TVS Diodes

Transient Voltage Suppressor Diodes

TVS3V3L4U

Low Capacitance ESD / Transient / Surge Protection Array

TVS3V3L4U

Data Sheet

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4	Halogen free deleted

1 Low Capacitance ESD / Transient / Surge Protection Array

1.1 Features

- ESD/Transient/Surge protection according to:
  IEC61000-4-2 (ESD): ±30 kV air/contact discharge
  IEC61000-4-4 (EFT): ±80 A (5/50 ns)
  IEC61000-4-5 (Surge): ±20 A (8/20 µs)
- Reverse working voltage maximum: V_{RWM} = 3.3 V
- Low leakage current: I_R < 50 nA
- **Low capacitance: C_L = 2 pF typ. (I/O to GND), 1 pF typ. (I/O to I/O)**
- Low clamping voltage: V_{CL} = 7.7 V typ. @ 20 A (8/20 µs)
- Pb-free (RoHS compliant) package

RoHS

1.2 Application Examples

- 10/100/1000 Ethernet
- 4 lines uni-directional (Pin 2 to GND)
- 2 lines bi-directional (Pin 2 n.c.)

1.3 Product Description

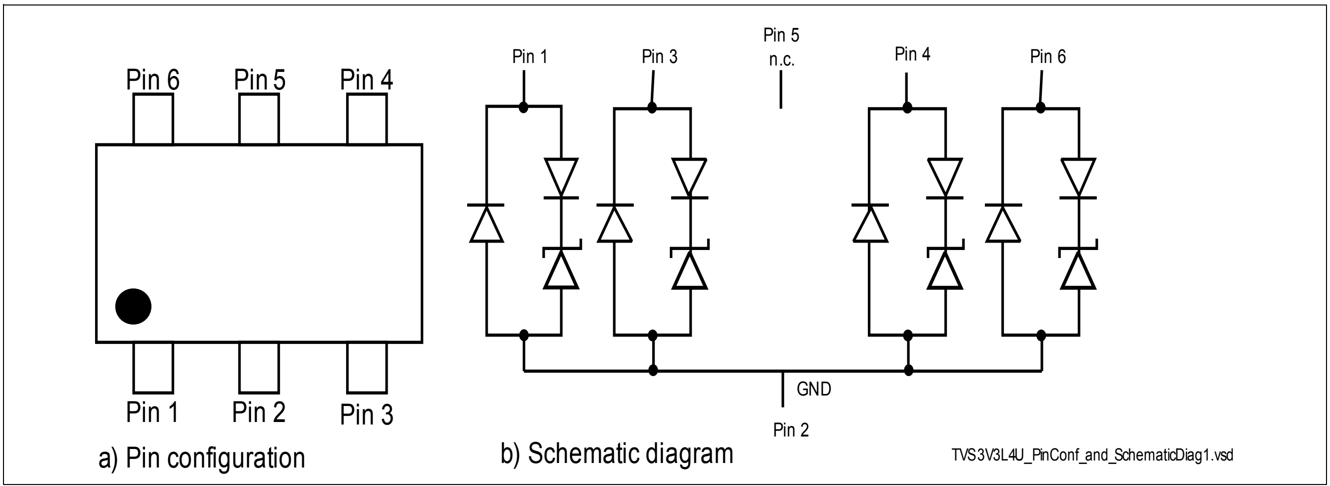

Figure 1-1 Pin configuration and Schematic diagram

Table 1-1 Ordering Information

Type	Package	Configuration	Marking code
TVS3V3L4U	SC74	4 lines, uni-directional or 2 lines, bidirectional	E1s

2 Electrical Characteristics

2.1 Maximum Ratings

Table 2-1 Maximum Ratings at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
ESD discharge[1] air contact	V_{ESD}	 -30 -30	 – –	 30 30	kV
Peak pulse current (t_P = 8/20 µs)[2]	I_{PP}	-20	–	20	A
Peak pulse power t_P = 8/20 µs[2] t_P = 100 ns[3]	P_{PK}	 – –	 – –	 154 1044	W
Operating temperature	T_{OP}	-55	–	125	°C
Storage temperature	T_{stg}	-55	–	150	°C

1) V_{ESD} according to IEC61000-4-2
2) I_{PP} according to IEC61000-4-5. P_{PK} is calculated by I_{PP} x V_{CL}.
3) Please refer to AN210[1]. P_{PK} is calculated by I_{TLP} x V_{CL}.

***Attention:** Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.*

2.2 DC Characteristics

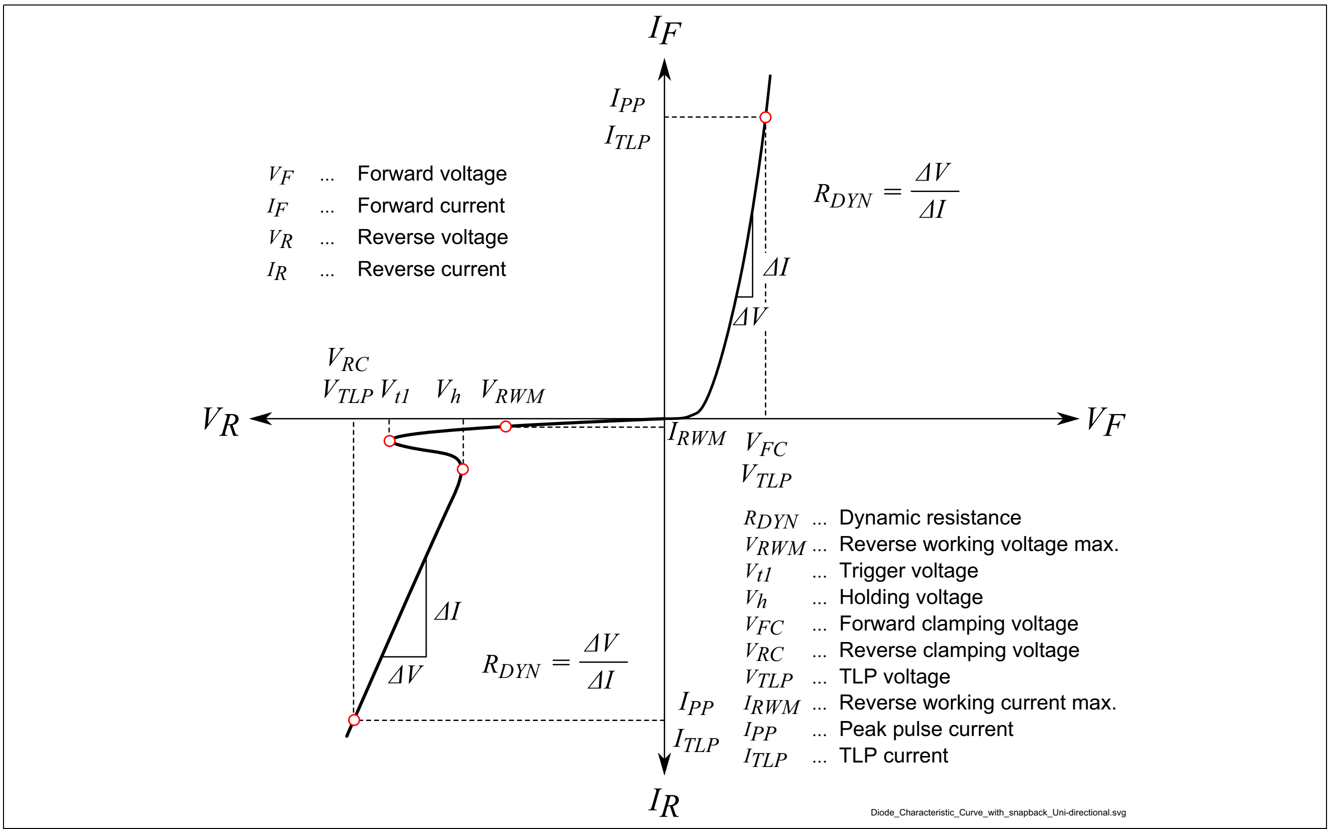

Figure 2-1 Definitions of electrical characteristics

Table 2-2 DC Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	**Symbol**	**Values**			**Unit**	**Note / Test Condition**
		Min.	**Typ.**	**Max.**		
Reverse working voltage	V_{RWM}	–	–	3.3	V	
Reverse current	I_R	–	–	50	nA	V_R = 3.3 V

2.3 RF Characteristics

Table 2-3 RF Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	**Symbol**	**Values**			**Unit**	**Note / Test Condition**
		Min.	**Typ.**	**Max.**		
Line capacitance	C_L				pF	V_R = 0 V, f = 1 MHz
I/O to GND		–	2	3		
I/O to I/O		–	1	–		

2.4 ESD Characteristics

Table 2-4 ESD Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse clamping voltage[1)]	V_{CL}				V	t_p = 8/20 µs
I/O to GND		–	4.2	–		I_{PP} = 1 A
I/O to GND		–	4.9	–		I_{PP} = 5 A
I/O to GND		–	5.8	–		I_{PP} = 10 A
I/O to GND		–	6.7	–		I_{PP} = 15 A
I/O to GND		–	7.7	–		I_{PP} = 20 A
Reverse clamping voltage[2)]						t_p = 100 ns
I/O to GND		–	5.8	–		I_{PP} = 16 A_{PP}
Forward clamping voltage[1)]	V_{FC}				V	t_p = 8/20 µs
GND to I/O		–	1.1	–		I_{PP} = 1 A
GND to I/O		–	4	–		I_{PP} = 20 A
Forward clamping voltage[2)]						t_p = 100 ns
GND to I/O		–	3.1	–		I_{PP} = 16 A
Dynamic resistance[1)]	R_{DYN}				Ω	
I/O to GND		–	0.15	–		t_p = 8/20 µs
Dynamic restiance[2)]						
I/O to GND		–	0.09	–		t_p = 100 ns

1) I_{PP} according to IEC61000-4-5

2) Please refer to Application Note AN210 [1]. TLP parameter: Z_0 = 50 Ω, t_p = 100ns, t_r = 300ps, averaging window: t_1 = 30 ns to t_2 = 60 ns, extraction of dynamic resistance using least squares fit of TLP characteristics between I_{PP1} = 10 A and I_{PP2} = 40 A.

3 Typical Characteristic

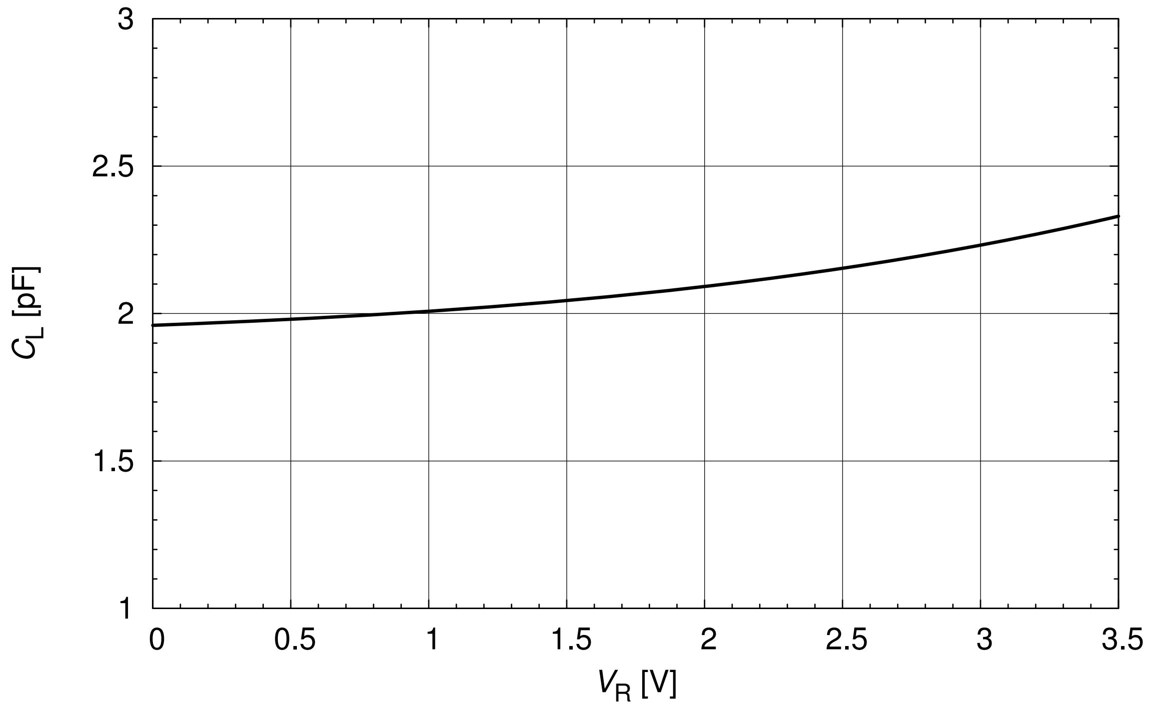

Figure 3-1 Line capacitance $C_L = f(V_R)$

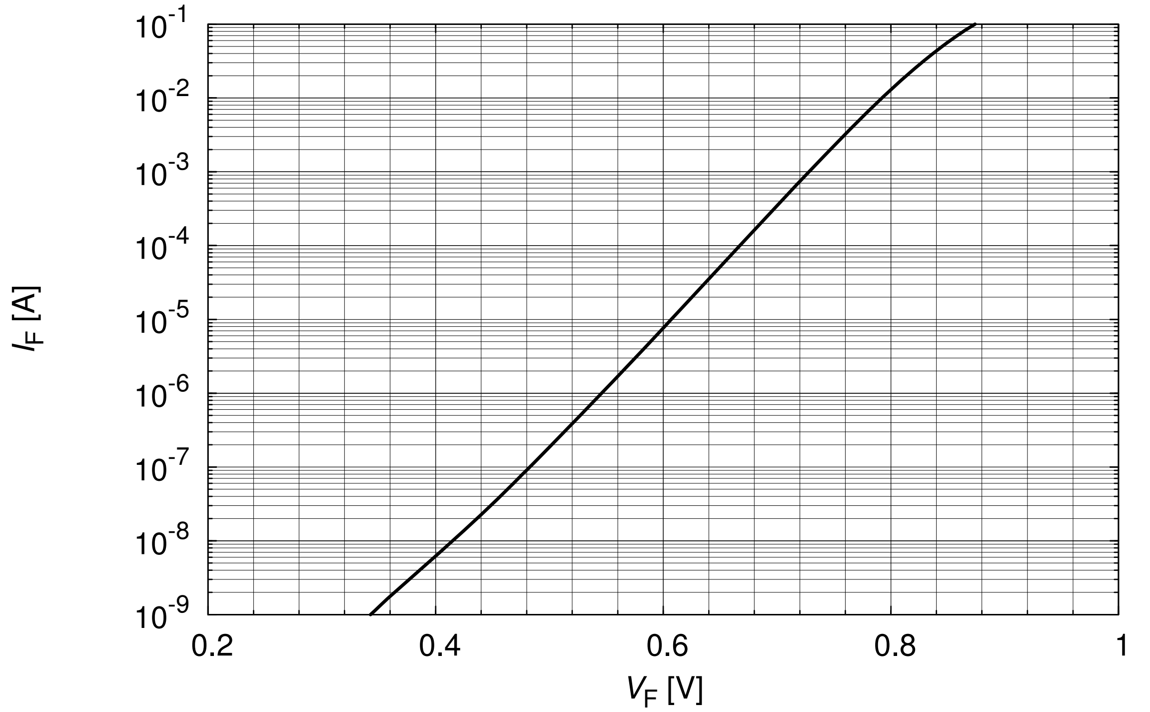

Figure 3-2 Forward characteristic, $I_F = f(V_F)$

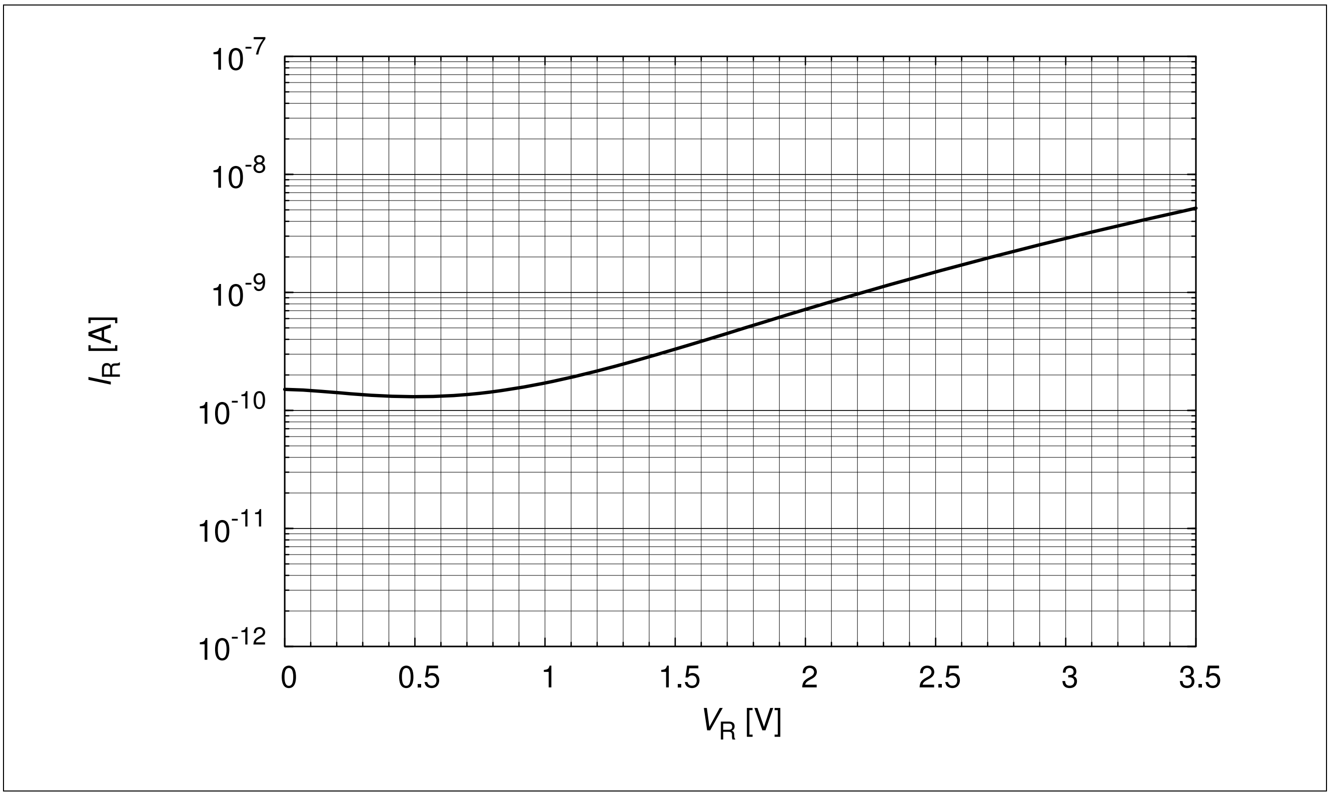

Figure 3-3 Reverse current, $I_R = f(V_R)$

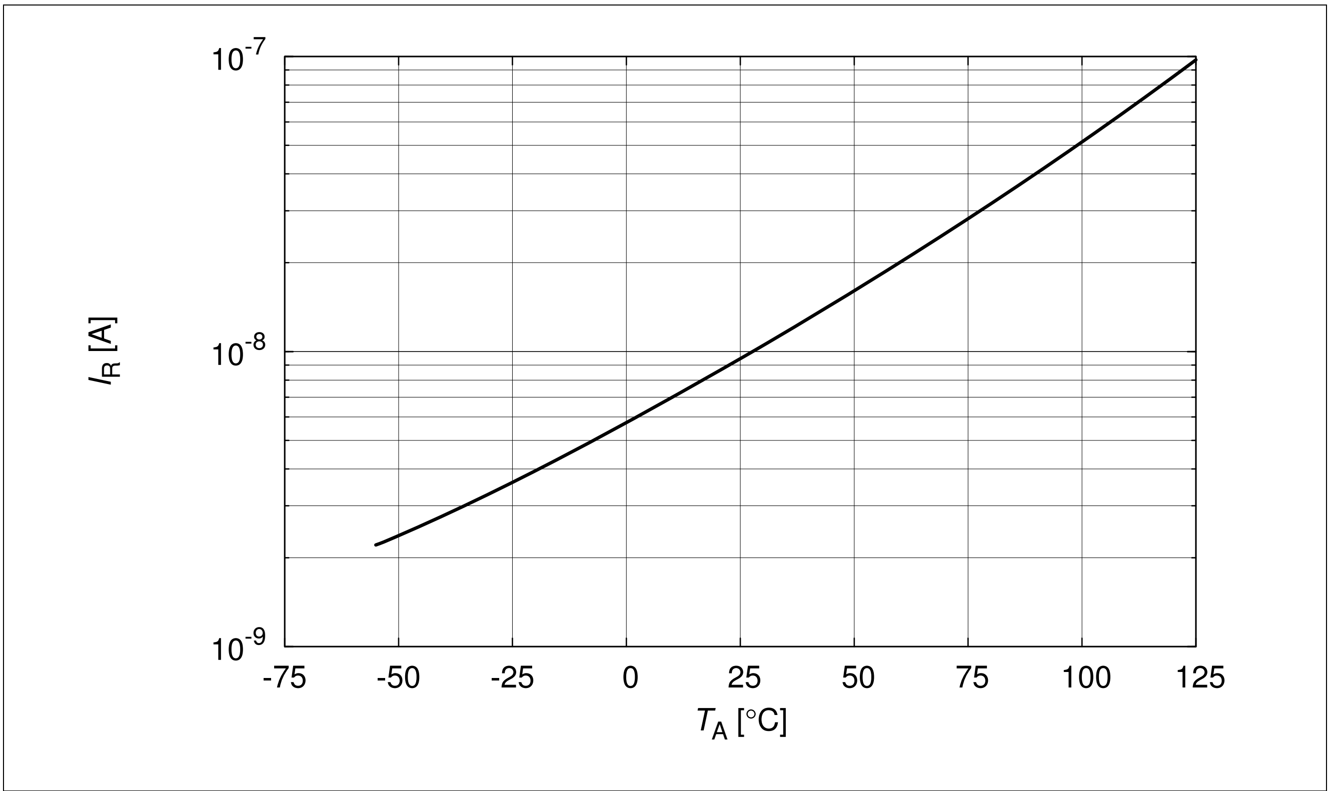

Figure 3-4 Reverse current $I_R = f(T_A)$, V_R = 3.3 V

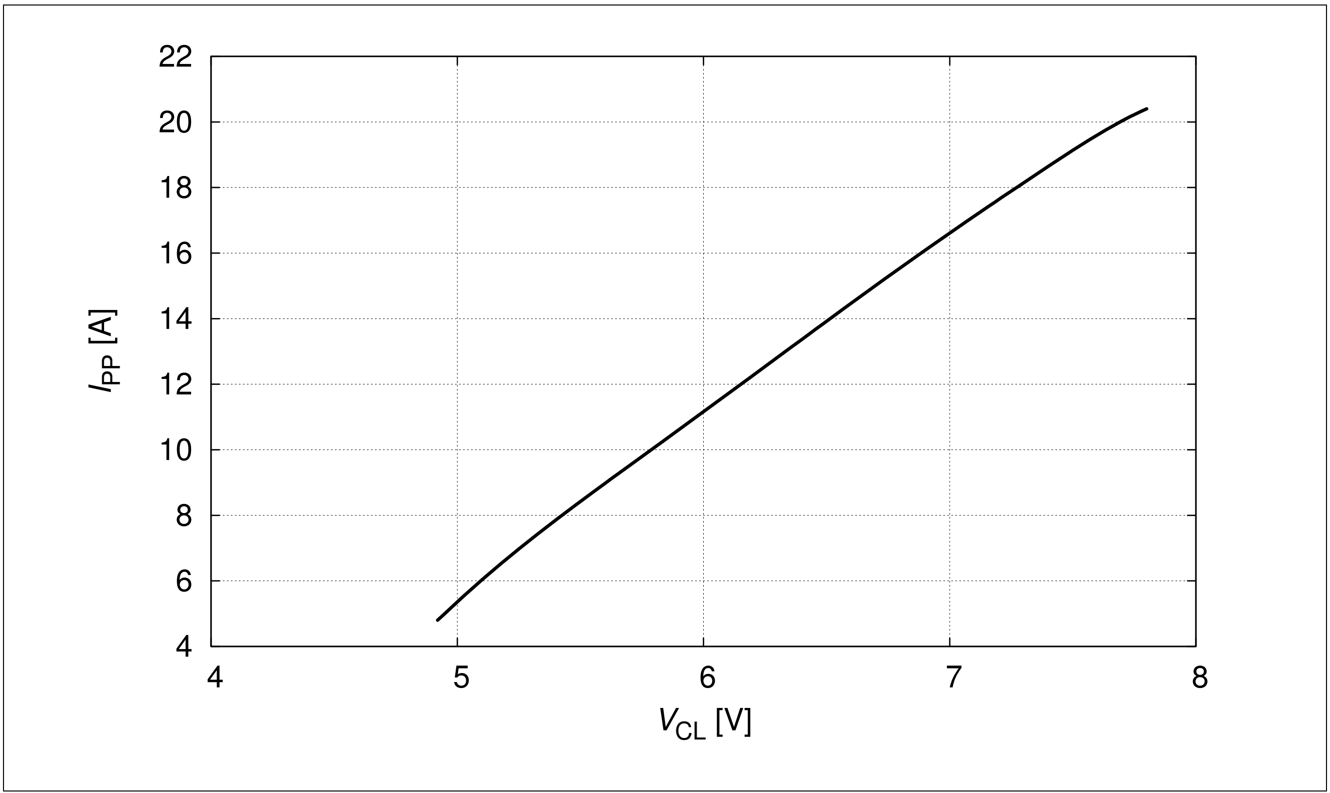

Figure 3-5 Pulse reverse current (IEC61000-4-5) versus clamping voltage, $I_{PP} = f(V_{CL})$

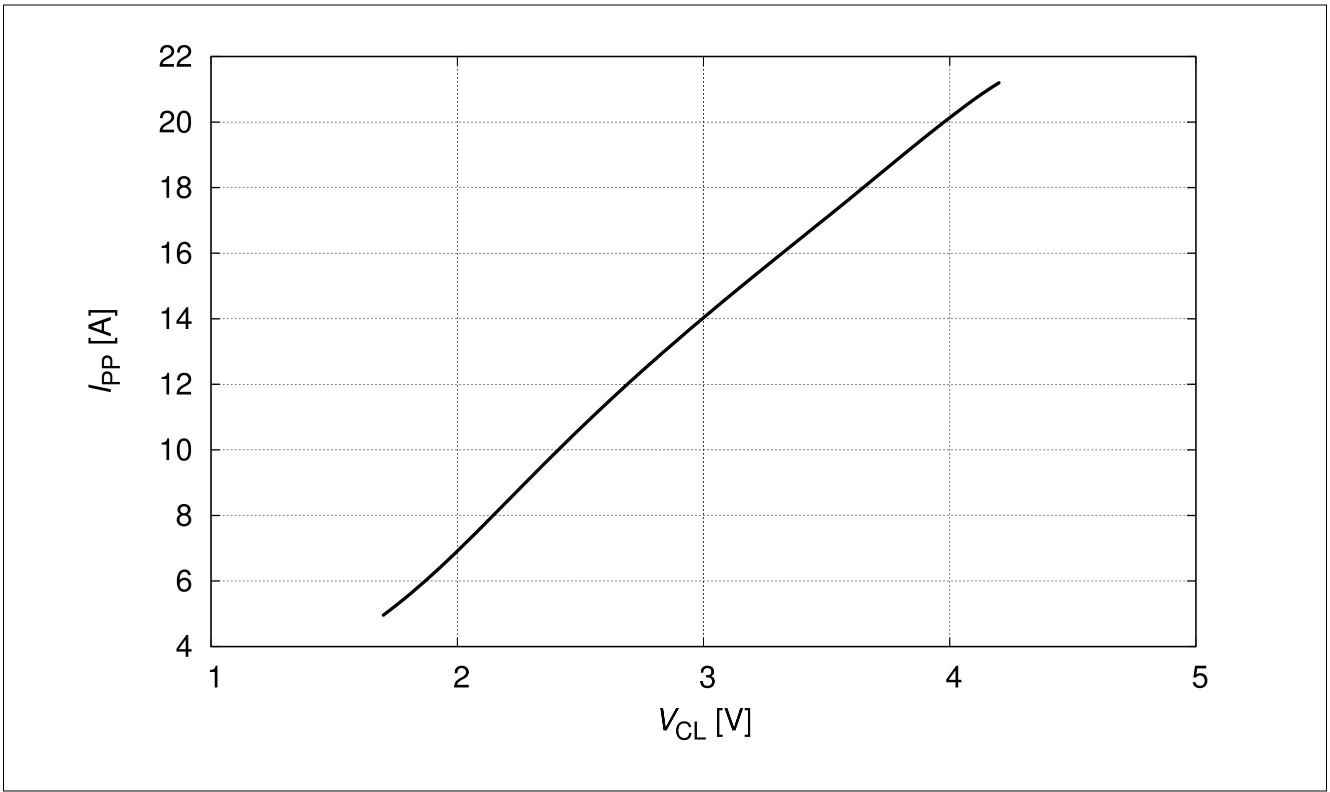

Figure 3-6 Pulse forward current (IEC61000-4-5) versus clamping voltage, $I_{PP} = f(V_{CL})$

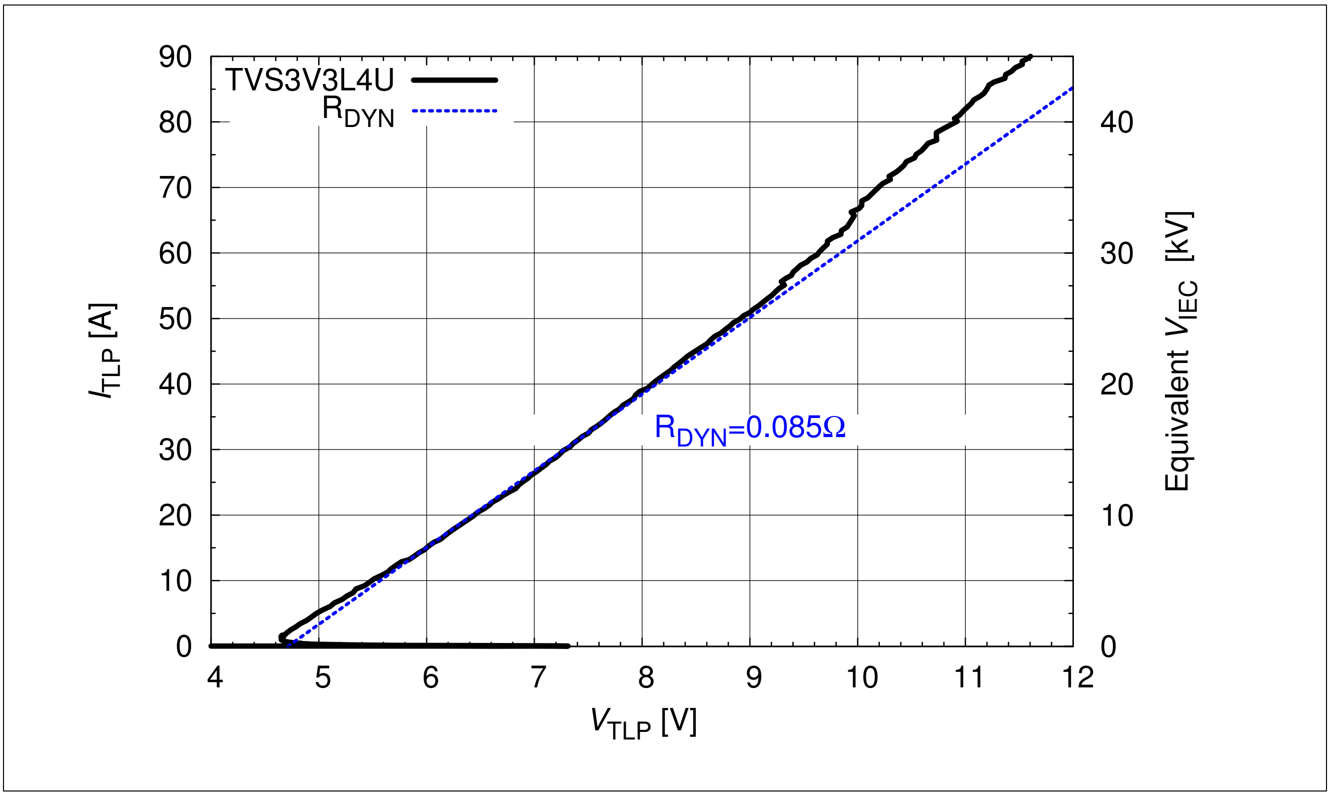

Figure 3-7 TLP characteristics, reverse pulse

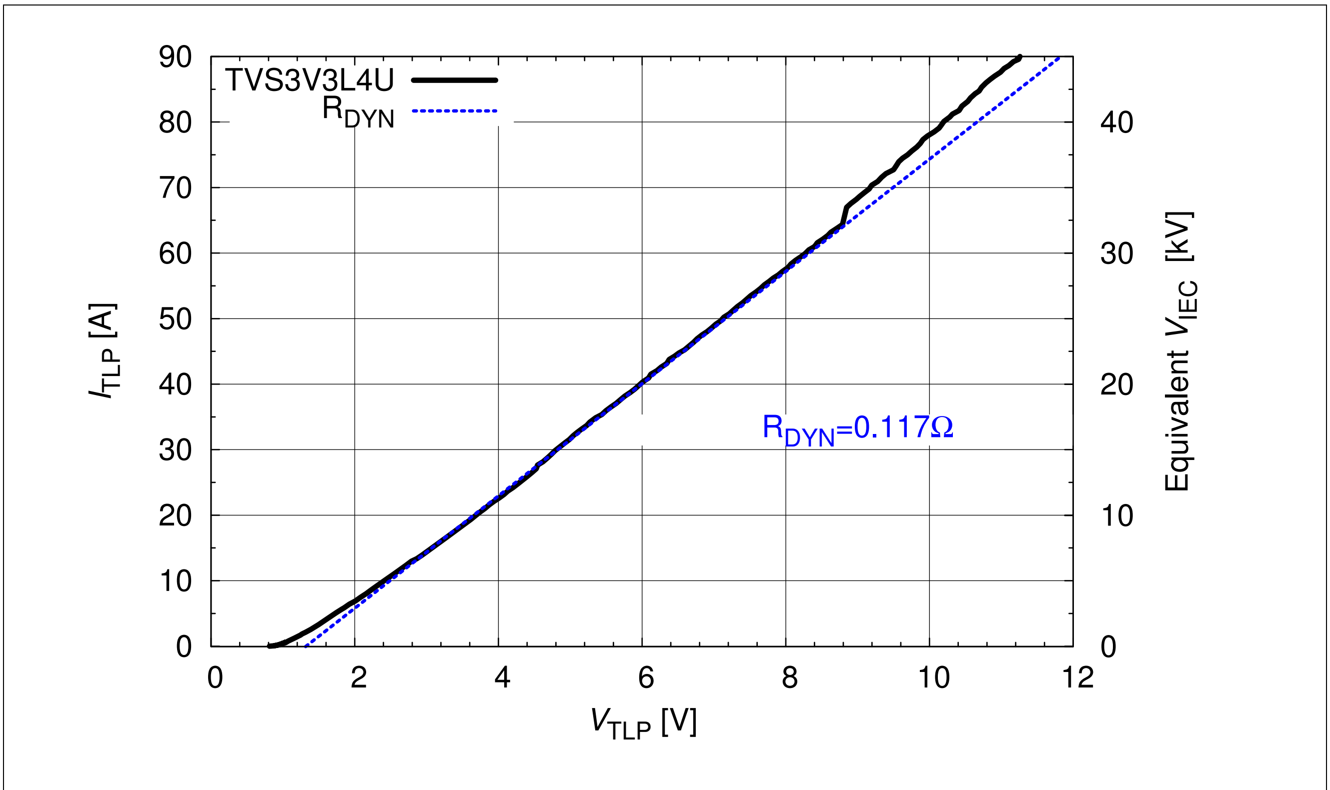

Figure 3-8 TLP characteristics, forward pulse

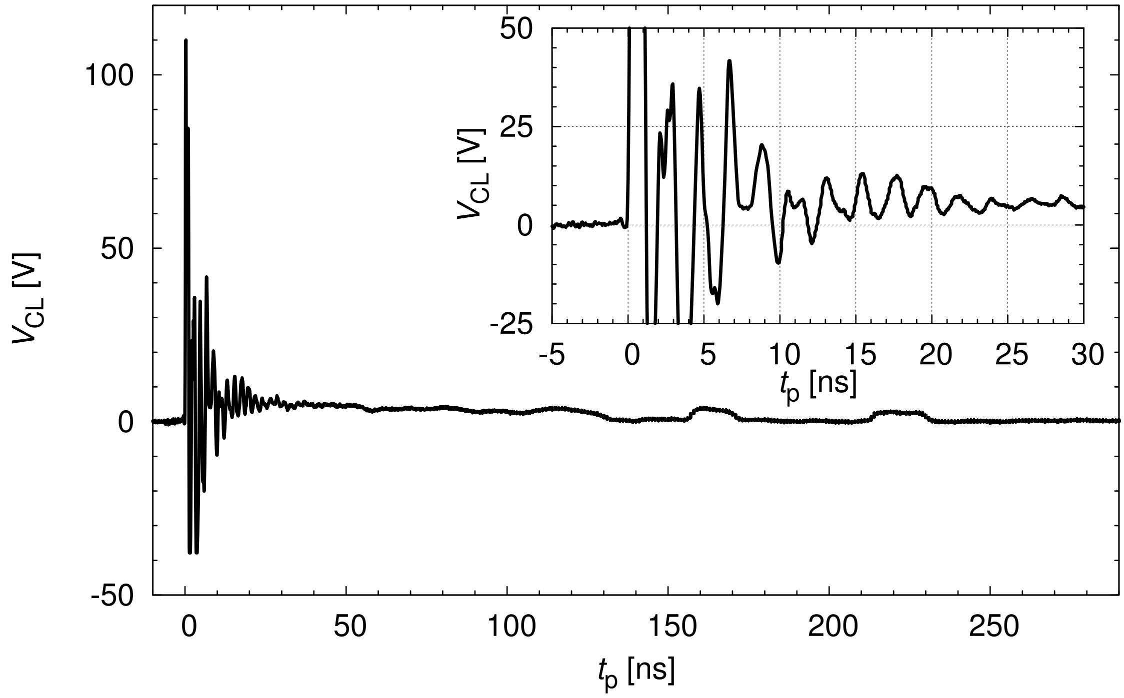

Figure 3-9 Clamping voltage at +8 kV contact discharge according IEC61000-4-2 (R = 330 Ω, C = 150 pF)

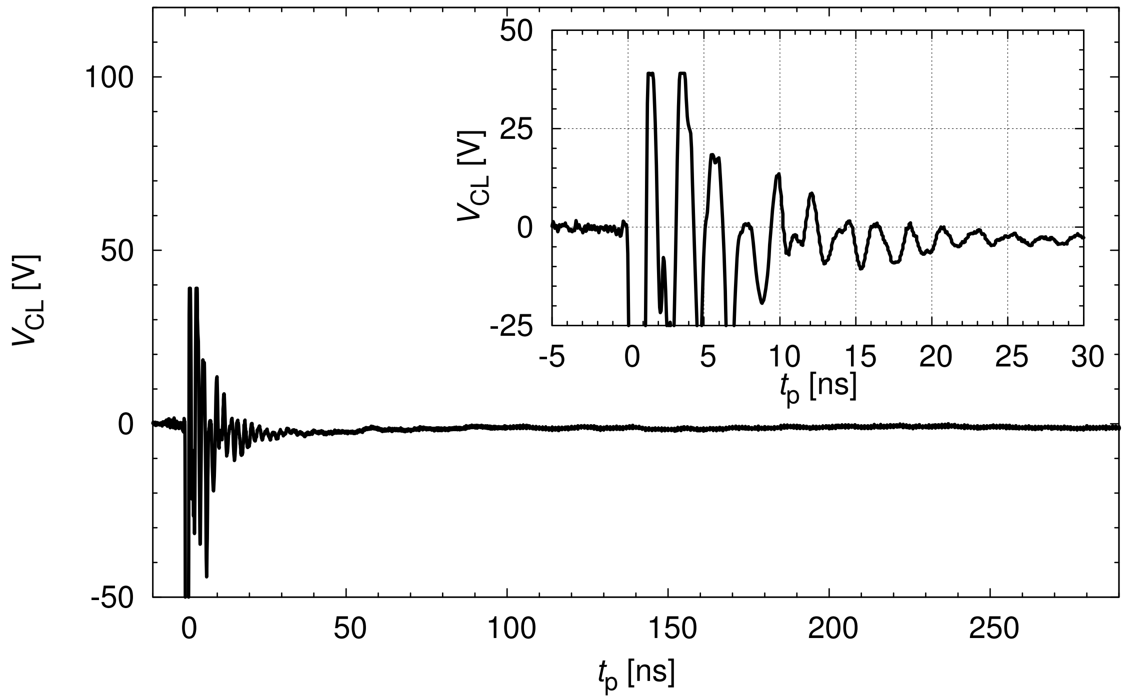

Figure 3-10 Clamping voltage at -8 kV contact discharge according IEC61000-4-2 (R = 330 Ω, C = 150 pF)

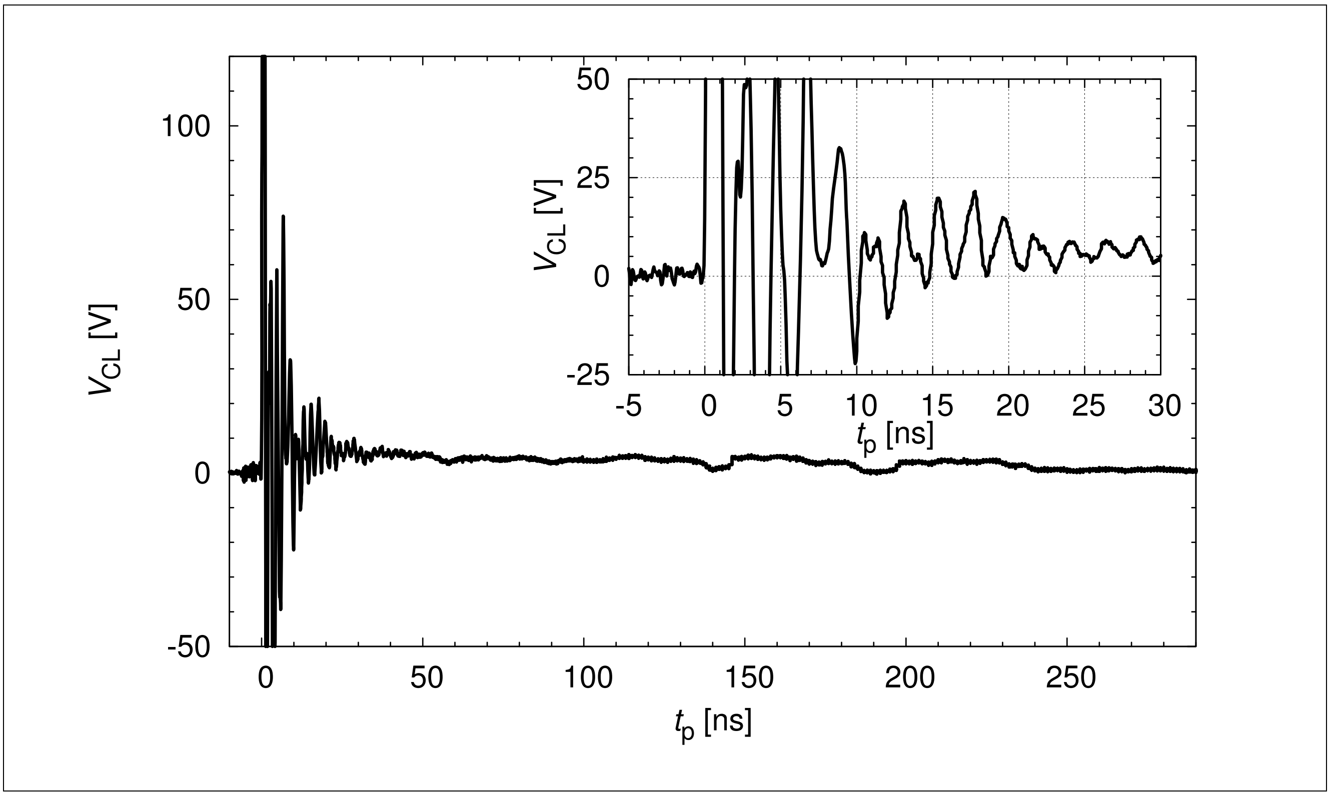

Figure 3-11 Clamping voltage at +15 kV contact discharge according IEC61000-4-2 (R = 330 Ω, C = 150 pF)

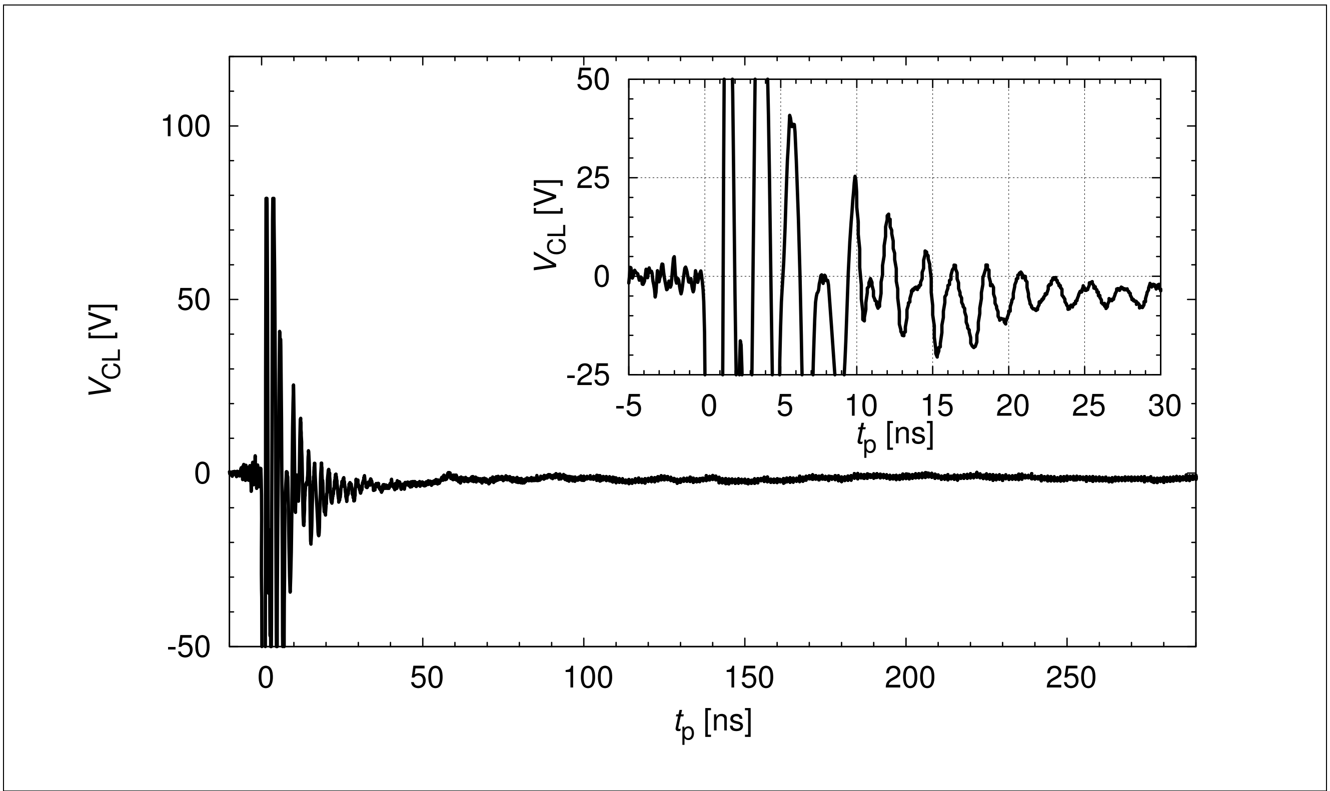

Figure 3-12 Clamping voltage at -15 kV contact discharge according IEC61000-4-2 (R = 330 Ω, C = 150 pF)

4 Package Information

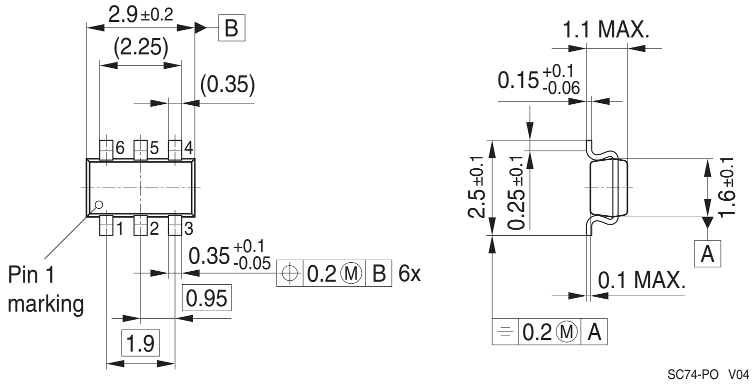

Figure 4-1 SC74 Package outline

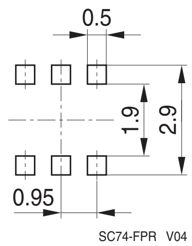

Figure 4-2 SC74 Footprint (Reflow Soldering)

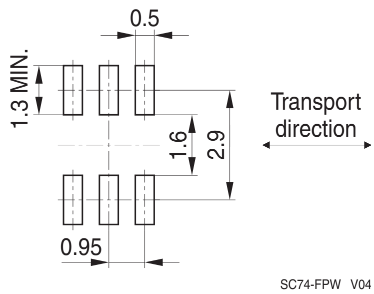

Figure 4-3 SC74 Footprint (Reflow Soldering)

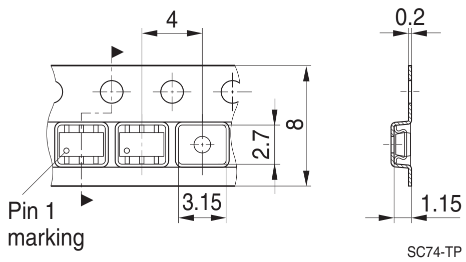

Figure 4-4 SC74 Packing

References

[1] Infineon AG - **Application Note AN210**: Effective ESD Protection Design at System Level using VF-TLP Characterization Methodology

[2] Infineon AG - Recommendations for PCB Assembly of Infineon TSLP and TSSLP Packages

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