

**N-Channel Logic Level Power MOSFET  
50 V, 14 A, 100 mΩ**

These are N-channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers and relay drivers. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate bias in the 3V-5V range, thereby facilitating true on-off power control directly from logic level (5V) integrated circuits.

Formerly developmental type TA09870.

**Ordering Information**

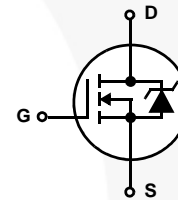
PART NUMBER	PACKAGE	BRAND
RFD14N05L	TO-251AA	14N05L
RFD14N05LSM	TO-252AA	14N05L
RFD14N05LSM9A	TO-252AA	14N05L

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252AA variant in the tape and reel, i.e., RFD14N05LSM9A.

**Features**

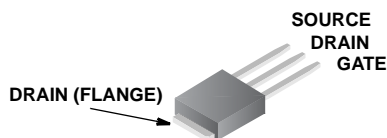
- 14A, 50V
- $r_{DS(ON)} = 0.100\Omega$
- Temperature Compensating PSPICE® Model
- Can be Driven Directly from CMOS, NMOS, and TTL Circuits
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- 175°C Operating Temperature
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

**Symbol**



**Packaging**

JEDEC TO-251AA



JEDEC TO-252AA



# RFD14N05L, RFD14N05LSM

## Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

	RFD14N05L, RFD14N05LSM, RFD14N05LSM9A	UNITS	
Drain to Source Voltage (Note 1).....	$V_{DSS}$	50	V
Drain to Gate Voltage ( $R_{GS} = 20k\Omega$ ) (Note 1).....	$V_{DGR}$	50	V
Gate to Source Voltage.....	$V_{GS}$	$\pm 10$	V
Continuous Drain Current.....	$I_D$	14	A
Pulsed Drain Current (Note 3).....	$I_{DM}$	Refer to Peak Current Curve	
Pulsed Avalanche Rating.....	$E_{AS}$	Refer to UIS Curve	
Power Dissipation.....	$P_D$	48	W
Derate above $25^\circ\text{C}$ .....		0.32	$\text{W}/^\circ\text{C}$
Operating and Storage Temperature.....	$T_J, T_{STG}$	-55 to 175	$^\circ\text{C}$
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s.....	$T_L$	300	$^\circ\text{C}$
Package Body for 10s, See Techbrief 334.....	$T_{pk}$	260	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

- $T_J = 25^\circ\text{C}$  to  $150^\circ\text{C}$ .

## Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	$BV_{DSS}$	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$ , Figure 13	50	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$ , Figure 12	1	-	2	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}, T_C = 150^\circ\text{C}$	-	-	50	$\mu\text{A}$
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 10\text{V}$	-	-	$\pm 100$	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = 14\text{A}, V_{GS} = 5\text{V}$ , Figures 9, 11	-	-	0.100	$\Omega$
Turn-On Time	$t_{(ON)}$	$V_{DD} = 25\text{V}, I_D = 7\text{A},$ $R_L = 3.57\Omega, V_{GS} = 5\text{V},$ $R_{GS} = 0.6\Omega$	-	-	60	ns
Turn-On Delay Time	$t_{d(ON)}$		-	13	-	ns
Rise Time	$t_r$		-	24	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	42	-	ns
Fall Time	$t_f$		-	16	-	ns
Turn-Off Time	$t_{(OFF)}$		-	-	100	ns
Total Gate Charge	$Q_{g(TOT)}$	$V_{GS} = 0\text{V}$ to $10\text{V}$	-	-	40	nC
Gate Charge at 5V	$Q_{g(5)}$	$V_{GS} = 0\text{V}$ to $5\text{V}$				
Threshold Gate Charge	$Q_{g(TH)}$	$V_{GS} = 0\text{V}$ to $1\text{V}$				
Input Capacitance	$C_{ISS}$	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$ Figure 14	-	670	-	pF
Output Capacitance	$C_{OSS}$		-	185	-	pF
Reverse Transfer Capacitance	$C_{RSS}$		-	50	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	3.125	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-251	-	-	100	$^\circ\text{C}/\text{W}$
	$R_{\theta JA}$	TO-252	-	-	100	$^\circ\text{C}/\text{W}$

## Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	$V_{SD}$	$I_{SD} = 14\text{A}$	-	-	1.5	V
Diode Reverse Recovery Time	$t_{rr}$	$I_{SD} = 14\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	125	ns

### NOTES:

- Pulse Test: Pulse Width  $\leq 300\text{ms}$ , Duty Cycle  $\leq 2\%$ .
- Repetitive Rating: Pulse Width limited by max junction temperature. See Transient Thermal Impedance Curve (Figure 3) and Peak Current Capability Curve (Figure 5).

Typical Performance Curves Unless Otherwise Specified

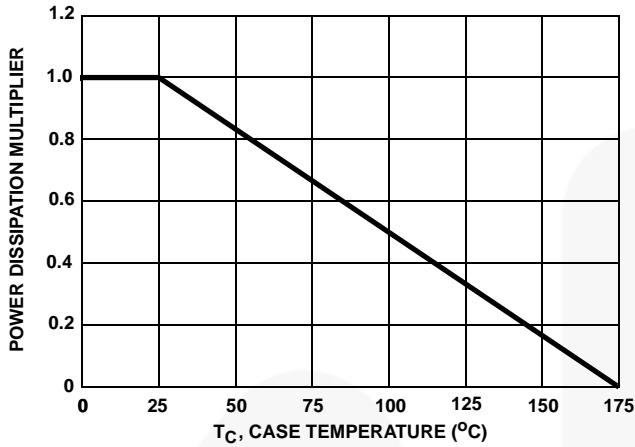


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

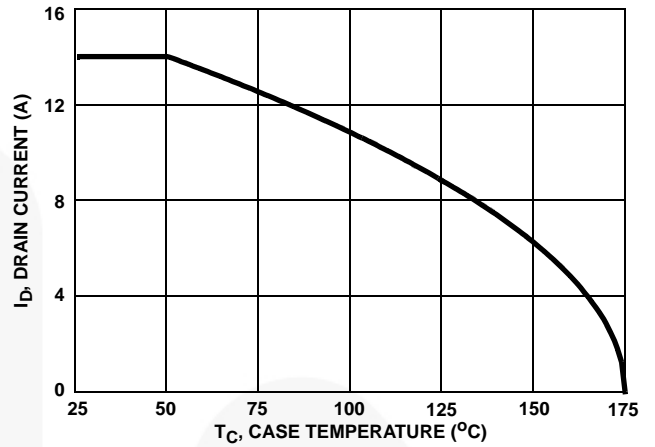


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

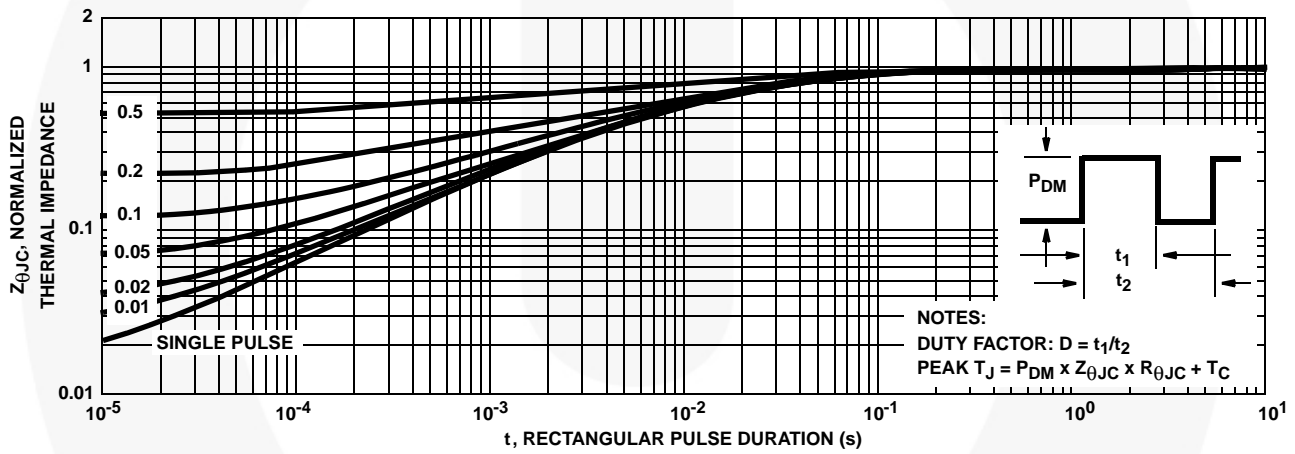


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

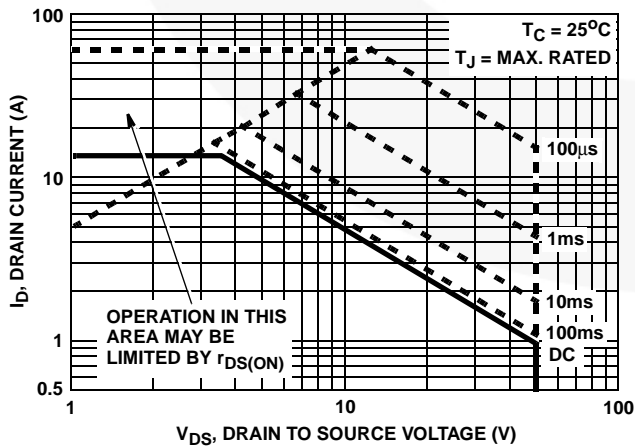


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

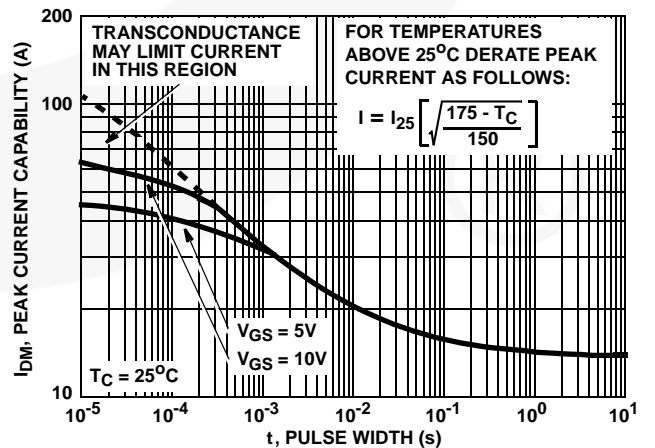
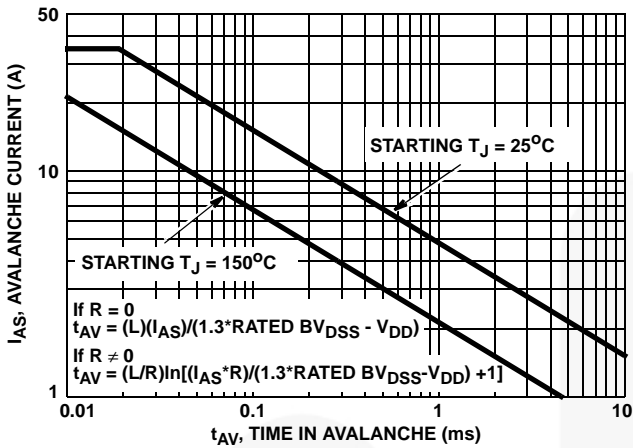


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves Unless Otherwise Specified (Continued)



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING

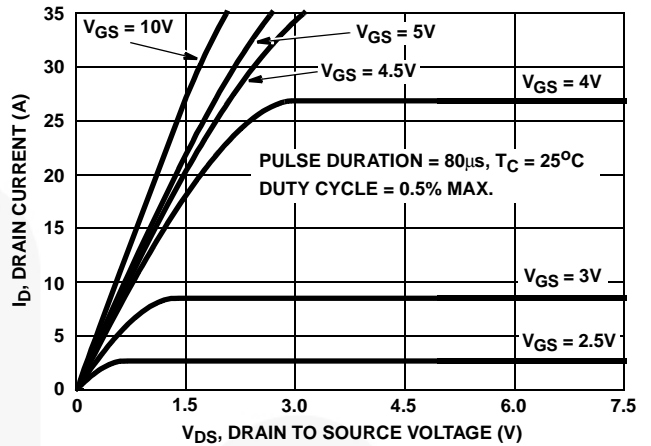


FIGURE 7. SATURATION CHARACTERISTICS

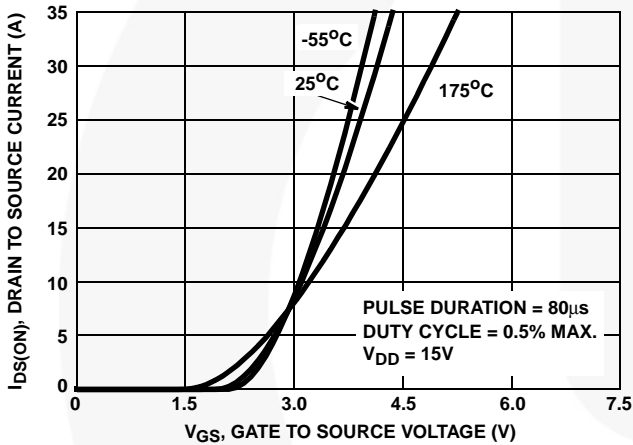


FIGURE 8. TRANSFER CHARACTERISTICS

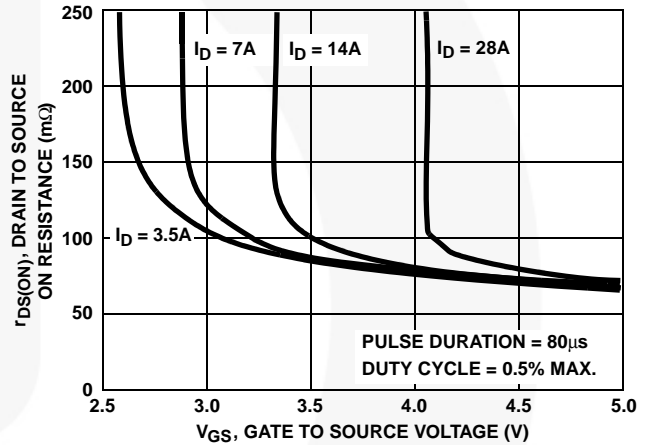


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

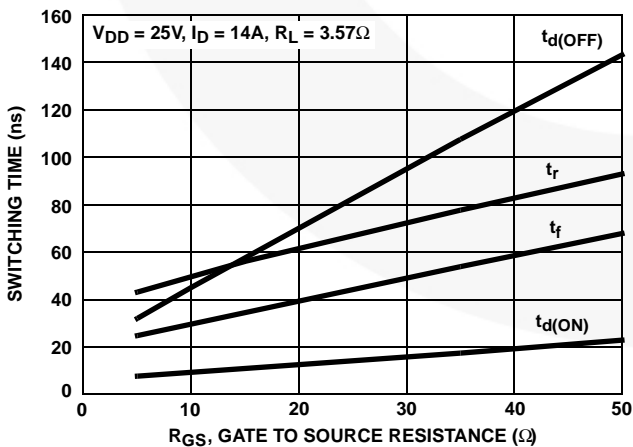


FIGURE 10. SWITCHING TIME vs GATE RESISTANCE

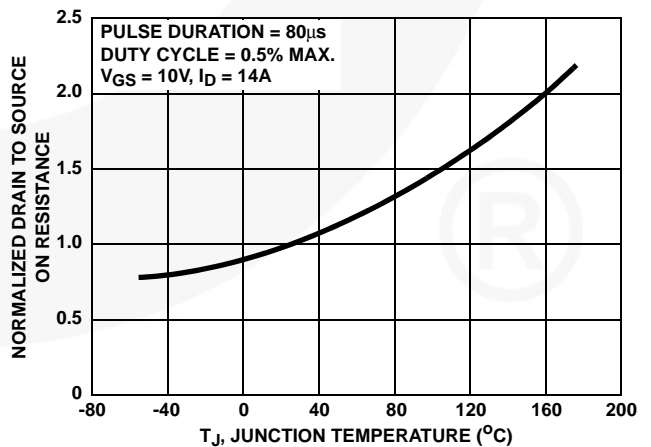


FIGURE 11. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

**Typical Performance Curves** Unless Otherwise Specified (Continued)

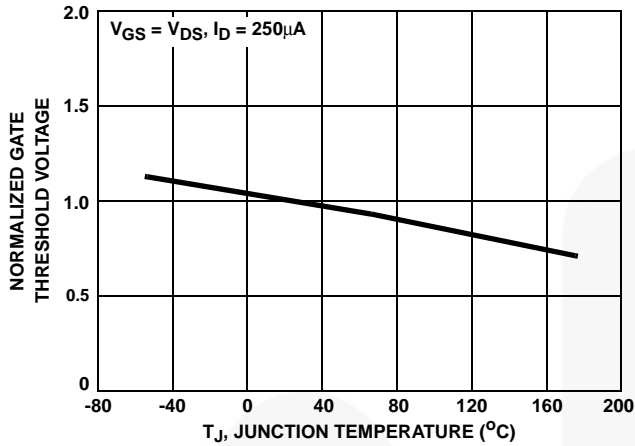


FIGURE 12. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

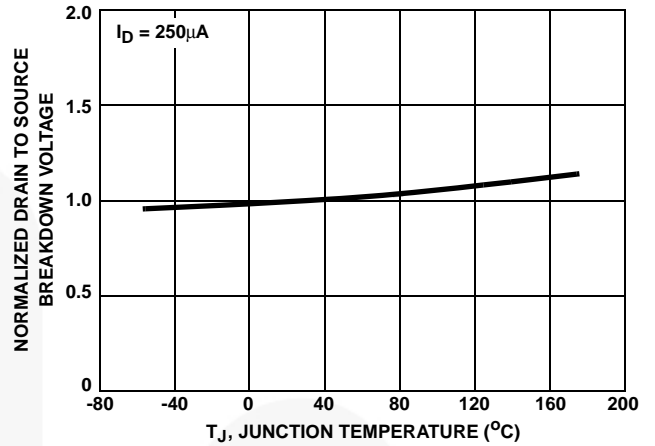


FIGURE 13. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

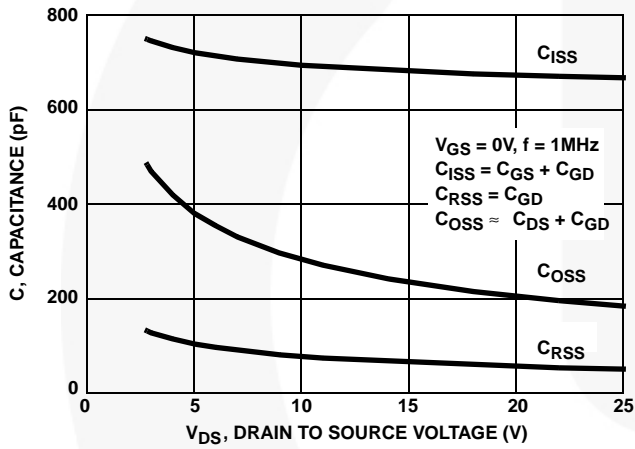
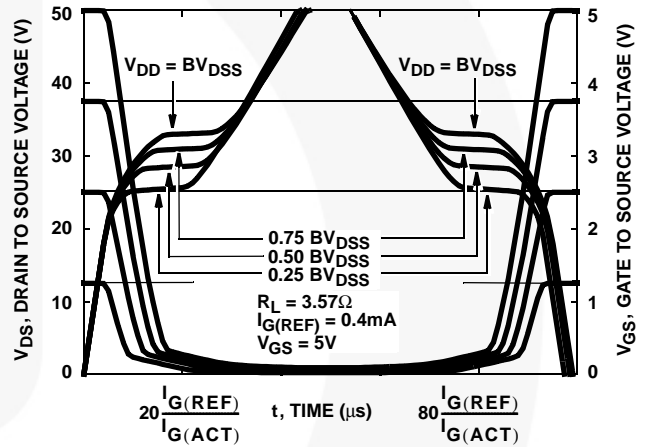


FIGURE 14. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260, FIGURE 15. TRANSCONDUCTANCE vs DRAIN CURRENT

**Test Circuits and Waveforms**

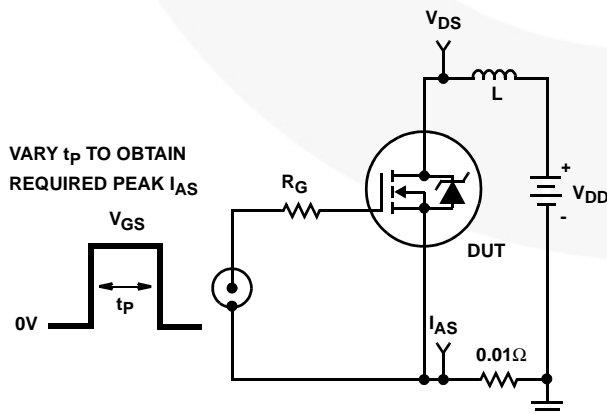


FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

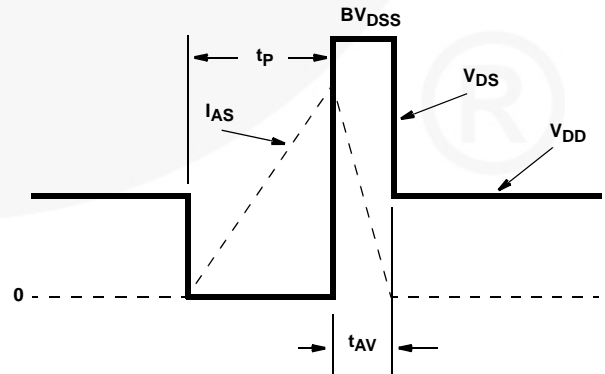


FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms (Continued)

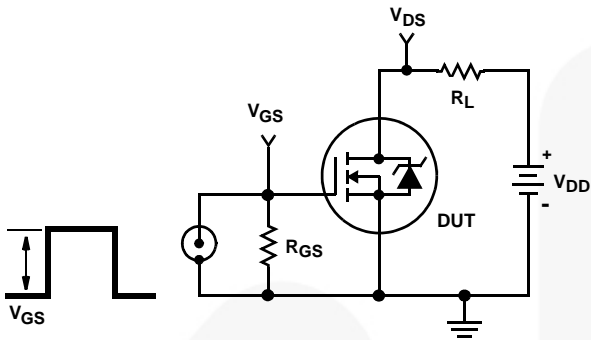


FIGURE 18. SWITCHING TIME TEST CIRCUIT

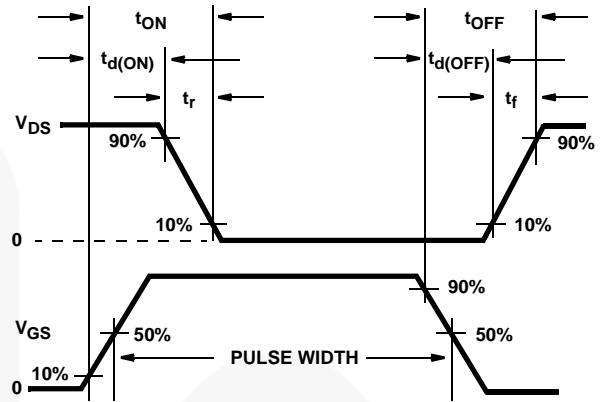


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

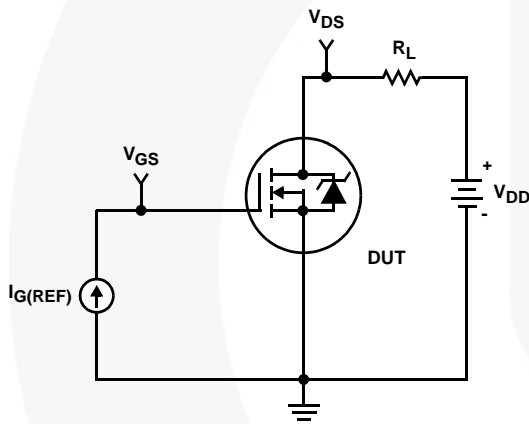


FIGURE 20. GATE CHARGE TEST CIRCUIT

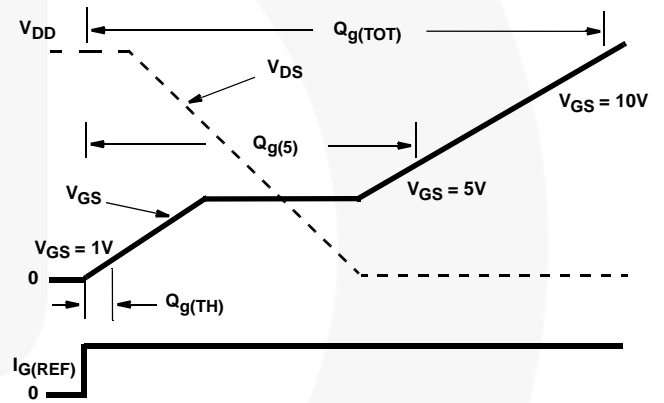



FIGURE 21. GATE CHARGE WAVEFORMS





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