FAN3850T
Microphone Pre-Amplifier with Temperature Compensation and Digital Output

Features
- Optimized for Mobile Handset and Notebook PC Microphone Applications
- Accepts Input from Electret Condenser Microphones
- Pulse Density Modulation (PDM) Output
- Standard 5-Wire Digital Interface
- Amplifier Gain: 15.7dB or 13.7dB
- Negative Temperature Coefficient to Compensate for ECM Positive Temperature Coefficient
- Low Input Capacitance, High PSR, 20kHz Pre-Amplifier
- Low-Power, 1.5µA Sleep Mode
- Typical 420µA Supply Current
- Signal to Noise Ratio of 62.4dB(A)
- Total Harmonic Distortion: 0.01%
- Input Clock Frequency Range of 1-4MHz
- Integrated Low Drop-Out Regulator (LDO)
- Small 1.26mm x 0.86mm 6-Ball WLCSP

Applications
- Electret Condenser Microphones with Digital Output
- Mobile Handsets
- Headset Accessories
- Personal Computers (PC)

Description
The FAN3850T integrates a pre-amplifier, LDO, and Analog-to-Digital Converter (ADC) to convert Electret Condenser Microphone (ECM) outputs to digital Pulse Density Modulation (PDM) data streams. The pre-amplifier accepts analog signals from the ECM and drives an over-sampled sigma delta ADC and outputs PDM data. The PDM digital audio has the advantage of noise rejection and interface-to-mobile handset processors.

The FAN3850T is powered from the system supply rails up to 3.63V, with a low power consumption of only 0.85mW, and less than 20µW in Power-Down Mode. The device compensates for the temperature variation of the microphone element to achieve a flat sensitivity response over-temperature.

Ordering Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Gain Option</th>
<th>Operating Temperature Range</th>
<th>Package</th>
<th>Packing Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>FAN3850TUC15X35</td>
<td>15.7dB</td>
<td>-30°C to +85°C</td>
<td>6-Ball, Wafer-Level Chip-Scale Package (WLCSP)</td>
<td>3000 Unit Tape &amp; Reel</td>
</tr>
<tr>
<td>FAN3850TUC13X35</td>
<td>13.7dB</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note:
1. Alternate gain options and temperature coefficient slopes are possible. Please contact a Fairchild representative.
Pin Configuration

Figure 2. Pin Configuration (Top View)

Pin Definitions

<table>
<thead>
<tr>
<th>Pin#</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>CLOCK</td>
<td>Input</td>
<td>Clock Input</td>
</tr>
<tr>
<td>B1</td>
<td>GND</td>
<td>Input</td>
<td>Ground Pin</td>
</tr>
<tr>
<td>C1</td>
<td>DATA</td>
<td>Output</td>
<td>PDM Output – 1-Bit ADC</td>
</tr>
<tr>
<td>A2</td>
<td>SELECT</td>
<td>Input</td>
<td>Rising or Falling Clock-Edge Select</td>
</tr>
<tr>
<td>B2</td>
<td>INPUT</td>
<td>Input</td>
<td>Microphone Input</td>
</tr>
<tr>
<td>C2</td>
<td>VDD</td>
<td>Input</td>
<td>Device Power Pin</td>
</tr>
</tbody>
</table>
Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>DC Supply Voltage</td>
<td>-0.3</td>
<td>4.0</td>
<td>V</td>
</tr>
<tr>
<td>VIO</td>
<td>Analog and Digital I/O</td>
<td>-0.3</td>
<td>VCC+0.3</td>
<td>V</td>
</tr>
<tr>
<td>ESD</td>
<td>Human Body Model, JESD22-A114(2), All Pins Except Microphone Input</td>
<td>±7</td>
<td></td>
<td>kV</td>
</tr>
<tr>
<td>ESD</td>
<td>Human Body Model, JESD22-A114(2), Microphone Input</td>
<td>±300</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

Note:

2. This device is fabricated using CMOS technology and is therefore susceptible to damage from electrostatic discharges. Appropriate precautions must be taken during handling and storage of this device to prevent exposure to ESD.

Reliability Information

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>TJ</td>
<td>Junction Temperature</td>
<td></td>
<td>+150</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>TSTG</td>
<td>Storage Temperature Range</td>
<td>-65</td>
<td></td>
<td>+125</td>
<td>°C</td>
</tr>
<tr>
<td>TREFLOW</td>
<td>Peak Reflow Temperature</td>
<td></td>
<td></td>
<td>+260</td>
<td>°C</td>
</tr>
<tr>
<td>ΘJA</td>
<td>Thermal Resistance, JEDEC Standard, Multilayer Test Boards, Still Air</td>
<td>90</td>
<td></td>
<td></td>
<td>°C/W</td>
</tr>
</tbody>
</table>

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>TA</td>
<td>Operating Temperature Range</td>
<td>-30</td>
<td></td>
<td>+85</td>
<td>°C</td>
</tr>
<tr>
<td>VDD</td>
<td>Supply Voltage Range</td>
<td>1.64</td>
<td>1.80</td>
<td>3.63</td>
<td>V</td>
</tr>
<tr>
<td>tRF-CLK</td>
<td>Clock Rise and Fall Time</td>
<td></td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>
## Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for $T_A=25^\circ C$, $V_{DD}=1.8V$, $V_{IN}=94dBSPL$, $f_{CLK}=2.4MHz$, duty cycle = 50%, and $C_{MIC}=15pF$.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>Supply Voltage Range</td>
<td></td>
<td>1.64</td>
<td>1.80</td>
<td>3.63</td>
<td>V</td>
</tr>
<tr>
<td>$I_{DD}$</td>
<td>Supply Current</td>
<td>$INPUT=AC$ Coupled to $GND$, $CLOCK=On$, No Load</td>
<td>420</td>
<td></td>
<td></td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$I_{SLEEP}$</td>
<td>Sleep Mode Current</td>
<td>$f_{CLK}=GND$</td>
<td></td>
<td>1.4</td>
<td>8.0</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>PSR</td>
<td>Power Supply Rejection</td>
<td>$INPUT=AC$ Coupled to $GND$, Test Signal on $V_{DD}=217Hz$ Square Wave and Broad Band Noise, both 100mVp-p</td>
<td></td>
<td></td>
<td></td>
<td>dBSFS</td>
</tr>
<tr>
<td>$I_{NOM}$</td>
<td>Nominal Sensitivity</td>
<td>$INPUT=94dBSPL$</td>
<td></td>
<td></td>
<td></td>
<td>dBSFS</td>
</tr>
<tr>
<td>SNR</td>
<td>Signal-to-Noise Ratio</td>
<td>$f_{IN}=1kHz$, A-Weighted</td>
<td>62.4</td>
<td></td>
<td></td>
<td>dBA</td>
</tr>
<tr>
<td>$e_N$</td>
<td>Input Referred Noise</td>
<td>$20Hz$ to $20kHz$, A-Weighted, $15.7dB$ Gain</td>
<td>5.3</td>
<td>8.6</td>
<td></td>
<td>$\mu V_{RMS}$</td>
</tr>
<tr>
<td>THD</td>
<td>Total Harmonic Distortion</td>
<td>$f_{IN}=1kHz$, $INPUT=-26dBFS$</td>
<td>0.01</td>
<td>0.10</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>THD+N</td>
<td>THD and Noise</td>
<td>$0Hz \leq f_{IN} \leq 1kHz$, $INPUT=-20dBFS$</td>
<td>0.2</td>
<td>1.0</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f_{IN}=1kHz$, $INPUT=-5dBFS$</td>
<td>1.0</td>
<td>5.0</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f_{IN}=1kHz$, $INPUT=0dBFS$</td>
<td>5.0</td>
<td>10.0</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>$t_c$</td>
<td>Temperature Coefficient</td>
<td>Gain Measured at $50^\circ C$ and $-10^\circ C$</td>
<td></td>
<td></td>
<td></td>
<td>dB/C</td>
</tr>
<tr>
<td>$C_{IN}$</td>
<td>Input Capacitance</td>
<td>$INPUT$</td>
<td>0.2</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>$R_{IN}$</td>
<td>Input Resistance</td>
<td>$INPUT$</td>
<td>&gt;100</td>
<td></td>
<td></td>
<td>$\Omega$</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>CLOCK &amp; SELECT Input, Logic LOW Level</td>
<td></td>
<td>0.3</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>CLOCK &amp; SELECT Input, Logic HIGH Level</td>
<td></td>
<td>1.5</td>
<td></td>
<td></td>
<td>$V_{DD}+0.3$ V</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Data Output, Logic LOW Level</td>
<td></td>
<td>0.35×$V_{DD}$</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Data Output, Logic HIGH Level</td>
<td></td>
<td>0.65×$V_{DD}$</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IN15dB}$</td>
<td>Maximum Input Signal for $15.7dB$ of Gain</td>
<td>$f_{IN}=1kHz$, THD+N &lt; 10%, DC Level=0V</td>
<td>503</td>
<td></td>
<td></td>
<td>mVp-p</td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>Acoustic Overload Point</td>
<td>THD &lt; 10%</td>
<td>120</td>
<td></td>
<td></td>
<td>dBSPL</td>
</tr>
</tbody>
</table>

*Continued on the following page...*
Electrical Characteristics (Continued)

Unless otherwise specified, all limits are guaranteed for $T_A=25^{\circ}C$, $V_{DD}=1.8\text{V}$, $V_{IN}=94\text{dB}$ (SPL), $f_{CLK}=2.4\text{MHz}$, duty cycle = 50%, and $C_{MIC}=15\text{pF}$.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_A$</td>
<td>Time from CLOCK Transition to Data Becoming Valid</td>
<td>On Falling Edge of CLOCK, SELECT=GND, $C_{LOAD}=15\text{pF}$</td>
<td>18</td>
<td>43</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_B$</td>
<td>Time from CLOCK Transition to Data Becoming Hi-Z</td>
<td>On Rising Edge of CLOCK, SELECT=GND, $C_{LOAD}=15\text{pF}$</td>
<td>0</td>
<td>5</td>
<td>16</td>
<td>ns</td>
</tr>
<tr>
<td>$t_A$</td>
<td>Time from CLOCK Transition to Data Becoming Valid</td>
<td>On Rising Edge of CLOCK, SELECT=VDD, $C_{LOAD}=15\text{pF}$</td>
<td>18</td>
<td>56</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_B$</td>
<td>Time from CLOCK Transition to Data Becoming Hi-Z</td>
<td>On Falling Edge of CLOCK, SELECT=VDD, $C_{LOAD}=15\text{pF}$</td>
<td>0</td>
<td>5</td>
<td>16</td>
<td>ns</td>
</tr>
<tr>
<td>$f_{CLK}$</td>
<td>Input CLOCK Frequency</td>
<td>Active Mode</td>
<td>1.0</td>
<td>2.4</td>
<td>4.0</td>
<td>MHz</td>
</tr>
<tr>
<td>$CLK_{dc}$</td>
<td>CLOCK Duty Cycle</td>
<td></td>
<td>40</td>
<td>50</td>
<td>60</td>
<td>%</td>
</tr>
<tr>
<td>$t_{WAKEUP}$</td>
<td>Wake-Up Time</td>
<td>$f_{CLK}=2.4\text{MHz}$</td>
<td>0.35</td>
<td>2.00</td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>$f_{FALLASLEEP}$</td>
<td>Fall-Asleep Time</td>
<td>$f_{CLK}=2.4\text{MHz}$</td>
<td>0</td>
<td>0.01</td>
<td>1.00</td>
<td>ms</td>
</tr>
<tr>
<td>$C_{LOAD}$</td>
<td>Load Capacitance on Data</td>
<td></td>
<td>100</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
</tbody>
</table>

Notes:
3. Pseudo-random noise with triangular probability density function. Bandwidth up to 10MHz.
4. Assumes 120dB(SPL) is mapped to 0dBFS.
5. Assumes an input -41, or -38dBV, depending on the part-specific gain.
6. Verified by design simulation, showing idle tones and low noise level modulation to be typical 96dB.
7. Guaranteed by characterization.
8. All parameters are tested at 2.4MHz. Frequency range guaranteed by characterization.
9. Device wakes up when $f_{CLK}\geq 300\text{kHz}$.
10. Device falls asleep when $f_{CLK}\leq 70\text{kHz}$.
11. Guaranteed by design.
12. Temperature coefficient is calculated by measuring gain in db at 50°F and -10°F and dividing by 60 (Gain(50°F) – Gain(-10°F)/60).

Figure 3. Interface Timing
Typical Performance Characteristics

Unless otherwise specified, all limits are guaranteed for \( T_A = 25^\circ C \), \( V_{DD} = 1.8V \), \( V_{IN} = 94dB(SPL) \), \( f_{CLK} = 2.4MHz \), and duty cycle=50%.

Figure 4. THD, SINAD, and SNR vs. Input Amplitude

Figure 5. THD, SINAD, and SNR vs. Output Level
Figure 6. Gain vs. Temperature (~0.035dB/°C)(1)

Note:
13. Alternate temperature coefficient slopes are possible. Please contact a Fairchild representative.
Applications Information

Figure 7. Mono Microphone Application Circuit

Figure 8. Stereo Microphone Application Circuit
Applications Information

A 0.1µF decoupling capacitor is required for $V_{DD}$. It can be located either inside the microphone or on the PCB very close to the VDD pin.

Due to high input impedance, careful consideration should be taken to remove all flux used during the reflow soldering process.

A 100Ω resistance is recommended on the clock output of the device driving the FAN3850T to minimize ringing and improve signal integrity.

For optimal PSR, route a trace to the VDD pin. Do not place a $V_{DD}$ plane under the device.
Physical Dimensions

Figure 10. 6-Ball, Wafer-Level Chip-Scale Package (WLCSP)

Table 1. Product-Specific Dimensions

<table>
<thead>
<tr>
<th>D</th>
<th>E</th>
<th>X</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.260mm</td>
<td>0.860mm</td>
<td>0.145mm</td>
<td>0.145mm</td>
</tr>
</tbody>
</table>

Ball Composition: SN97.5-Ag2.5

NOTES:
A. NO JEDEC REGISTRATION APPLIES.
B. DIMENSIONS ARE IN MILLIMETERS.
D. DATUM C, THE SEATING PLANE IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
E. PACKAGE TYPICAL HEIGHT IS 273 MICRONS ±23 MICRONS (254-300 MICRONS).
F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

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SignaWise™
SmartMax™
SMART START™
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SPM™
STEALTH™
SuperFET®
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
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TinyPower™
TinyPWM™
TinyWire™
TranSIC™
TriFault Detect™
TRUECURRENT™
u babe™
UHC™
Ultra FRFET™
UniFET™
VCX™
VisualMax™
VoltagePlus™
XS™

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2. A critical component in any component of a life support device, or system whose failure to perform can be reasonably expected to result in the failure of the life support device or system, or to affect its safety or effectiveness.

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PRODUCT STATUS DEFINITIONS

<table>
<thead>
<tr>
<th>Datasheet Identification</th>
<th>Product Status</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Advance Information</td>
<td>Formative / In Design</td>
<td>Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.</td>
</tr>
<tr>
<td>Preliminary</td>
<td>First Production</td>
<td>Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.</td>
</tr>
<tr>
<td>No Identification Needed</td>
<td>Full Production</td>
<td>Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.</td>
</tr>
<tr>
<td>Obsolete</td>
<td>Not in Production</td>
<td>Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.</td>
</tr>
</tbody>
</table>

Rev. 161
Mouser Electronics

Authorized Distributor

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Fairchild Semiconductor:
FAN3850TUC13X35  FAN3850TUC15X35