Features

- True dual-ported memory cells, which allow simultaneous reads of the same memory location
- 4K × 8 organization
- 0.65 micron CMOS for optimum speed and power
- High speed access: 15 ns
- Low operating power: ICC = 180 mA (max)
- Fully asynchronous operation
- Automatic power down
- Available in 52-pin plastic leaded chip carrier (PLCC)
- Pb-free packages available

Functional Description

The CY7C135 is a high speed CMOS 4K × 8 dual-port static RAMs. Two ports are provided permitting independent, asynchronous access for reads and writes to any location in memory. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: chip enable (CE), read or write enable (R/W), and output enable (OE). The CY7C135 is suited for those systems that do not require on-chip arbitration or are intolerant of wait states. Therefore, the user must be aware that simultaneous access to a location is possible. An automatic power down feature is controlled independently on each port by a chip enable (CE) pin.

The CY7C135 is available in 52-pin PLCC.

For a complete list of related documentation, click here.
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Selection Guide

<table>
<thead>
<tr>
<th>Parameter</th>
<th>7C135-15</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum access time</td>
<td>15</td>
<td>ns</td>
</tr>
<tr>
<td>Maximum operating current</td>
<td>Commercial</td>
<td>220</td>
</tr>
<tr>
<td>Maximum standby current for $I_{SB1}$</td>
<td>Commercial</td>
<td>60</td>
</tr>
</tbody>
</table>

Pin Configurations

![Figure 1. 52-pin PLCC pinout (Top View)](image)

Pin Definitions

<table>
<thead>
<tr>
<th>Left Port</th>
<th>Right Port</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0L–11L</td>
<td>A0R–11R</td>
<td>Address lines</td>
</tr>
<tr>
<td>CE_L</td>
<td>CE_R</td>
<td>Chip Enable</td>
</tr>
<tr>
<td>OE_L</td>
<td>OE_R</td>
<td>Output Enable</td>
</tr>
<tr>
<td>R/W_L</td>
<td>R/W_R</td>
<td>Read/Write Enable</td>
</tr>
</tbody>
</table>
Architecture

The CY7C135 consists of an array of 4K words of 8 bits each of dual-port RAM cells, I/O and address lines, and control signals (CE, OE, R/W).

Functional Description

Write Operation

Data must be set up for a duration of $t_{SD}$ before the rising edge of R/W to guarantee a valid write. Because there is no on-chip arbitration, the user must be sure that a specific location is not accessed simultaneously by both ports or erroneous data could result. A write operation is controlled by either the OE pin (see Figure 6 on page 9) or the R/W pin (see Figure 7 on page 9). Data can be written $t_{HZOE}$ after the OE is deasserted or $t_{HZWE}$ after the falling edge of R/W. Required inputs for write operations are summarized in Table 1.

If a location is being written to by one port and the opposite port attempts to read the same location, a port-to-port flowthrough delay is met before the data is valid on the output. Data is valid on the port wishing to read the location $t_{DDD}$ after the data is presented on the writing port.

Read Operation

When reading the device, the user must assert both the OE and CE pins. Data is available $t_{ACE}$ after CE or $t_{DOE}$ after OE are asserted. Required inputs for read operations are summarized in Table 1.

Table 1. Non-Contending Read/Write

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>CE</td>
<td>R/W</td>
<td>OE</td>
</tr>
<tr>
<td>H</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>X</td>
</tr>
</tbody>
</table>
**Maximum Ratings**

Exceeding maximum ratings \([1]\) may shorten the useful life of the device. User guidelines are not tested.

- **Storage temperature**: \(-65^\circ\text{C} to +150^\circ\text{C}\)
- **Ambient temperature with power applied**: \(-55^\circ\text{C} to +125^\circ\text{C}\)
- **Supply voltage to ground potential (Pin 48 to Pin 24)**: \(-0.5\text{ V} to +7.0\text{ V}\)
- **DC voltage applied to outputs in High Z state**: \(-0.5\text{ V} to +7.0\text{ V}\)

**Electrical Characteristics**

Over the Operating Range

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>7C135-15</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{OH})</td>
<td>Output HIGH voltage</td>
<td>(V_{CC} = \text{Min}, I_{OH} = -4.0\text{ mA})</td>
<td>2.4</td>
<td>V</td>
</tr>
<tr>
<td>(V_{OL})</td>
<td>Output LOW voltage</td>
<td>(V_{CC} = \text{Min}, I_{OL} = 4.0\text{ mA})</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>(V_{IH})</td>
<td>Input HIGH voltage</td>
<td></td>
<td>2.2</td>
<td>V</td>
</tr>
<tr>
<td>(V_{IL})</td>
<td>Input LOW voltage</td>
<td></td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>(I_{IX})</td>
<td>Input load current</td>
<td>(GND \leq V_{I} \leq V_{CC})</td>
<td>-10</td>
<td>(\mu\text{A})</td>
</tr>
<tr>
<td>(I_{IOZ})</td>
<td>Output leakage current</td>
<td>Outputs disabled, (GND \leq V_{O} \leq V_{CC})</td>
<td>-10</td>
<td>(\mu\text{A})</td>
</tr>
<tr>
<td>(I_{CC})</td>
<td>Operating current</td>
<td>(V_{CC} = \text{Max}, I_{OUT} = 0\text{ mA})</td>
<td>Commercial</td>
<td>220</td>
</tr>
<tr>
<td>(I_{SB1})</td>
<td>Standby current (Both ports TTL levels)</td>
<td>(\overline{CE}<em>L \text{ and } \overline{CE}<em>R \geq V</em>{IH}, f = f</em>{\text{MAX}}[3])</td>
<td>Commercial</td>
<td>60</td>
</tr>
<tr>
<td>(I_{SB2})</td>
<td>Standby current (One port TTL level)</td>
<td>(\overline{CE}<em>L \text{ and } \overline{CE}<em>R \geq V</em>{IH}, f = f</em>{\text{MAX}}[3])</td>
<td>Commercial</td>
<td>130</td>
</tr>
<tr>
<td>(I_{SB3})</td>
<td>Standby current (Both ports CMOS levels)</td>
<td>Both ports (\overline{CE}<em>L \text{ and } \overline{CE}<em>R \geq V</em>{CC} - 0.2\text{ V, } V</em>{IN} \geq V_{CC} - 0.2\text{ V or } V_{IN} \leq 0.2\text{ V, } f = 0 [3])</td>
<td>Commercial</td>
<td>15</td>
</tr>
<tr>
<td>(I_{SB4})</td>
<td>Standby current (One port CMOS level)</td>
<td>One port (\overline{CE}<em>L \text{ or } \overline{CE}<em>R \geq V</em>{CC} - 0.2\text{ V, } V</em>{IN} \geq V_{CC} - 0.2\text{ V or } V_{IN} \leq 0.2\text{ V, Active port outputs, } f = f_{\text{MAX}}[3])</td>
<td>Commercial</td>
<td>125</td>
</tr>
</tbody>
</table>

**Notes**

1. The voltage on any input or I/O pin cannot exceed the power pin during power up.
2. Pulse width < 20 ns.
3. \(f_{\text{MAX}} = 1/f_{\text{RC}}\) = All inputs cycling at \(f = 1/f_{\text{RC}}\) (except output enable). \(f = 0\) means no address or control lines change. This applies only to inputs at CMOS level standby \(I_{SB3}\).
### Capacitance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>C\textsubscript{IN}</td>
<td>Input capacitance</td>
<td>T\textsubscript{A} = 25 °C, f = 1 MHz, V\textsubscript{CC} = 5.0 V</td>
<td>10</td>
<td>pF</td>
</tr>
<tr>
<td>C\textsubscript{OUT}</td>
<td>Output capacitance</td>
<td></td>
<td>10</td>
<td>pF</td>
</tr>
</tbody>
</table>

### AC Test Loads and Waveforms

![AC Test Loads and Waveforms](image)

**Figure 2. AC Test Loads and Waveforms**

(a) Normal Load (Load 1)  
(b) Thévenin Equivalent (Load 1)  
(c) Three-State Delay (Load 3)

**Note**
4. Tested initially and after any design or process changes that may affect these parameters.
Switching Characteristics
Over the Operating Range

<table>
<thead>
<tr>
<th>Parameter [5]</th>
<th>Description</th>
<th>7C135-15 Unit</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Read Cycle</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tRC</td>
<td>Read cycle time</td>
<td>15 – ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tAA</td>
<td>Address to data valid</td>
<td>– 15 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tOHA</td>
<td>Output hold from address change</td>
<td>3 – ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tACE</td>
<td>CE LOW to data valid</td>
<td>– 15 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tDOE</td>
<td>OE LOW to data valid</td>
<td>– 10 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tLZOE [6, 7, 8]</td>
<td>OE Low to Low Z</td>
<td>3 – ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tHZOE [6, 7, 8]</td>
<td>OE HIGH to High Z</td>
<td>– 10 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tLZCE [6, 7, 8]</td>
<td>CE LOW to Low Z</td>
<td>3 – ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tHZCE [6, 7, 8]</td>
<td>CE HIGH to High Z</td>
<td>– 10 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tPU [8]</td>
<td>CE LOW to Power-up</td>
<td>0 – ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tPD [8]</td>
<td>CE HIGH to Power-down</td>
<td>– 15 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Write Cycle</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tWC</td>
<td>Write cycle time</td>
<td>15 – ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tSCE</td>
<td>CE LOW to Write End</td>
<td>12 – ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tAW</td>
<td>Address setup to Write End</td>
<td>12 – ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tHA</td>
<td>Address hold from Write End</td>
<td>2 – ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tSA</td>
<td>Address setup to Write Start</td>
<td>0 – ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tPWE</td>
<td>Write pulse width</td>
<td>12 – ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tSD</td>
<td>Data setup to Write End</td>
<td>10 – ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tHD</td>
<td>Data hold from Write End</td>
<td>0 – ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tHZWE [7, 8]</td>
<td>R/W LOW to High Z</td>
<td>– 10 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tLZWE [7, 8]</td>
<td>R/W HIGH to Low Z</td>
<td>3 – ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tWDD [9]</td>
<td>Write pulse to data delay</td>
<td>– 30 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tDDD [9]</td>
<td>Write data valid to read data valid</td>
<td>– 25 ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Notes**
5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified IOL/IOH and 30 pF load capacitance.
6. At any given temperature and voltage condition for any given device, tHZCE is less than tLZCE and tHZOE is less than tLZOE.
7. Test conditions used are Load 3.
8. This parameter is guaranteed but not tested.
9. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Figure 5 on page 8.
Switching Waveforms

Figure 3. Read Cycle No. 1\textsuperscript{[10, 11]}

Either Port Address Access

![diagram](attachment:read_cycle_no_1.png)

Figure 4. Read Cycle No. 2\textsuperscript{[10, 12]}

Either Port CE/OE Access

![diagram](attachment:read_cycle_no_2.png)

Figure 5. Read Timing with Port-to-Port\textsuperscript{[13]}

![diagram](attachment:read_timing_port_to_port.png)

Notes
10. R/W is HIGH for read cycle.
11. Device is continuously selected, CE = V\textsubscript{IL} and OE = V\textsubscript{IL}.
12. Address valid prior to or coincident with CE transition LOW.
13. CE\textsubscript{L} = CE\textsubscript{R} = LOW; N/R\textsubscript{L} = HIGH.
Switching Waveforms (continued)

Figure 6. Write Cycle No. 1: Œ Three-States Data I/Os (Either Port) \(^{[14, 15, 16]}\)

Figure 7. Write Cycle No. 2: R/W Three-States Data I/Os (Either Port) \(^{[15, 17]}\)

Notes

14. The internal write time of the memory is defined by the overlap of CE and R/W LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

15. R/W must be HIGH during all address transactions.

16. If CE is LOW during a R/W controlled write cycle, the write pulse width must be the larger of tPWE or (tHZWE + tSD) to allow the I/O drivers to turn off and data to be placed on the bus for the required tSD. If CE is HIGH during a R/W controlled write cycle (as in this example), this requirement does not apply and the write pulse can be as short as the specified tPWE.

17. Data I/O pins enter high impedance when Œ is held LOW during write.
Typical DC and AC Characteristics

NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE

NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE

OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE

NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE

NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE

TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE

TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING

NORMALIZED ICC vs. CYCLE TIME
### Ordering Information

**4K x 8 Dual-Port SRAM**

<table>
<thead>
<tr>
<th>Speed (ns)</th>
<th>Ordering Code</th>
<th>Package Diagram</th>
<th>Package Type</th>
<th>Operating Range</th>
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<tbody>
<tr>
<td>15</td>
<td>CY7C135-15JXC</td>
<td>51-85004</td>
<td>52-pin PLCC (Pb-free)</td>
<td>Commercial</td>
</tr>
</tbody>
</table>

### Ordering Code Definitions

- **Part Number Identifier**
- **Technology Code**: C = CMOS
- **Marketing Code**: 7 = SRAM
- **Company ID**: CY = Cypress
- **Temperature Range**: C = Commercial
- **Package Type**: J = 52-pin PLCC
- **Speed**: 15 ns
- **Pb-free**
Figure 8. 52-pin PLCC (0.756 × 0.756 Inches) J52 Package Outline, 51-85004
### Acronyms

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
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<tbody>
<tr>
<td>CMOS</td>
<td>Complementary Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>I/O</td>
<td>Input/Output</td>
</tr>
<tr>
<td>PLCC</td>
<td>Plastic Leaded Chip Carrier</td>
</tr>
<tr>
<td>SRAM</td>
<td>Static Random Access Memory</td>
</tr>
<tr>
<td>TQFP</td>
<td>Thin Quad Flat Pack</td>
</tr>
</tbody>
</table>

### Document Conventions

#### Units of Measure

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Unit of Measure</th>
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<tbody>
<tr>
<td>°C</td>
<td>degree Celsius</td>
</tr>
<tr>
<td>MHz</td>
<td>megahertz</td>
</tr>
<tr>
<td>µA</td>
<td>microampere</td>
</tr>
<tr>
<td>mA</td>
<td>milliampere</td>
</tr>
<tr>
<td>mV</td>
<td>millivolt</td>
</tr>
<tr>
<td>ns</td>
<td>nanosecond</td>
</tr>
<tr>
<td>Ω</td>
<td>ohm</td>
</tr>
<tr>
<td>pF</td>
<td>picofarad</td>
</tr>
<tr>
<td>V</td>
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<td>watt</td>
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Document History Page (continued)

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<td>4264122</td>
<td>SMCH</td>
<td>01/27/2014</td>
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<tr>
<td>*J</td>
<td>4580622</td>
<td>SMCH</td>
<td>11/26/2014</td>
<td>Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.</td>
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<tr>
<td>*K</td>
<td>5506734</td>
<td>NILE</td>
<td>11/04/2016</td>
<td>Updated Ordering Information: No change in part numbers. Removed column “Package Name”. Added a column “Package Diagram”. Updated to new template. Completing Sunset Review.</td>
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</tbody>
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