



XTX™ **conga-XEVAL**

*Detailed description of the congatec XTX™ evaluation
baseboard*

User's Guide

Revision 1.3

Revision History

| Revision | Date | Author | Changes |
|----------|----------|--------|---|
| 1.0 | 17.10.05 | HCH | Official release |
| 1.1 | 09.11.05 | HCH | Changed LPT/#FPY Signal; updated debug display description; added TP. |
| 1.2 | 20.01.06 | GDA | Corrected errors in sections 2.2, 2.4, 3.2.2 and added section 5 "Mechanical Drawing conga-XEVAL". Added link table to connector diagram page. Added description of pins 7 and 8 in the LCD power connector pinout table in section 3.4.2. Changed the LCD Voltage value for Jumper X45 5-6 from 12V to 3.3V. |
| 1.3 | 20.06.06 | GDA | Added pinout table for LPT2, COM3 and COM4. Corrected fuse values for X47 pinout, was 15A but the correct value is 1.5A. Added connection possibilities diagram for X47 connector. |

Preface

This user's guide provides information about the components, features and connectors available on the XTX Evaluation Baseboard.

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Intended Audience

This user's guide is intended for technically qualified personnel. It is not intended for general audiences.

Symbols

The following symbols are used in this user's guide:



Warning

Warnings indicate conditions that, if not observed, can cause personal injury.



Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.



Note

Notes call attention to important information that should be observed.



Connector Type

Describes the connector that must be used with the XTX Evaluation Baseboard, not the connector found on the XTX Evaluation Baseboard.



Link to connector diagram

This link icon is located in the top right corner of each page. It provides a direct link to the connector diagram on page 8 of this document.

Terminology

| Term | Description |
|----------------------|---|
| PCI Express (PCIe) | Peripheral Component Interface Express – next-generation high speed Serialized I/O bus |
| PCI Express Lane | One PCI Express Lane is a set of 4 signals that contains two differential lines for Transmitter and two differential lines for Receiver. Clocking information is embedded into the data stream. |
| x1, x2, x4 | x1 refers to one PCI Express Lane of basic bandwidth; x2 to a collection of two PCI Express Lanes; etc.. Also referred to as x1, x2 or x4 link. |
| ExpressCard | A PCMCIA standard built on the latest USB 2.0 and PCI Express buses. |
| USB | Universal Serial Bus |
| SATA | Serial AT Attachment: serial-interface standard for hard disks |
| AC '97 / HDA | Audio CODEC (Coder-Decoder) / High Definition Audio |
| LPC | Low Pin-Count Interface: a low speed interface used for peripheral circuits such as Super I/O controllers, which typically combine legacy-device support into a single IC. |
| I ² C Bus | Inter-Integrated Circuit Bus: is a simple two-wire bus with a software-defined protocol that was developed to provide the communications link between integrated circuits in a system. |
| SM Bus | System Management Bus: is a popular derivative of the I ² C-bus. |
| N.C. | Not connected |
| N.A. | Not available |
| T.B.D. | To be determined |

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ETX[®] Concept and XTX[™] Extension

The ETX[®] concept is an off the shelf, multi vendor, Single-Board-Computer that integrates all the core components of a common PC and is mounted onto an application specific baseboard. ETX[®] modules have a standardized form factor of just 95mm x 114mm and have identical pinouts on the four system connectors. The ETX[®] module provides most of the functional requirements for any application. These functions include, but are not limited to, graphics, sound, keyboard/mouse, IDE, Ethernet, parallel, serial and USB ports. Four ruggedized connectors provide the baseboard interface and carry all the I/O signals to and from the ETX[®] module.

Baseboard designers can utilize as little or as many of the I/O interfaces as deemed necessary. The baseboard can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration. Most importantly ETX[®] applications are scalable, which means once a product has been created there is the ability to diversify the product range through the use of different performance class ETX[®] modules. Simply unplug one module and replace it with another, no redesign is necessary.

XTX[™] is an expansion and continuation of the well-established and highly successful ETX[®] standard. XTX[™] offers the newest I/O technologies on this proven form factor. Now that the ISA bus is being used less and less in modern embedded applications congatec AG offers an array of different features on the X2 connector than those currently found on the ETX[®] platform. These features include new serial high speed buses such as PCI Express[™] and Serial ATA[®]. All other signals found on connectors X1, X3, and X4 remain the same in accordance to the ETX[®] standard (Rev. 2.7) and therefore will be completely compatible. If the embedded PC application still requires the ISA bus then an ISA bridge can be implemented on the application specific baseboard or the readily available LPC bus located on the XTX[™] module may be used. Please contact congatec technical support for details.

Lead-Free Designs (RoHS)

As of July 2006 all electronic products are required to be environmentally friendly. In future, many of the currently available embedded computer modules will not be offered as lead-free variants. For this reason all congatec AG designs are created from lead-free components and are completely RoHS compliant. This makes congatec AG products ideal lead-free substitutes for new and existing designs.

Certification

congatec AG is certified to DIN EN ISO 9001:2000 standard.



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2 Specifications

2.1 Mechanical Dimensions

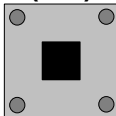
- 294.0mm x 244.0mm
- Height approx. 44mm

2.2 Power Supply

The XTX Evaluation baseboards can be used with standard AT (Connector X10) or ATX (Connector X11) power supplies.

When using an ATX power supply, the XTX module will start after the power-on button M9 is pressed. The ATX power supply can also be used in AT mode. In this case the module will start after the power switch on the power supply is turned on.

**Pwr On
(M9)**



**ATX / AT
(X12)**



| Jumper X12 | Configuration |
|------------|----------------------------------|
| 1 - 2 | ATX Power supply |
| 3 - 4 | ATX Power supply runs in AT mode |

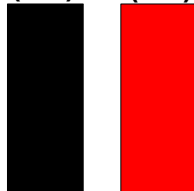


Connector Type

X12: 2.54mm grid jumper.

The XTX Evaluation Baseboard can also be used with 5V power supply (connector M1 and M2). In this case the +12V power supply for Fan and LCD Backlight is not available. The +3.3V used by some devices on the XTX Evaluation Baseboard is generated onboard from the 5V power supply.

**GND
(M1)** **+5V
(M2)**



| Connector | Configuration |
|-----------|---------------|
| M1 | Ground |
| M2 | +5VDC, ±5% |



Connector Type

4mm diameter plug



2.3 CMOS Battery

The XTX Evaluation Baseboard includes a battery that supplies the RTC and CMOS memory of the XTX CPU module. The battery needs to provide a power of 3V. The specified battery type is CR2032.



Warning

Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

To fulfill the requirements of the EN60950, the XTX Evaluation Baseboard incorporates two current-limiting devices (resistor and diode) in the battery power supply path.

2.4 Environmental Specifications

Temperature Operation: 0° to 60°C Storage: -20° to +80°C

Humidity Operation: 10% to 90% Storage: 5% to 95%



Note

The above operating temperatures must be strictly adhered to at all times. The maximum operating temperature refers to any measurable spot on the modules surface.

Humidity specifications are for non-condensing conditions.



3 Connector Description

3.1 XTX Module Connector

3.1.1 Connector X1 (PCI Bus, USB, Audio)

| Pin | Signal | Description | Pin | Signal | Description |
|-----|---------|--------------------------------|-----|----------|--------------------------------------|
| 1 | GND | Power Ground | 2 | GND | Power Ground |
| 3 | PCICLK3 | PCI Clock output 3 | 4 | PCICLK4 | PCI Clock output 4 |
| 5 | GND | Power Ground | 6 | GND | Power Ground |
| 7 | PCICLK1 | PCI Clock output 1 | 8 | PCICLK2 | PCI Clock output 2 |
| 9 | REQ3# | PCI Bus request 3 | 10 | GNT3# | PCI Bus grant 3 |
| 11 | GNT2# | PCI Bus grant 2 | 12 | 3V | Power Supply +3.3VDC |
| 13 | REQ2# | PCI Bus request 2 | 14 | GNT1# | PCI Bus grant 1 |
| 15 | REQ1# | PCI Bus request 1 | 16 | 3V | Power Supply +3.3VDC |
| 17 | GNT0# | PCI Bus grant 0 | 18 | RESERVED | |
| 19 | VCC | Power Supply +5VDC, ±5% | 20 | VCC | Power Supply +5VDC, ±5% |
| 21 | SERIRQ | Serial Interrupt request | 22 | REQ0# | PCI Bus request 0 |
| 23 | AD0 | PCI Address/Data bus line 0 | 24 | 3V | Power Supply +3.3VDC |
| 25 | AD1 | PCI Address/Data bus line 1 | 26 | AD2 | PCI Address/Data bus line 2 |
| 27 | AD4 | PCI Address/Data bus line 4 | 28 | AD3 | PCI Address/Data bus line 3 |
| 29 | AD6 | PCI Address/Data bus line 6 | 30 | AD5 | PCI Address/Data bus line 5 |
| 31 | CBE0# | PCI Bus command/byte enables 0 | 32 | AD7 | PCI Address/Data bus line 7 |
| 33 | AD8 | PCI Address/Data bus line 8 | 34 | AD9 | PCI Address/Data bus line 9 |
| 35 | GND | Power Ground | 36 | GND | Power Ground |
| 37 | AD10 | PCI Address/Data bus line 10 | 38 | AUXAL | Audio Auxiliary input A left |
| 39 | AD11 | PCI Address/Data bus line 11 | 40 | MIC | Microphone input |
| 41 | AD12 | PCI Address/Data bus line 12 | 42 | AUXAR | Audio Auxiliary input A right |
| 43 | AD13 | PCI Address/Data bus line 13 | 44 | ASVCC | Analog supply of sound controller |
| 45 | AD14 | PCI Address/Data bus line 14 | 46 | SNDL | Audio Line-Level stereo output left |
| 47 | AD15 | PCI Address/Data bus line 15 | 48 | ASGND | Analog ground of sound controller |
| 49 | CBE1# | PCI Bus command/byte enables 1 | 50 | SNDR | Audio Line-Level stereo output right |
| 51 | VCC | Power Supply +5VDC, ±5% | 52 | VCC | Power Supply +5VDC, ±5% |
| 53 | PAR | PCI Bus parity | 54 | SERR# | PCI Bus system error |
| 55 | GPERR# | PCI Bus grant parity error | 56 | RESERVED | |
| 57 | PME# | PCI Bus power management event | 58 | USB2# | USB Port 2, data - or D- |
| 59 | LOCK# | PCI Bus lock | 60 | DEVSEL# | PCI Bus device select |
| 61 | TRDY# | PCI Bus target ready | 62 | USB3# | USB Port 3, data - or D- |
| 63 | IRDY# | PCI Bus initiator ready | 64 | STOP# | PCI Bus stop |
| 65 | FRAME# | PCI Bus frame | 66 | USB2 | USB Port 2, data + or D+ |
| 67 | GND | Power Ground | 68 | GND | Power Ground |
| 69 | AD16 | PCI Address/Data bus line 16 | 70 | CBE2# | PCI Bus command/byte enables 2 |
| 71 | AD17 | PCI Address/Data bus line 17 | 72 | USB3 | USB Port 3, data + or D+ |
| 73 | AD19 | PCI Address/Data bus line 19 | 74 | AD18 | PCI Address/Data bus line 18 |
| 75 | AD20 | PCI Address/Data bus line 20 | 76 | USB0# | USB Port 0, data - or D- |
| 77 | AD22 | PCI Address/Data bus line 22 | 78 | AD21 | PCI Address/Data bus line 21 |
| 79 | AD23 | PCI Address/Data bus line 23 | 80 | USB1# | USB Port 1, data - or D- |
| 81 | AD24 | PCI Address/Data bus line 24 | 82 | CBE3# | PCI Bus command/byte enables 3 |
| 83 | VCC | Power Supply +5VDC, ±5% | 84 | VCC | Power Supply +5VDC, ±5% |
| 85 | AD25 | PCI Address/Data bus line 25 | 86 | AD26 | PCI Address/Data bus line 26 |
| 87 | AD28 | PCI Address/Data bus line 28 | 88 | USB0 | USB Port 0, data + or D+ |
| 89 | AD27 | PCI Address/Data bus line 27 | 90 | AD29 | PCI Address/Data bus line 29 |
| 91 | AD30 | PCI Address/Data bus line 30 | 92 | USB1 | USB Port 1, data + or D+ |
| 93 | PCIRST# | PCI Bus reset | 94 | AD31 | PCI Address/Data bus line 31 |
| 95 | INTC# | PCI Bus interrupt C | 96 | INTD# | PCI Bus interrupt D |
| 97 | INTA# | PCI Bus interrupt A | 98 | INTB# | PCI Bus interrupt B |
| 99 | GND | Power Ground | 100 | GND | Power Ground |

3.1.2 Connector X2 (PCIe, SATA, USB, ExpressCard, AC'97/HDA, LPC, ...)



| Pin | Signal | Description | Pin | Signal | Description |
|-----|---------------|--|-----|-----------|--|
| 1 | GND | Power Ground | 2 | GND | Power Ground |
| 3 | PCIE_CLK_REF+ | PCI Express Reference Clock, positive differential line | 4 | SATA0_RX+ | Serial ATA channel 0, receive input, positive diff. line |
| 5 | PCIE_CLK_REF- | PCI Express Reference Clock, negative differential line | 6 | SATA0_RX- | Serial ATA channel 0, receive input, negative diff. line |
| 7 | GND | Power Ground | 8 | GND | Power Ground |
| 9 | PCIE3_TX+ | PCI Express lane 3, transmit output, positive line | 10 | SATA0_TX- | Serial ATA channel 0, transmit output, negative diff. line |
| 11 | PCIE3_TX- | PCI Express lane 3, transmit output, negative line | 12 | SATA0_TX+ | Serial ATA channel 0, transmit output, positive diff. line |
| 13 | GND | Power Ground | 14 | 5V_SB | Supply of internal suspend circuit |
| 15 | PCIE3_RX+ | PCI Express lane 3, receive input, positive line | 16 | SATA1_RX+ | Serial ATA channel 1, receive input, positive diff. line |
| 17 | PCIE3_RX- | PCI Express lane 3, receive input, negative line | 18 | SATA1_RX- | Serial ATA channel 1, receive input, negative diff. line |
| 19 | VCC | Power Supply +5VDC, ±5% | 20 | 5V_SB | Supply of internal suspend circuit |
| 21 | EXC1_CPPE# | ExpressCard capable card request for slot 2 | 22 | SATA1_TX- | Serial ATA channel 1, transmit output, negative diff. line |
| 23 | EXC1_RST# | ExpressCard Reset for slot 2 | 24 | SATA1_TX+ | Serial ATA channel 1, transmit output, positive diff. line |
| 25 | USBP5 | Universal Serial Bus Port 5, positive differential line | 26 | GND | Power Ground |
| 27 | USBP5# | Universal Serial Bus Port 5, negative differential line | 28 | SATA2_RX+ | Serial ATA channel 2, receive input, positive diff. line |
| 29 | GND | Power Ground | 30 | SATA2_RX- | Serial ATA channel 2, receive input, negative diff. line |
| 31 | PCIE2_TX+ | PCI Express lane 2, transmit output, positive diff. line | 32 | SUS_STAT# | Suspend Status |
| 33 | PCIE2_TX- | PCI Express lane 2, transmit output, negative diff. line | 34 | RESERVED | N.C. |
| 35 | GND | Power Ground | 36 | GND | Power Ground |
| 37 | PCIE2_RX+ | PCI Express lane 2, receive input, positive diff. line | 38 | SATA2_TX- | Serial ATA channel 2, transmit output, negative diff. line |
| 39 | PCIE2_RX- | PCI Express lane 2, receive input, negative diff. line | 40 | SATA2_TX+ | Serial ATA channel 2, transmit output, positive diff. line |
| 41 | EXC0_CPPE# | ExpressCard capable card request for slot 1 | 42 | GND | Power Ground |
| 43 | EXC0_RST# | ExpressCard Reset for slot 1 | 44 | SATA3_RX+ | Serial ATA channel 3, receive input, positive diff. line |
| 45 | USBP4 | Universal Serial Bus Port 4, positive differential line | 46 | SATA3_RX- | Serial ATA channel 3, receive input, negative diff. line |
| 47 | USBP4# | Universal Serial Bus Port 4, negative differential line | 48 | WDTRIG | Watch Dog Trigger input |
| 49 | SLP_S3# | S3 (Suspend to RAM) Sleep Control | 50 | SATALED# | Serial ATA activity LED |
| 51 | VCC | Power Supply +5VDC, ±5% | 52 | VCC | Power Supply +5VDC, ±5% |
| 53 | PCIE1_RX- | PCI Express lane 1, receive input, negative diff. line | 54 | SATA3_TX- | Serial ATA channel 3, transmit output, negative diff. line |
| 55 | PCIE1_RX+ | PCI Express lane 1, receive input, positive diff. line | 56 | SATA3_TX+ | Serial ATA channel 3, transmit output, positive diff. line |
| 57 | GND | Power Ground | 58 | IL_SATA# | Serial ATA Interlock Switch Input |
| 59 | PCIE1_TX- | PCI Express lane 1, transmit output, negative diff. line | 60 | RESERVED | N.C. |
| 61 | PCIE1_TX+ | PCI Express lane 1, transmit output, positive diff. line | 62 | RESERVED | N.C. |
| 63 | PCE_WAKE# | PCI Express Wake Event | 64 | PCI_GNT#A | Reserved |
| 65 | RESERVED | N.C. | 66 | PCI_REQ#A | Reserved |
| 67 | GND | Power Ground | 68 | GND | Power Ground |
| 69 | PCIE0_RX- | PCI Express channel 0, | 70 | RESERVED | N.C. |

| Pin | Signal | Description | Pin | Signal | Description |
|-----|------------|---|-----|-------------|--|
| | | receive input, negative diff. line | | | |
| 71 | PCIE0_RX+ | PCI Express channel 0, receive input, positive line | 72 | RESERVED | N.C. |
| 73 | GND | Power Ground | 74 | VCC | Power Supply +5VDC, ±5% |
| 75 | PCIE0_TX- | PCI Express channel 0, transmit output, negative line | 76 | RESERVED | N.C. |
| 77 | PCIE0_TX+ | PCI Express channel 0, transmit output, positive line | 78 | RESERVED | N.C. |
| 79 | CODECSET | AC'97/HDA Disable onboard Audio Codec | 80 | VCC | Power Supply +5VDC, ±5% |
| 81 | AC_RST# | AC'97/HDA CODEC Reset | 82 | AC_SDOUT | AC'97/HDA Audio Serial Data Output to CODEC |
| 83 | VCC | Power Supply +5VDC, ±5% | 84 | VCC | Power Supply +5VDC, ±5% |
| 85 | AC_SYNC | AC'97/HDA Serial Bus Synchronization | 86 | AC_SDIN0 | AC'97/HDA Audio Serial Data Input from CODEC0 |
| 87 | AC_SDIN1 | AC'97/HDA Audio Serial Data Input from CODEC1 | 88 | AC_SDIN2 | AC'97/HDA Audio Serial Data Input from CODEC2 |
| 89 | AC_BIT_CLK | AC'97/HDA 12.228 MHz Serial Bit Clock from CODEC | 90 | FAN_TACHOIN | Fan tachometer input |
| 91 | LPC_AD0 | LPC Multiplexed Command, Address and Data line 0 | 92 | FAN_PWMOUT | Fan speed control |
| 93 | LPC_AD1 | LPC Multiplexed Command, Address and Data line 1 | 94 | LPC_FRAME# | LPC Frame: Indicates start of a new or termination of a broken cycle |
| 95 | LPC_AD2 | LPC Multiplexed Command, Address and Data line 2 | 96 | LPC_DRQ0# | LPC Encoded DMA/Bus Master Request line 0 |
| 97 | LPC_AD3 | LPC Multiplexed Command, Address and Data line 3 | 98 | LPC_DRQ1# | LPC Encoded DMA/Bus Master Request line 1 |
| 99 | GND | Power Ground | 100 | GND | Power Ground |

3.1.3 Connector X3 (VGA, LCD, Video, COM1, COM2, LPT/Floppy, IrDA, Mouse, Keyboard)

| Pin | Signal | Description | Pin | Signal | Description |
|-----|---------------|---|-----|-------------------|--|
| 1 | GND | Power Ground | 2 | GND | Power Ground |
| 3 | R | CRT Red channel RGB Analog Video Output | 4 | B | CRT Blue channel RGB Analog Video Output |
| 5 | HSY | CRT Horizontal Synchronization Pulse | 6 | G | CRT Green channel RGB Analog Video Output |
| 7 | VSY | CRT Vertical Synchronization Pulse | 8 | DDCK | CRT Display Data Channel Clock |
| 9 | DETECT# | Panel hot-plug detection | 10 | DDDA | CRT Display Data Channel Data |
| 11 | LCDDO16 / B4* | LVDS channel data line 16 / TTL RGB signal Blue 4 | 12 | LCDDO18 / SHFCLK* | LVDS channel data line 18 / TTL Panel data clock |
| 13 | LCDDO17 / B5* | LVDS channel data line 17 / TTL RGB signal Blue 5 | 14 | LCDDO19 / EN* | LVDS channel data line 19 / TTL Data-enable signal |
| 15 | GND | Power Ground | 16 | GND | Power Ground |
| 17 | LCDDO13 / B1* | LVDS channel data line 13 / TTL RGB signal Blue 1 | 18 | LCDDO15 / B3* | LVDS channel data line 15 / TTL RGB signal Blue 3 |
| 19 | LCDDO12 / B0* | LVDS channel data line 12 / TTL RGB signal Blue 0 | 20 | LCDDO14 / B2* | LVDS channel data line 14 / TTL RGB signal Blue 2 |
| 21 | GND | Power Ground | 22 | GND | Power Ground |
| 23 | LCDDO8 / G2* | LVDS channel data line 8 / TTL RGB signal Green 2 | 24 | LCDDO11 / G5* | LVDS channel data line 11 / TTL RGB signal Green 5 |
| 25 | LCDDO9 / G3* | LVDS channel data line 9 / TTL RGB signal Green 3 | 26 | LCDDO10 / G4* | LVDS channel data line 10 / TTL RGB signal Green 4 |
| 27 | GND | Power Ground | 28 | GND | Power Ground |
| 29 | LCDDO4 / R4* | LVDS channel data line 4 / TTL RGB signal Red 4 | 30 | LCDDO7 / G1* | LVDS channel data line 7 / TTL RGB signal Green 1 |
| 31 | LCDDO5 / R5* | LVDS channel data line 5 / TTL RGB signal Red 5 | 32 | LCDDO6 / G0* | LVDS channel data line 6 / TTL RGB signal Green 0 |
| 33 | GND | Power Ground | 34 | GND | Power Ground |
| 35 | LCDDO1 / | LVDS channel data line 1 / | 36 | LCDDO3 / | LVDS channel data line 3 / |

| Pin | Signal | Description | Pin | Signal | Description |
|-----|-------------------|--|-----|------------------|---|
| | R1* | TTL RGB signal Red 1 | | R3* | TTL RGB signal Red 3 |
| 37 | LCDDO0 / R0* | LVDS channel data line 0 / TTL RGB Signals Red 0 | 38 | LCDDO2 / R2* | LVDS channel data line 2 / TTL RGB signal Red 2 |
| 39 | VCC | Power Supply +5VDC, ±5% | 40 | VCC | Power Supply +5VDC, ±5% |
| 41 | FPDDC_DAT | LCD Display Data Channel Data | 42 | LTGIO0 / VSYNC* | General Purpose I O / Vertical synchronization pulse |
| 43 | FPDDC_CLK | LCD Display Data Channel Clock | 44 | BLON# | Controls display Backlight |
| 45 | BIASON / HSYNC* | Controls display contrast voltage / TTL Horizontal synchronization pulse | 46 | DIGON | Controls display Power |
| 47 | COMP | TV Composite Video or Blue for RGB Video | 48 | Y | TV Luminance for S-Video or Red for RGB Video |
| 49 | SYNC | TV Composite sync for RGB Video | 50 | C | TV Chrominance for S-Video or Green for RGB Video |
| 51 | LPT / FLPY# | Not supported | 52 | RESERVED | N.C. |
| 53 | VCC | Power Supply +5VDC, ±5% | 54 | GND | Power Ground |
| 55 | STB# / RESERVED** | LPC Strobe signal / N.C. | 56 | AFD / DENSEL** | LPT Automatic feed / FLPY Indicates low or high data rate |
| 57 | RESERVED | N.C. | 58 | PD7 / RESERVED** | LPT Data bus D7 / N.C. |
| 59 | IRRX | Infrared Receive | 60 | ERR# / HDSEL#** | LPT error / FLPY Head select |
| 61 | IRTX | Infrared Transmit | 62 | PD6 / RESERVED** | LPT Data bus D6 / N.C. |
| 63 | RXD2 | Data receive for COM2 | 64 | INIT# / DIR#** | LPT Initiate / FLPY Direction |
| 65 | GND | Power Ground | 66 | GND | Power Ground |
| 67 | RTS2# | Request to send for COM2 | 68 | PD5 / RESERVED* | LPT Data bus D5 / N.C. |
| 69 | DTR2# | Data terminal ready for COM2 | 70 | SLIN# / STEP#** | LPT Select / FLPY Motor step |
| 71 | DCD2# | Data carrier detect for COM2 | 72 | PD4 / DSKCHG#** | LPT Data bus D4 / FLPY Disk change |
| 73 | DSR2# | Data set ready for COM2 | 74 | PD3 / RDATA#** | LPT Data bus D3 / FLPY Raw data read |
| 75 | CTS2# | Clear to send for COM2 | 76 | PD2 / WP#** | LPT Data bus D2 / FLPY Write protect signal |
| 77 | TXD2 | Data transmit for COM2 | 78 | PD1 / TRK0#** | LPT Data bus D1 / FLPY Track signal |
| 79 | RI2# | Ring indicator for COM2 | 80 | PD0 / INDEX#** | LPT Data bus D0 / FLPY Index signal |
| 81 | VCC | Power Supply +5VDC, ±5% | 82 | VCC | Power Supply +5VDC, ±5% |
| 83 | RXD1 | Data receive for COM1 | 84 | ACK# / DRV** | LPT Acknowledge / FLPY Drive select |
| 85 | RTS1# | Request to send for COM1 | 86 | BUSI / MOT** | LPT Busy / FLPY Motor select |
| 87 | DTR1# | Data terminal ready for COM1 | 88 | PE / WDATA#** | LPT Paper empty / FLPY Raw write data |
| 89 | DCD1# | Data carrier detect for COM1 | 90 | SLCT / WGATE#** | LPT Power On / FLPY Write enable |
| 91 | DSR1# | Data set ready for COM1 | 92 | MSCLK | Mouse Clock |
| 93 | CTS1# | Clear to send for COM1 | 94 | MSDAT | Mouse Data |
| 95 | TXD1 | Data transmit for COM1 | 96 | KBCLK | Keyboard Clock |
| 97 | RI1# | Ring indicator for COM1 | 98 | KBDAT | Keyboard Data |
| 99 | GND | Power Ground | 100 | GND | Power Ground |

Note



* Configuration for TTL Flat Panel output, otherwise LVDS output.

** Configuration for Floppy output, otherwise LPT output.

3.1.4 Connector X4 (IDE 1, IDE 2, Ethernet, Miscellaneous)



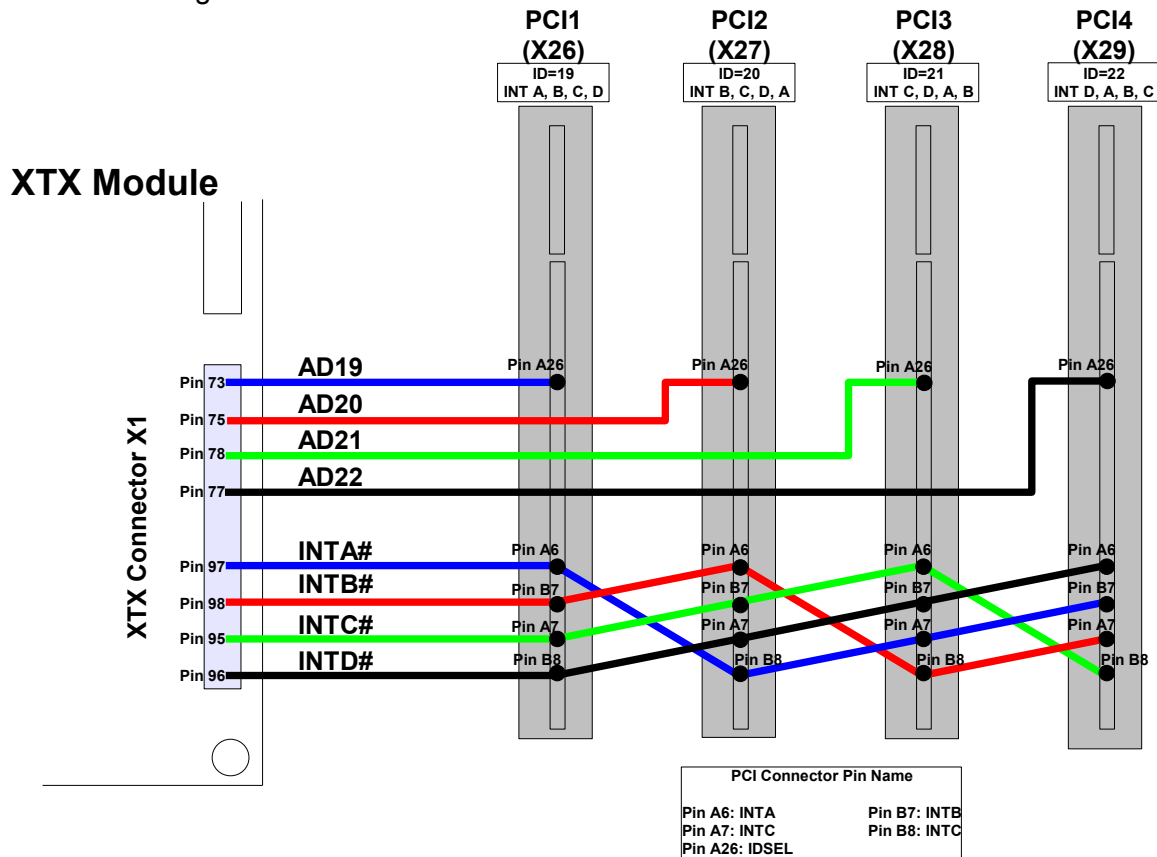
| Pin | Signal | Description | Pin | Signal | Description |
|-----|------------|--|-----|------------|---|
| 1 | GND | Power Ground | 2 | GND | Power Ground |
| 3 | 5V_SB | Supply of internal suspend circuit | 4 | PWGIN | Power good input |
| 5 | PS_ON# | Power Save ON | 6 | SPEAKER | Speaker output |
| 7 | PWRBTN# | Power Button | 8 | BATT | Battery supply |
| 9 | KBINH# | Keyboard inhibit | 10 | LILED# | Ethernet link LED |
| 11 | RSMRST# | Resume Reset input | 12 | ACTLED# | Ethernet activity LED |
| 13 | ROMKBCS# | Internal use. Do not connect | 14 | SPEEDLED# | Ethernet speed LED |
| 15 | EXT_PRG | Internal use. Do not connect | 16 | I2CLK | I ² C Bus Clock |
| 17 | VCC | Power Supply +5VDC, ±5% | 18 | VCC | Power Supply +5VDC, ±5% |
| 19 | OVCR# | USB Over current detection | 20 | GPCS# | General purpose chip select |
| 21 | EXTSMI# | System management interrupt input | 22 | I2DAT | I ² C Bus Data |
| 23 | SMBCLK | SM Bus Clock | 24 | SMBDATA | SM Bus Data |
| 25 | SIDE_CS3# | Secondary IDE chip select 3 | 26 | SMBALRT# | SM Bus Alert input |
| 27 | SIDE_CS1# | Secondary IDE chip select 1 | 28 | DASP_S | Secondary IDE Drive active |
| 29 | SIDE_A2 | Secondary IDE Address line 2 | 30 | PIDE_CS3# | Primary IDE chip select 3 |
| 31 | SIDE_A0 | Secondary IDE Address line 0 | 32 | PIDE_CS1# | Primary IDE chip select 1 |
| 33 | GND | Power Ground | 34 | GND | Power Ground |
| 35 | PDIAG_S | Sec. IDE Master/Slave negotiation | 36 | PIDE_A2 | Primary IDE Address line 2 |
| 37 | SIDE_A1 | Secondary IDE Address line 1 | 38 | PIDE_A0 | Primary IDE Address line 0 |
| 39 | SIDE_INTRQ | Secondary IDE interrupt request | 40 | PIDE_A1 | Primary IDE Address line 1 |
| 41 | BATLOW# | Battery low input | 42 | GPE1# | General purpose power management event input 1 |
| 43 | SIDE_AK# | Secondary IDE DMA acknowledge | 44 | PIDE_INTRQ | Primary IDE interrupt request |
| 45 | SIDE_RDY | Secondary IDE ready | 46 | PIDE_AK# | Primary IDE DMA acknowledge |
| 47 | SIDE_IOR# | Secondary IDE IO read | 48 | PIDE_RDY | Primary IDE ready |
| 49 | VCC | Power Supply +5VDC, ±5% | 50 | VCC | Power Supply +5VDC, ±5% |
| 51 | SIDE_IOW# | Secondary IDE IO write | 52 | PIDE_IOR# | Primary IDE IO read |
| 53 | SIDE_DRQ | Secondary IDE DMA request | 54 | PIDE_IOW# | Primary IDE IO write |
| 55 | SIDE_D15 | Secondary IDE Data line 15 | 56 | PIDE_DRQ | Primary IDE DMA request |
| 57 | SIDE_D0 | Secondary IDE Data line 0 | 58 | PIDE_D15 | Primary IDE Data line 15 |
| 59 | SIDE_D14 | Secondary IDE Data line 14 | 60 | PIDE_D0 | Primary IDE Data line 0 |
| 61 | SIDE_D1 | Secondary IDE Data line 1 | 62 | PIDE_D14 | Primary IDE Data line 14 |
| 63 | SIDE_D13 | Secondary IDE Data line 13 | 64 | PIDE_D1 | Primary IDE Data line 1 |
| 65 | GND | Power Ground | 66 | GND | Power Ground |
| 67 | SIDE_D2 | Secondary IDE Data line 2 | 68 | PIDE_D13 | Primary IDE Data line 13 |
| 69 | SIDE_D12 | Secondary IDE Data line 12 | 70 | PIDE_D2 | Primary IDE Data line 2 |
| 71 | SIDE_D3 | Secondary IDE Data line 3 | 72 | PIDE_D12 | Primary IDE Data line 12 |
| 73 | SIDE_D11 | Secondary IDE Data line 11 | 74 | PIDE_D3 | Primary IDE Data line 3 |
| 75 | SIDE_D4 | Secondary IDE Data line 4 | 76 | PIDE_D11 | Primary IDE Data line 11 |
| 77 | SIDE_D10 | Secondary IDE Data line 10 | 78 | PIDE_D4 | Primary IDE Data line 4 |
| 79 | SIDE_D5 | Secondary IDE Data line 5 | 80 | PIDE_D10 | Primary IDE Data line 10 |
| 81 | VCC | Power Supply +5VDC, ±5% | 82 | VCC | Power Supply +5VDC, ±5% |
| 83 | SIDE_D9 | Secondary IDE Data line 9 | 84 | PIDE_D5 | Primary IDE Data line 5 |
| 85 | SIDE_D6 | Secondary IDE Data line 6 | 86 | PIDE_D9 | Primary IDE Data line 9 |
| 87 | SIDE_D8 | Secondary IDE Data line 8 | 88 | PIDE_D6 | Primary IDE Data line 6 |
| 89 | GPE2# | General purpose power management event input 2 | 90 | CBLID_P# | Primary cable ID for DMA66 or DMA100 transfer modes |
| 91 | RXD# | Ethernet Twisted Pair receive, negative signal | 92 | PIDE_D8 | Primary IDE Data line 8 |
| 93 | RXD | Ethernet Twisted Pair receive, positive signal | 94 | SIDE_D7 | Secondary IDE Data line 7 |
| 95 | TXD# | Ethernet Twisted Pair transmit negative signal | 96 | PIDE_D7 | Primary IDE Data line 7 |
| 97 | TXD | Ethernet Twisted Pair transmit positive signal | 98 | HDRST# | Hard Drive reset |
| 99 | GND | Power Ground | 100 | GND | Power Ground |



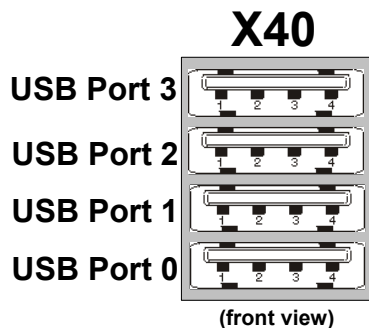
3.2 Subsystems of XTX Connector X1

3.2.1 PCI Bus

This chapter only describes the interrupt routing for the 4 PCI slots used on the XTX Evaluation baseboard. A detailed pin description of the PCI connector can be found in the XTX Design Guide.



3.2.2 Universal Serial Bus (USB)



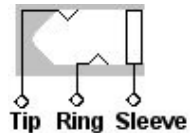
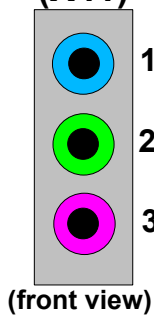
| Pin | Signal |
|-----|--------|
| 1 | +5V |
| 2 | DATA- |
| 3 | DATA+ |
| 4 | GND |



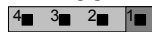
3.2.3 XTX Module Audio

The audio signals provided by the XTX module are available on following connectors.

XTX Audio (X41)



X39



| Stereo Jack 1 | Signal |
|---------------|------------------|
| Tip | Line Input Left |
| Ring | Line Input Right |
| Sleeve | Ground |

| Stereo Jack 2 | Signal |
|---------------|-------------------|
| Tip | Line Output Left |
| Ring | Line Output Right |
| Sleeve | Ground |

| Stereo Jack 3 | Signal |
|---------------|---------------------------|
| Tip | Microphone Input |
| Ring | +5V Microphone Bias Power |
| Sleeve | Analog Ground |

| Pin | Signal |
|-----|------------------|
| 1 | Line Input Left |
| 2 | Analog Ground |
| 3 | Analog Ground |
| 4 | Line Input Right |



Connector Type

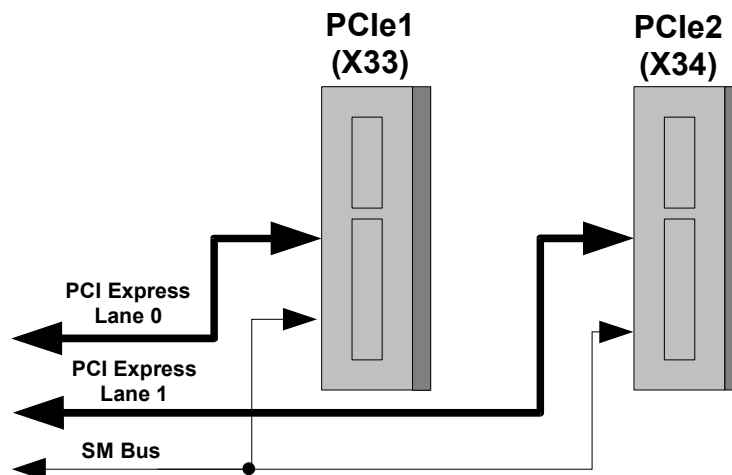
X41: 3.5mm stereo plug,

X39: 4 pin, 1 row 2.54mm grid female.

3.3 Subsystems of XTX Connector X2

3.3.1 PCI Express™ x1 Connectors

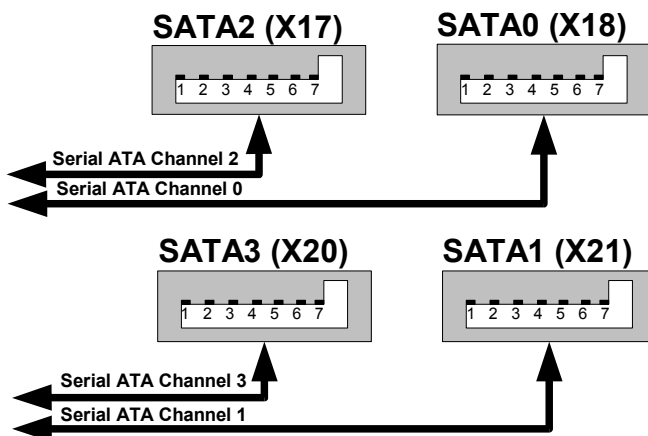
A detailed pin description of the PCI connector can be found in the XTX Design Guide.




 **Note**

The JTAG Interface is not available on the two PCI Express connectors PCIe1 and PCIe2.

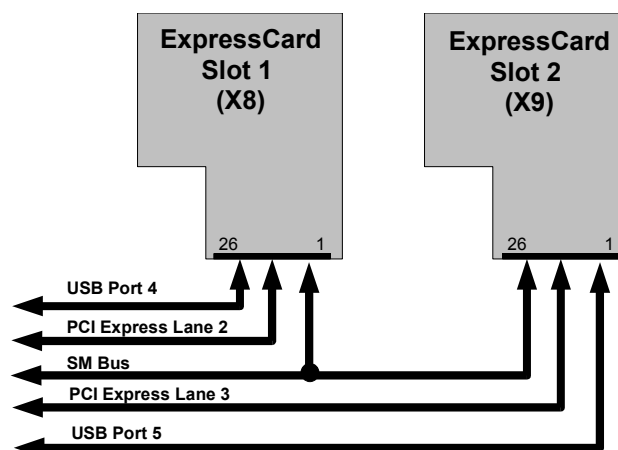
3.3.2 Serial ATA™



| Pin | Signal |
|-----|--------|
| 1 | GND |
| 2 | TX+ |
| 3 | TX- |
| 4 | GND |
| 5 | RX+ |
| 6 | RX- |
| 7 | GND |

3.3.3 ExpressCard™

The XTX Evaluation baseboard supports two ExpressCard slots. A detailed pin description of the ExpressCard connector can be found in the XTX Design Guide.



The XTX Evaluation Baseboard supports ExpressCard/34 and ExpressCard/54 types.

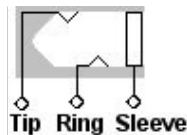
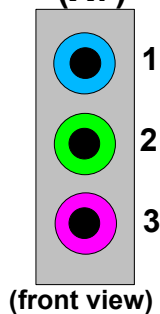


3.3.4 AC'97/HDA Audio

The XTX evaluation baseboard has an AC'97 Audio Codec (VIA VT1616) mounted. The stereo audio output and optical S/PDIF interface of this codec is available on the connectors described below. The Windows driver for this audio codec can be found on the congatec website at www.congatec.com in the 'Products' section under 'Accessories'. There is also a jumper (X15) on the XTX evaluation baseboard that allows you to choose to use either the XTX CPU module's onboard audio codec or the XTX evaluation baseboard's audio codec. You must choose which one to use, both cannot be used at the same time. The XTX CPU module's onboard audio codec is enabled by default. The jumper (X15) configuration is described below.

The XTX evaluation baseboard AC'97 codec can be used in two different modes; either stereo or 5.1 audio mode. The modes can be changed in the audio codec driver.

AC'97 Audio (X7)



| Stereo Jack 1 | Stereo Mode | 5.1 Channel Mode |
|---------------|------------------|---------------------------|
| Tip | Line Input Left | Rear Channel Output Left |
| Ring | Line Input Right | Rear Channel Output Right |
| Sleeve | Ground | Ground |

| Stereo Jack 2 | Stereo Mode | 5.1 Channel Mode |
|---------------|-------------------|----------------------------|
| Tip | Line Output Left | Front Channel Output Left |
| Ring | Line Output Right | Front Channel Output Right |
| Sleeve | Ground | Ground |

| Stereo Jack 3 | Stereo Mode | 5.1 Channel Mode |
|---------------|-------------|---|
| Tip | Microphone* | Center Output |
| Ring | Not used | Low Frequency Effects Output (Sub Woofer) |
| Sleeve | Ground | Ground |



Connector Type

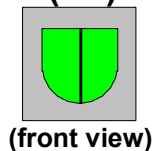
3.5mm stereo plug.



*Note

Only mono microphones can be used on the XTX Evaluation baseboard.

S/PDIF (X5)



Connector Type

Optical Toslink plug.

Jumper (X15)



| Jumper X15 | Configuration |
|------------|--------------------------------------|
| 1 - 2 | XTX evaluation baseboard audio codec |
| 3 - 4 | XTX module CPU audio codec (default) |



Connector Type

X15: 2.54mm grid jumper.



3.3.5 Low Pin Count Bus (LPC)

The X49 connector is intended for internal use. LPC devices must be supported by the CPU BIOS. Please contact the congatec AG support for further information.



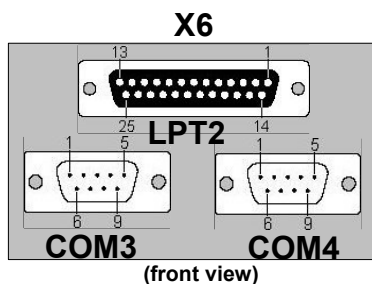
Note

Connector X49 is intended for internal use.

LPC Super I/O device

The XTX Evaluation Baseboard integrates a Super I/O controller that provides additional interfaces such as two serial ports and a parallel port. The Winbond W83627HG controller is connected to the LPC Bus of the XTX module.

The interfaces provided by this Super I/O controller are available on the X6 connector. Serial port COM3 follows the RS232 standard while the signals of COM4 are transformed on the XTX Baseboard to follow the RS485/RS422 standard.



For the pinout of the LPT2 and COM ports 3 and 4, see the table below.



Connector Type

COM: 9 pin D-SUB, female,

LPT: 24 pin D-SUB, male.

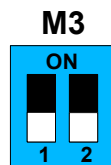
| Pin | LPT2 | COM3 | COM4 |
|-----|---------|------|------|
| 1 | STROBE# | DCD# | TXD+ |
| 2 | PD0 | RXD | |
| 3 | PD1 | TXD | TXD- |
| 4 | PD2 | DTR# | |
| 5 | PD3 | GND | GND |
| 6 | PD4 | DSR | RXD+ |
| 7 | PD5 | RTS# | |
| 8 | PD6 | CTS# | RXD- |
| 9 | PD7 | RI# | |
| 10 | ACK# | | |
| 11 | BUSY | | |
| 12 | PE | | |
| 13 | SEL | | |
| 14 | AUTOFD# | | |
| 15 | ERROR# | | |
| 16 | INIT# | | |
| 17 | SELIN# | | |
| 18 | GND | | |
| 19 | GND | | |
| 20 | GND | | |
| 21 | GND | | |
| 22 | GND | | |
| 23 | GND | | |
| 24 | GND | | |
| 25 | GND | | |

LPC Firmware Hubs



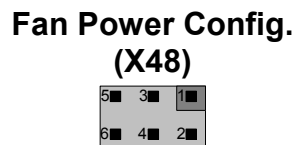
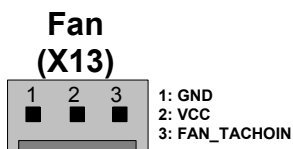
The XTX Evaluation Baseboard offers the possibility to boot the XTX CPU module with a BIOS that is located on the XTX Evaluation Baseboard. This can be very useful when a customized BIOS must be evaluated.

The Evaluation Baseboard includes two 32-lead PLCC sockets for two LPC firmware hubs (FWH1 in socket S1 and FWH2 in socket S2). With the DIP switch M3, the user can configure which hub the XTX module should boot from.



| DIP Switch M3 | | Configuration |
|---------------|-------|-----------------------------------|
| 1 OFF | 2 OFF | XTX Module boots from onboard FWH |
| 1 ON | 2 OFF | XTX Module boots from FWH1 |
| 1 OFF | 2 ON | XTX Module boots from FWH2 |
| 1 ON | 2 ON | Invalid configuration |

3.3.6 Fan Connector and Power Configuration



| Jumper X48 | Configuration |
|------------|---------------|
| 1 - 2 | 12 Volt Fan |
| 3 - 4 | N.C. |
| 5 - 6 | 5 Volt Fan |



Connector Type

X13: 3 pin 2.54mm grid fan connector,

X48: 2.54mm grid jumper.



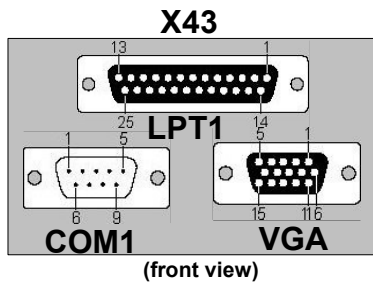
Note

The FAN_TACHOIN signal, that is found on XTX modules and is connected to pin 3 on connector X13 of the conga-XEVAL, must receive two pulses per revolution in order to produce an accurate reading and therefore a two pulse per revolution fan is recommended.



3.4 Subsystems of XTX Connector X3

3.4.1 VGA Output, Serial Ports and Parallel Port / Floppy



| Pin | LPT1 | VGA | COM1 | COM2 (X32) |
|-----|---------|-----------|------|------------|
| 1 | STROBE# | RED | DCD# | DCD# |
| 2 | PD0 | GREEN | RXD | DSR# |
| 3 | PD1 | BLUE | TXD | RXD |
| 4 | PD2 | N.C. | DTR# | RTS# |
| 5 | PD3 | GND | GND | TXD |
| 6 | PD4 | GND | DSR | CTS# |
| 7 | PD5 | GND | RTS# | DTR# |
| 8 | PD6 | GND | CTS# | RI# |
| 9 | PD7 | DDC Power | RI# | GND |
| 10 | ACK# | GND | | +5V |
| 11 | BUSY | N.C. | | |
| 12 | PE | DDC DAT | | |
| 13 | SEL | HSYNC | | |
| 14 | AUTOFD# | VSYNC | | |
| 15 | ERROR# | DDC CLK | | |
| 16 | INIT# | | | |
| 17 | SELIN# | | | |
| 18 | GND | | | |
| 19 | GND | | | |
| 20 | GND | | | |
| 21 | GND | | | |
| 22 | GND | | | |
| 23 | GND | | | |
| 24 | GND | | | |
| 25 | GND | | | |



Connector Type

COM: 9 pin, D-SUB female. LPT: 24 pin, D-SUB male. VGA: 15 pin, high density D-SUB male. X32: 10 pin, 2 row 2.54mm grid female.

The TTL level of the two serial ports supported on the XTX modules is transformed on the XTX Evaluation Baseboard to RS232 level.

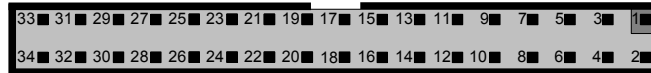
The Parallel Port (LPT1) on the XTX module is shared with the Floppy interface. The user can choose in the system BIOS if the Parallel Port or the Floppy interface should be made available.

congatec XTX Modules do not support the LPT/#FPY signal (XTX connector X3, pin 51). Jumper X30 therefore has no function.

The Floppy signals are available on the standard Floppy connector X36.



Floppy (X36)



| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|-----|--------|-----|--------|-----|--------|-----|---------|
| 1 | GND | 2 | DENSEL | 19 | GND | 20 | STEP# |
| 3 | GND | 4 | N.C. | 21 | GND | 22 | WDATA# |
| 5 | GND | 6 | N.C. | 23 | GND | 24 | WGATE# |
| 7 | GND | 8 | INDEX# | 25 | GND | 26 | TRK0# |
| 9 | GND | 10 | N.C. | 27 | GND | 28 | WP# |
| 11 | GND | 12 | DRV | 29 | GND | 30 | RDATA# |
| 13 | GND | 14 | N.C. | 31 | GND | 32 | HDSEL |
| 15 | GND | 16 | MOT | 33 | GND | 34 | DSKCHG# |
| 17 | GND | 18 | DIR# | | | | |

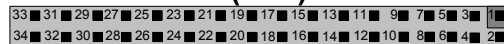


Connector Type

34 pin, 2 row 2.54mm grid female.

3.4.2 Flat Panel Interface

LCD (X31)



| Pin | LVDS output | Digital (TTL) output | Pin | LVDS output | Digital (TTL) output |
|-----|-------------|----------------------|-----|-------------|----------------------|
| 1 | FPDDC_DAT | | 2 | FPDDC_CLK | |
| 3 | N.C. | | 4 | N.C. | |
| 5 | GND | | 6 | LCDDO0 | R0 |
| 7 | LCDDO1 | R1 | 8 | DIGON | |
| 9 | LCDDO2 | R2 | 10 | LCDDO3 | R3 |
| 11 | BLON# | | 12 | LCDDO5 | R5 |
| 13 | LCDDO4 | R4 | 14 | LTGIO0 | VSYNC |
| 15 | LCDDO6 | G0 | 16 | LCDDO7 | G1 |
| 17 | BIASON | HSYNC | 18 | LCDDO9 | G3 |
| 19 | LCDDO8 | G2 | 20 | GND | |
| 21 | LCDDO10 | G4 | 22 | LCDDO11 | G5 |
| 23 | GND | | 24 | LCDDO12 | B0 |
| 25 | LCDDO13 | B1 | 26 | GND | |
| 27 | LCDDO14 | B2 | 28 | LCDDO15 | B3 |
| 29 | GND | | 30 | LCDDO17 | B5 |
| 31 | LCDDO16 | B4 | 32 | DETECT# | |
| 33 | LCDDO19 | EN | 34 | LCDDO18 | SHFTCLK |



Connector Type

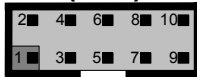
34 pin, 2 row 2mm grid female.



Flat Panel and Backlight Power Supply

The power supply for flat panels and their backlight inverter is available on connector X47.

LCD Power (X47)



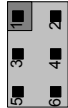
| Pin | Signal | Pin | Signal |
|-----|----------------------------|-----|------------------------------|
| 1 | SW_VDD (1.5A Fuse) | 2 | SW_BACK (0.75A Fuse) |
| 3 | +5V (1.5A Fuse) | 4 | +12V (0.75A Fuse) |
| 5 | DIGON | 6 | BL_ON |
| 7 | Potentiometer Low Terminal | 8 | Potentiometer Wiper Terminal |
| 9 | GND | 10 | GND |



Connector Type

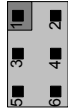
10 pin, 2 row 2.54 mm grid female.

LCD Power Config. (X45)



| Jumper X45 | Configuration |
|------------|------------------|
| 1 - 2 | 5V LCD Voltage |
| 3 - 4 | N.C. |
| 5 - 6 | 3.3V LCD Voltage |

Backlight Power Config. (X46)



| Jumper X46 | Configuration |
|------------|-----------------------|
| 1 - 2 | 12V Backlight Voltage |
| 3 - 4 | N.C. |
| 5 - 6 | 5V Backlight Voltage |



Connector Type

X45 and X46: 2.54mm grid jumper



Note

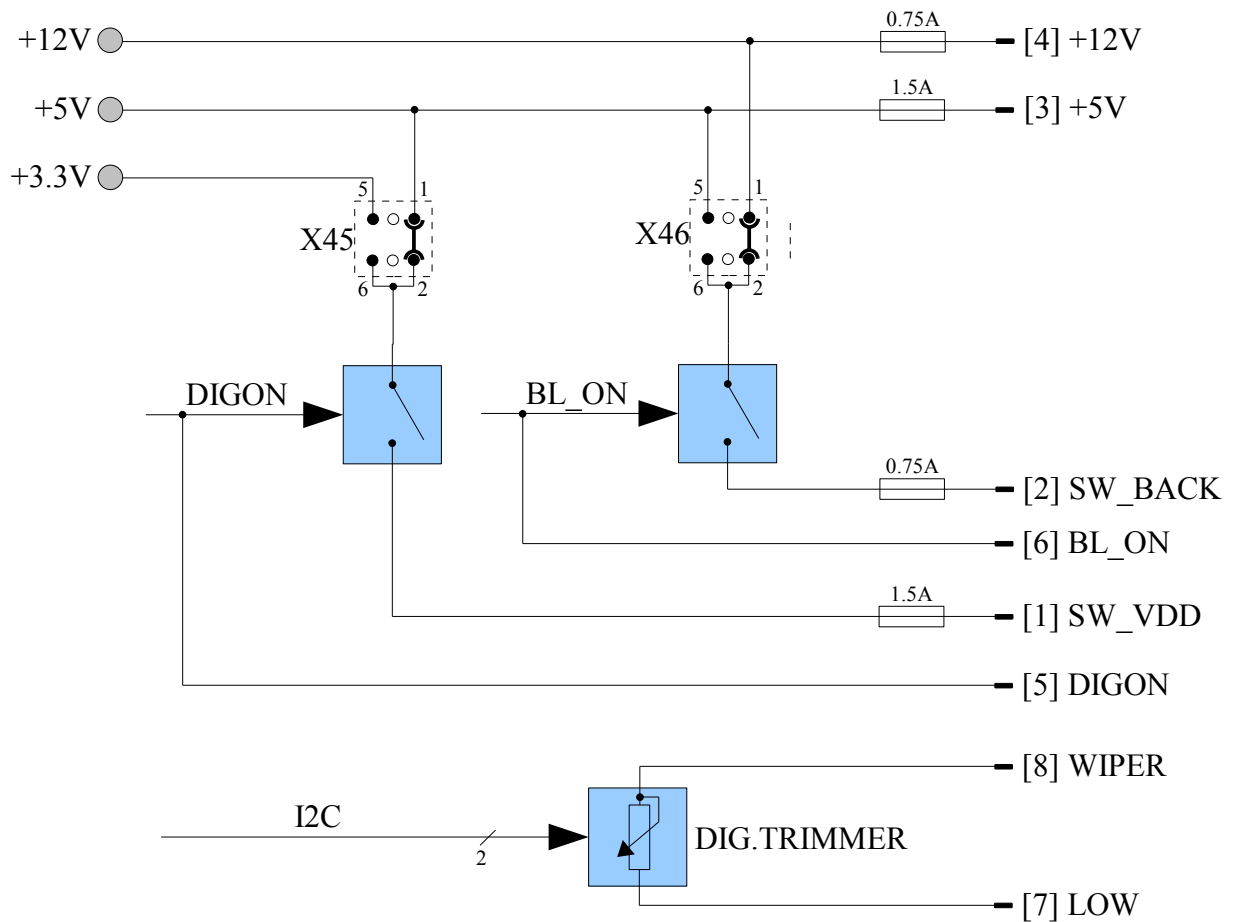
See the following page for information about connection possibilities for the LCD Power X47 connector.



Flat Panel and Backlight Power Supply Connection Possibilities

The following diagram shows the typical connection for powering panel/backlight by either the SW_VDD/SW_BACK signals or by using DIGON/BL_ON for external power switches.

- Signals 1-8 correspond to signals 1-8 found on the X47 connector.
- X45 and X46 represent Jumpers X45 and X46 found on the XTX evaluation baseboard.
- The conga-EVAL baseboard is equipped with a Maxim MAX5434 device.



Flat Panel Configuration Data

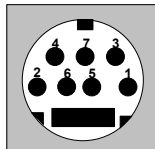
The flat panel configuration data (EPI extended EDID™ 1.3 file) for most common displays is included in the XTX module's system BIOS. The customer also has the possibility to use a customized EPI extended EDID™ file that can be stored in a serial EEPROM located on the XTX Evaluation baseboard (DIL 8 socket U19).

Supported EEPROMs: 24C02, 24C04 and 24C16 at address A0h.



3.4.3 TV Interface

TV-Out (X44)



(front view)

| Pin | Signal | Pin | Signal |
|-----|--------|-----|--------|
| 1 | GND | 2 | GND |
| 3 | Y | 4 | C |
| 5 | GND | 6 | N.C. |
| 7 | COMP | | |



Connector Type

7 pin MINI-DIN male.

The X44 connector is compatible and can be used with the standard 4pin SVIDEO plug. Composite video is not available in this configuration.

When S-Video and Composite Video signals are required, the adapter cable '7-pin to S-VIDEO and RCA' (7-PIN-SV+RCA) from www.svideo.com can be used to make these signals available on standard S-Video and Composite Video connectors.

3.4.4 Serial Infrared Interface (IrDA)

IrDA (X35)



| Pin | Signal | Pin | Signal |
|-----|--------|-----|--------|
| 1 | +5V | 2 | N.C. |
| 3 | IRRX | 4 | GND |
| 5 | IRTX | | |

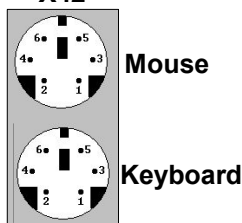


Connector Type

5 pin, 1 row 2.54 mm grid female.

3.4.5 PS/2 Mouse and Keyboard

X42



| Pin | Mouse | Keyboard |
|-----|-------|----------|
| 1 | MSDAT | KBCLK |
| 2 | N.C. | N.C. |
| 3 | GND | GND |
| 4 | +5V | +5V |
| 5 | MSCLK | KBCLK |
| 6 | N.C. | N.C. |



Connector Type

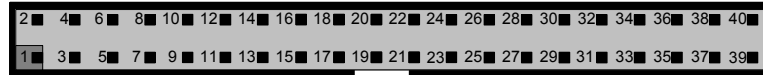
Mouse and Keyboard: 6 pin MINI-DIN female



3.5 Subsystems of XTX Connector X4

3.5.1 IDE

IDE2 (X16)



IDE1 (X19)



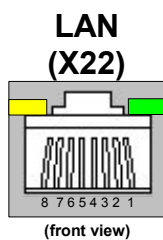
| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|-----|--------|-----|---------|-----|-----------|-----|--|
| 1 | HDRST# | 2 | GND | 21 | IDE_DRQ | 22 | GND |
| 3 | IDE_D7 | 4 | IDE_D8 | 23 | IDE_IOW# | 24 | GND |
| 5 | IDE_D6 | 6 | IDE_D9 | 25 | IDE_IOR# | 26 | GND |
| 7 | IDE_D5 | 8 | IDE_D10 | 27 | IDE_RDY | 28 | CSEL |
| 9 | IDE_D4 | 10 | IDE_D11 | 29 | IDE_ACK | 30 | GND |
| 11 | IDE_D3 | 12 | IDE_D12 | 31 | IDE_INTRQ | 32 | N.C. |
| 13 | IDE_D2 | 14 | IDE_D13 | 33 | IDE_A1 | 34 | CBLID_P# (prim. IDE port) PDIAG_S (sec. IDE port) |
| 15 | IDE_D1 | 16 | IDE_D14 | 35 | IDE_A0 | 36 | IDE_A2 |
| 17 | IDE_D0 | 18 | IDE_D15 | 37 | IDE_CS1 | 38 | IDE_CS3 |
| 19 | GND | 20 | N.C. | 39 | ACTIVITY | 40 | GND |



Connector Type

40 pin, 2 row 2.54mm grid female.

3.5.2 Ethernet



| Pin | Signal | Pin | Signal |
|-----|------------|-----|------------|
| 1 | TX+ | 2 | TX- |
| 3 | RX+ | 4 | Shield GND |
| 5 | Shield GND | 6 | RX- |
| 7 | Shield GND | 8 | Shield GND |

| LED | Description |
|--------|---------------------------------|
| Yellow | Link |
| Green | Activity |
| D28 | Speed Indicator (10 / 100 MBit) |



Connector Type

8 pin RJ45 plug



Note

Connector X23 is intended for internal use.



3.5.3 Feature Connector

Feature (X24)

| | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 2 | 4 | 6 | 8 | 10 | 12 | 14 | 16 | 18 | 20 | 22 | 24 | 26 | 28 | 30 | 32 | 34 | 36 | 38 | 40 |
| 1 | 3 | 5 | 7 | 9 | 11 | 13 | 15 | 17 | 19 | 21 | 23 | 25 | 27 | 29 | 31 | 33 | 35 | 37 | 39 |

| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|-----|-------------------|-----|---------------------|-----|-----------|-----|---------|
| 1 | +5V (750 mA fuse) | 2 | 5V_SB (750 mA fuse) | 21 | GND | 22 | GND |
| 3 | +5V (750 mA fuse) | 4 | Hard Disk Activity | 23 | SUS_STAT# | 24 | EXTSMI# |
| 5 | I2DAT | 6 | SMBCLK | 25 | GND | 26 | GND |
| 7 | I2CLK | 8 | SMBDATA | 27 | WDTRIG | 28 | GPE2# |
| 9 | Internal use | 10 | SERIRQ | 29 | GND | 30 | GND |
| 11 | Internal use | 12 | Reserved | 31 | BATTLOW# | 32 | GPE1# |
| 13 | Reserved | 14 | GPCS# | 33 | GND | 34 | GND |
| 15 | Reserved | 16 | IL_SATA# | 35 | KBINH# | 36 | RSMRST# |
| 17 | GND | 18 | GND | 37 | GND | 38 | GND |
| 19 | Reserved | 20 | SMBALRT# | 39 | PWBTN# | 40 | PWGIN |



Connector Type

40 pin, 2 row 2.54mm grid female.



Note

Connector X25 is intended for internal use.

3.5.4 I²C Bus

The I²C signals are available on the feature connector (X24) described in the previous section.

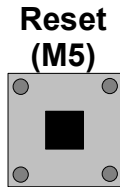
The XTX Evaluation Baseboard includes a socket for an I²C EEPROM (U17) that can be used for test purposes during the system development.

The 8 pin DIP socket on the XTX Evaluation Baseboard can be used with different 2-wire serial EEPROMS (for example 24C04 / 08 / 16 ...) and can be accessed easily by using the I²C control commands implemented in the congatec CGOS API driver. Please refer to the XTX module's User's Guide and CGOS manual for details.



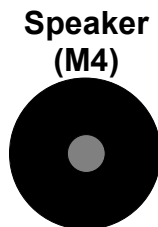
4 Additional Features

4.1 Reset



The XTX module and all connected components will perform a hard reset when this button is pressed. The Reset button is connected to the XTX modules PWGIN signal.

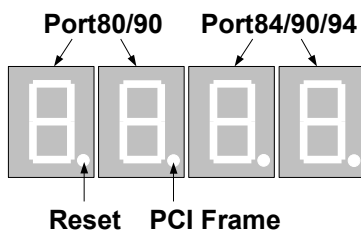
4.2 PC Speaker (Beeper)



The board-mounted speaker provides audible error code (beep code) information during POST. The speaker M4 is connected to the XTX modules SPEAKER signal.

4.3 Debug Display

During the POST (Power On Self Test), the BIOS generates diagnostic progress codes (POST-codes) to different I/O ports (usually port 80h). If the POST fails, execution stops and the last POST code generated is left at the respective port. This code is useful for determining the point where an error occurred.

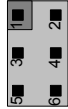


The XTX Evaluation Baseboard decodes these ports and displays their contents on 4 seven-segment displays (D35 to D38). The dots in the first two displays show the state of the Reset and the PCI Frame signals.

A list of the POST codes and associated POST test and initialization routines for the BIOS used on congatec XTX modules is available on: <http://www.congatec.com>.



Debug Config. (X37)



| Jumper X37 | Configuration |
|------------|------------------------------|
| 1 - 2 | Port 80h and port 84h output |
| 3 - 4 | Port 80h and port 90h output |
| 5 - 6 | Port 90h and port 94h output |



Connector Type

2.54mm grid jumper.



Note

Connector X38 is intended for internal use.

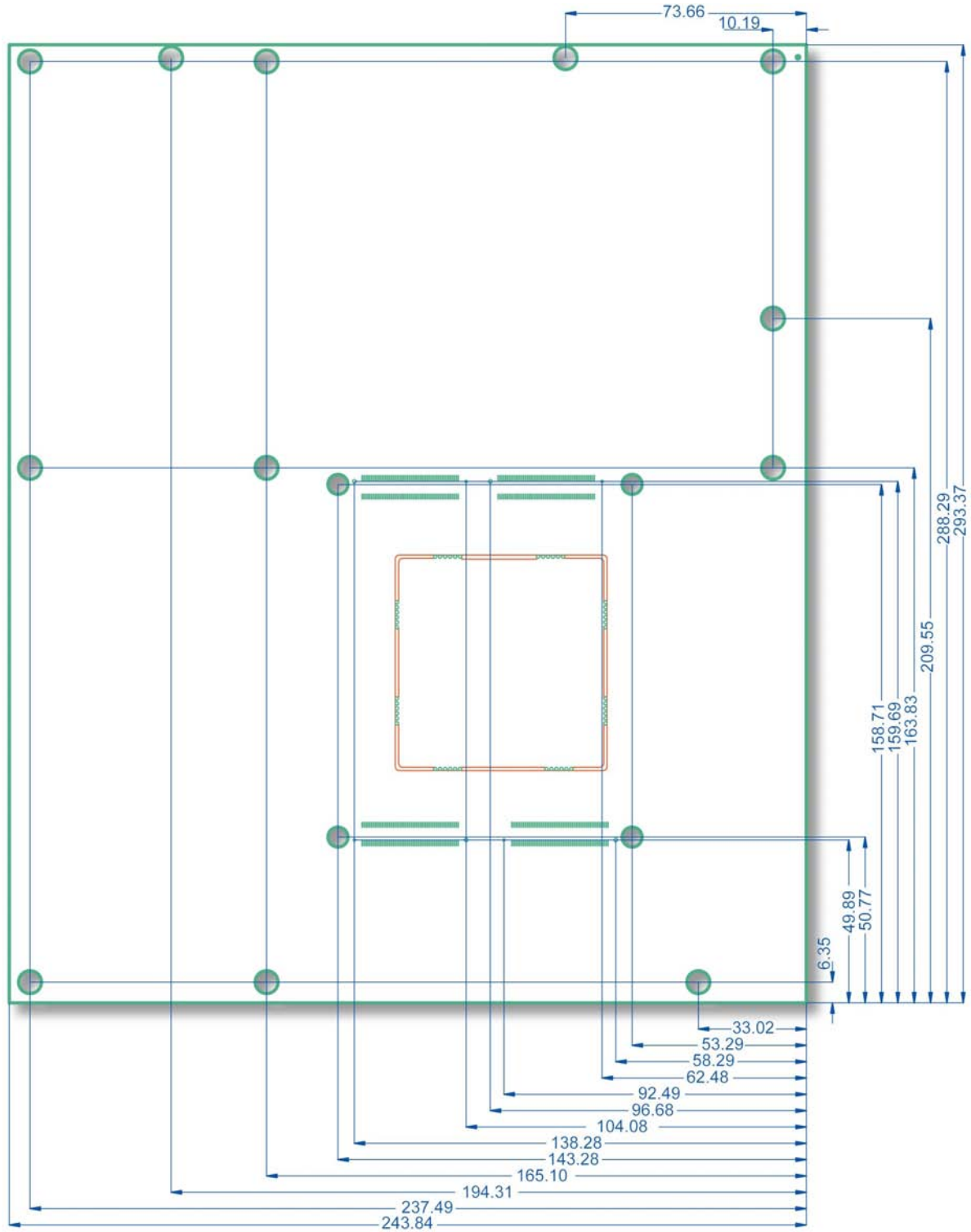
4.4 Ground Test Points

Test Point (TP)



The XTX Evaluation Baseboard provides 4 test points that are connected to Ground Potential (TP1 to TP4). These test points make it easier to connect oscilloscope probes and/or multimeter lines to Ground when performing measurements on the XTX module.

5 Mechanical Drawing conga-XEVAL



6 Industry Specifications

The list below provides links to industry specifications that apply to congatec AG modules.

| Specification | Link |
|---|---|
| XTX Specification 1.0 | http://www.xtx-standard.org/fileadmin/XTX-Spec10.pdf |
| ETX Specification 2.7 | http://www.jumptec.de/product/data/etx/pdf/ETXSpecV2.7.pdf |
| Audio Codec '97 Component Specification, Version 2.3 (AC '97) | http://www.intel.com/design/chipsets/audio/ |
| Low Pin Count Interface Specification, Revision 1.0 (LPC) | http://developer.intel.com/design/chipsets/industry/lpc.htm |
| Universal Serial Bus (USB) Specification, Revision 2.0 | http://www.usb.org/home |
| PCI Specification, Revision 2.2 | http://www.pcisig.com/specifications |
| PCI Express Base Specification, Revision 1.0a | http://www.pcisig.com/specifications |
| Serial ATA Specification, Revision 1.0a | http://www.serialata.org |

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