# ANALOG DEVICES

# 1 nV/√Hz Low Noise
# 210°C Instrumentation Amplifier

Data Sheet

# AD8229

## FEATURES

**Designed and guaranteed for 210°C operation**
**Low noise**
   1 nV/√Hz input noise
   45 nV/√Hz output noise
**High CMRR**
   126 dB CMRR (minimum), G = 100
   80 dB CMRR (minimum) to 5 kHz, G = 1
**Excellent ac specifications**
   15 MHz bandwidth (G = 1)
   1.2 MHz bandwidth (G = 100)
   22 V/µs slew rate
   THD: −130 dBc (1 kHz, G = 1)
**Versatile**
   ±4 V to ±17 V dual supply
   Gain set with single resistor (G = 1 to 1000)
   Specified temperature range
      −40°C to +210°C, SBDIP package
      −40°C to +175°C, SOIC package

## APPLICATIONS

**Down-hole instrumentation**
**Harsh environment data acquisition**
**Exhaust gas measurements**
**Vibration analysis**

## GENERAL DESCRIPTION

The AD8229 is an ultralow noise instrumentation amplifier designed for measuring small signals in the presence of large common-mode voltages and high temperatures.

The AD8229 has been designed for high temperature operation. The process is dielectrically isolated to avoid leakage currents at high temperatures. The design architecture was chosen to compensate for the low $V_{BE}$ voltages at high temperatures.

The AD8229 excels at measuring tiny signals. It delivers industry leading 1 nV/√Hz input noise performance. The high CMRR of the AD8229 prevents unwanted signals from corrupting the acquisition. The CMRR increases as the gain increases, offering high rejection when it is most needed.

The AD8229 is one of the fastest instrumentation amplifiers available. Its current feedback architecture provides high
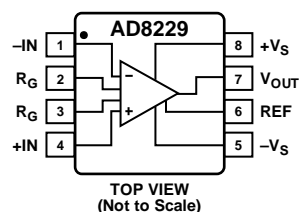
## FUNCTIONAL BLOCK DIAGRAM



Figure 1.
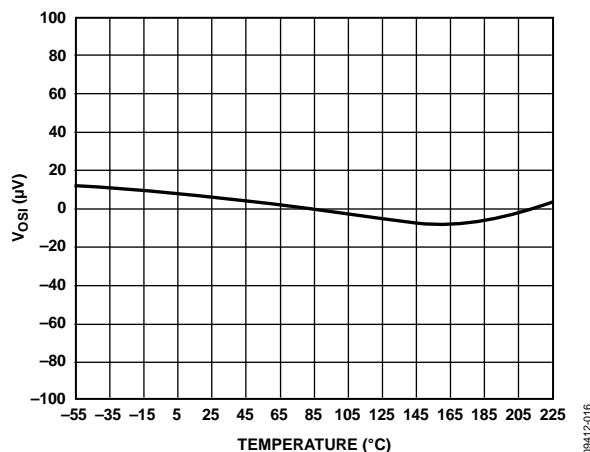


Figure 2. Typical Input Offset vs. Temperature (G = 100)

bandwidth at high gain, for example, 1.2 MHz at G = 100. The design includes circuitry to improve settling time after large input voltage transients. The AD8229 was designed for excellent distortion performance, allowing use in demanding applications such as vibration analysis.

Gain is set from 1 to 1000 with a single resistor. A reference pin allows the user to offset the output voltage. This feature can be useful when interfacing with analog-to-digital converters.

For the most demanding applications, the AD8229 is available in an 8-lead side-brazed ceramic dual in-line package (SBDIP). For space-constrained applications, the AD8229 is available in an 8-lead plastic standard small outline package (SOIC).

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## REVISION HISTORY

# SPECIFICATIONS

$+V_S$ = 15 V, $-V_S$ = −15 V, $V_{REF}$ = 0 V, $T_A$ = 25°C, G = 1, $R_L$ = 10 kΩ, unless otherwise noted.

**Table 1.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| COMMON-MODE REJECTION RATIO (CMRR) | | | | | |
| CMRR DC to 60 Hz with 1 kΩ Source Imbalance | $V_{CM}$ = ±10 V | | | | |
| G = 1 | | 86 | | | dB |
| Temperature Drift | $T_A$ = −40°C to +210°C | | | 300 | nV/V/°C |
| G = 10 | | 106 | | | dB |
| Temperature Drift | $T_A$ = −40°C to +210°C | | | 30 | nV/V/°C |
| G = 100 | | 126 | | | dB |
| Temperature Drift | $T_A$ = −40°C to +210°C | | | 3 | nV/V/°C |
| G = 1000 | $T_A$ = −40°C to +210°C | 134 | | | dB |
| CMRR at 5 kHz | $V_{CM}$ = ±10 V | | | | |
| G = 1 | | 80 | | | dB |
| G = 10 | | 90 | | | dB |
| G = 100 | | 90 | | | dB |
| G = 1000 | | 90 | | | dB |
| VOLTAGE NOISE | $V_{IN}+$, $V_{IN}-$ = 0 V | | | | |
| Spectral Density[1]: 1 kHz | | | | | |
| Input Voltage Noise, $e_{ni}$ | | | 1 | 1.1 | nV/√Hz |
| Output Voltage Noise, $e_{no}$ | | | 45 | 50 | nV/√Hz |
| Peak to Peak: 0.1 Hz to 10 Hz | | | | | |
| G = 1 | | | 2 | | µV p-p |
| G = 1000 | | | 100 | | nV p-p |
| CURRENT NOISE | | | | | |
| Spectral Density: 1 kHz | | | 1.5 | | pA/√Hz |
| Peak to Peak: 0.1 Hz to 10 Hz | | | 100 | | pA p-p |
| VOLTAGE OFFSET | $V_{OS}$ = $V_{OSI}$ + $V_{OSO}$/G | | | | |
| Input Offset, $V_{OSI}$ | | | | 100 | µV |
| Average TC | $T_A$ = −40°C to +210°C | | 0.1 | 1 | µV/°C |
| Output Offset, $V_{OSO}$ | | | | 1000 | µV |
| Average TC | $T_A$ = −40°C to +210°C | | 3 | 10 | µV/°C |
| Offset RTI vs. Supply (PSR) | $V_S$ = ±5 V to ±15 V | | | | |
| G = 1 | $T_A$ = −40°C to +210°C | 86 | | | dB |
| G = 10 | $T_A$ = −40°C to +210°C | 106 | | | dB |
| G = 100 | $T_A$ = −40°C to +210°C | 126 | | | dB |
| G = 1000 | $T_A$ = −40°C to +210°C | 130 | | | dB |
| INPUT CURRENT | | | | | |
| Input Bias Current | | | | 70 | nA |
| High Temperature | $T_A$ = 210°C | | | 200 | nA |
| Input Offset Current | | | | 35 | nA |
| High Temperature | $T_A$ = 210°C | | | 50 | nA |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DYNAMIC RESPONSE | | | | | |
| Small Signal Bandwidth −3 dB | | | | | |
| G = 1 | | | 15 | | MHz |
| G = 10 | | | 4 | | MHz |
| G = 100 | | | 1.2 | | MHz |
| G = 1000 | | | 0.15 | | MHz |
| Settling Time 0.01% | 10 V step | | | | |
| G = 1 | | | 0.75 | | μs |
| G = 10 | | | 0.65 | | μs |
| G = 100 | | | 0.85 | | μs |
| G = 1000 | | | 5 | | μs |
| Settling Time 0.001% | 10 V step | | | | |
| G = 1 | | | 0.9 | | μs |
| G = 10 | | | 0.9 | | μs |
| G = 100 | | | 1.2 | | μs |
| G = 1000 | | | 7 | | μs |
| Slew Rate | | | | | |
| G = 1 to 100 | | | 22 | | V/μs |
| THD (FIRST FIVE HARMONICS) | f = 1 kHz, $R_L$ = 2 kΩ, $V_{OUT}$ = 10 V p-p | | | | |
| G = 1 | | | −130 | | dBc |
| G = 10 | | | −116 | | dBc |
| G = 100 | | | −113 | | dBc |
| G = 1000 | | | −111 | | dBc |
| THD + Noise | f = 1 kHz, $R_L$ = 2 kΩ, $V_{OUT}$ = 10 V p-p, G = 100 | | 0.0005 | | % |
| GAIN[2] | G = 1 + (6 kΩ/$R_G$) | | | | |
| Gain Range | | 1 | | 1000 | V/V |
| Gain Error | $V_{OUT}$ = ±10 V | | | | |
| G = 1 | | | 0.01 | 0.03 | % |
| G = 10 | | | 0.05 | 0.3 | % |
| G = 100 | | | 0.05 | 0.3 | % |
| G = 1000 | | | 0.1 | 0.3 | % |
| Gain Nonlinearity | $V_{OUT}$ = −10 V to +10 V | | | | |
| G = 1 to 1000 | $R_L$ = 10 kΩ | | 2 | | ppm |
| Gain vs. Temperature | | | | | |
| G = 1 | $T_A$ = −40°C to +210°C | | 2 | 5 | ppm/°C |
| G > 10 | $T_A$ = −40°C to +210°C | | | −100 | ppm/°C |
| INPUT | | | | | |
| Impedance (Pin to Ground)[3] | | | 1.5\|\|3 | | GΩ\|\|pF |
| Input Operating Voltage Range[4] | $V_S$ = ±5 V to ±18 V for dual supplies | −$V_S$ + 2.8 | | +$V_S$ − 2.5 | V |
| Over Temperature | $T_A$ = −40°C to +210°C | −$V_S$ + 2.8 | | +$V_S$ − 2.5 | V |
| OUTPUT | | | | | |
| Output Swing, $R_L$ = 2 kΩ | | −$V_S$ + 1.9 | | +$V_S$ − 1.5 | V |
| High Temperature, SBDIP package | $T_A$ = 210°C | −$V_S$ + 1.1 | | +$V_S$ − 1.1 | V |
| High Temperature, SOIC package | $T_A$ = 175°C | −$V_S$ + 1.2 | | +$V_S$ − 1.1 | V |
| Output Swing, $R_L$ = 10 kΩ | | −$V_S$ + 1.8 | | +$V_S$ − 1.2 | V |
| High Temperature, SBDIP package | $T_A$ = 210°C | −$V_S$ + 1.1 | | +$V_S$ − 1.1 | V |
| High Temperature, SOIC package | $T_A$ = 175°C | −$V_S$ + 1.2 | | +$V_S$ − 1.1 | V |
| Short-Circuit Current | | | 35 | | mA |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| REFERENCE INPUT | | | | | |
| $R_{IN}$ | | | 10 | | kΩ |
| $I_{IN}$ | $V_{IN}+, V_{IN}- = 0$ V | | 70 | | µA |
| Voltage Range | | $-V_S$ | | $+V_S$ | V |
| Reference Gain to Output | | | 1 | | V/V |
| Reference Gain Error | | | 0.01 | | % |
| POWER SUPPLY | | | | | |
| Operating Range | | ±4 | | ±17 | V |
| Quiescent Current | | | 6.7 | 7 | mA |
| High Temperature, SBDIP package | $T_A = 210°C$ | | | 12 | mA |
| High Temperature, SOIC package | $T_A = 175°C$ | | | 11 | mA |
| TEMPERATURE RANGE | | | | | |
| For Specified Performance[5] | | | | | |
| SBDIP package | | −40 | | +210 | °C |
| SOIC package | | −40 | | +175 | °C |

[1] Total Voltage Noise = $\sqrt{(e_{ni}^2 + (e_{no}/G)^2)} + e_{RG}^2$. See the Theory of Operation section for more information.

[2] These specifications do not include the tolerance of the external gain setting resistor, $R_G$. For G>1, $R_G$ errors should be added to the specifications given in this table.

[3] Differential and common-mode input impedance can be calculated from the pin impedance: $Z_{DIFF} = 2(Z_{PIN})$; $Z_{CM} = Z_{PIN}/2$.

[4] Input voltage range of the AD8229 input stage only. The input range can depend on the common-mode voltage, differential voltage, gain, and reference voltage. See the Input Voltage Range section for more details.

[5] For the guaranteed operation time at the maximum specified temperature, refer to the Predicted Lifetime vs. Operating Temperature section.

# ABSOLUTE MAXIMUM RATINGS

**Table 2.**

| Parameter | Rating |
|---|---|
| Supply Voltage | ±17 V |
| Output Short-Circuit Current Duration | Indefinite |
| Maximum Voltage at −IN, +IN[1] | ±$V_S$ |
| Differential Input Voltage[1] | |
| Gain ≤ 4 | ±$V_S$ |
| 4 > Gain > 50 | ±50 V/gain |
| Gain ≥ 50 | ±1 V |
| Maximum Voltage at REF | ±$V_S$ |
| Storage Temperature Range | −65°C to +150°C |
| Specified Temperature Range | |
| SBDIP | −40°C to +210°C |
| SOIC | −40°C to +175°C |
| Maximum Junction Temperature | |
| SBDIP | 245°C |
| SOIC | 200°C |
| ESD | |
| Human Body Model | 4 kV |
| Charge Device Model | 1.5 kV |
| Machine Model | 200 V |

[1] For voltages beyond these limits, use input protection resistors. See the Theory of Operation section for more information.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## PREDICTED LIFETIME VS. OPERATING TEMPERATURE

Comprehensive reliability testing is performed on the AD8229. Product lifetimes at extended operating temperature are obtained using high temperature operating life (HTOL). Lifetimes are predicted from the Arrhenius equation, taking into account potential design and manufacturing failure mechanism assumptions. HTOL is performed to JEDEC JESD22-A108. A minimum of three wafer fab and assembly lots are processed through HTOL at the maximum operating temperature. Comprehensive reliability testing is performed on all Analog Devices, Inc., high temperature (HT) products.
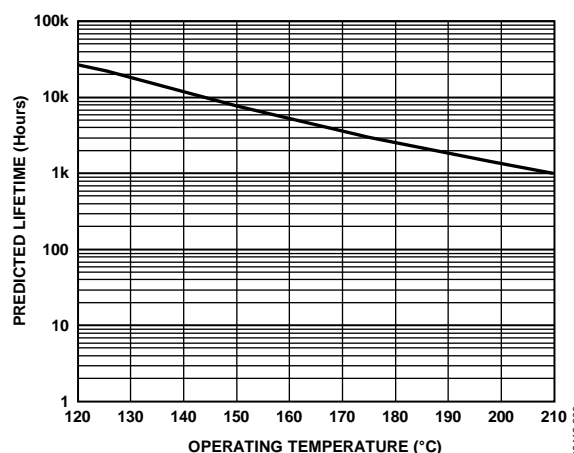


Figure 3. Predicted Lifetime vs. Operating Temperature

Refer to the AD8229 Predicted Lifetime vs. Operating Temperature document for the most up-to-date reliability data.

## THERMAL RESISTANCE

$\theta_{JA}$ is specified for a device in free air using a 4-layer JEDEC printed circuit board (PCB).

**Table 3.**

| Package Type | $\theta_{JA}$ | Unit |
|---|---|---|
| 8-Lead SBDIP | 100 | °C/W |
| 8-Lead SOIC | 121 | °C/W |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

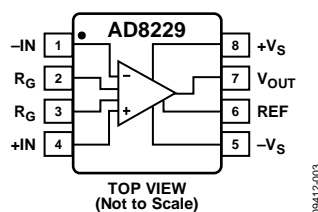# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



*Figure 4. Pin Configuration*

**Table 4. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | −IN | Negative Input Terminal. |
| 2, 3 | $R_G$ | Gain Setting Terminals. Place resistor across the $R_G$ pins to set the gain. $G = 1 + (6\ k\Omega/R_G)$. |
| 4 | +IN | Positive Input Terminal. |
| 5 | $-V_S$ | Negative Power Supply Terminal. |
| 6 | REF | Reference Voltage Terminal. Drive this terminal with a low impedance voltage source to level-shift the output. |
| 7 | $V_{OUT}$ | Output Terminal. |
| 8 | $+V_S$ | Positive Power Supply Terminal. |

# TYPICAL PERFORMANCE CHARACTERISTICS

T = 25°C, $V_S$ = ±15, $V_{REF}$ = 0, $R_L$ = 2 kΩ, unless otherwise noted.
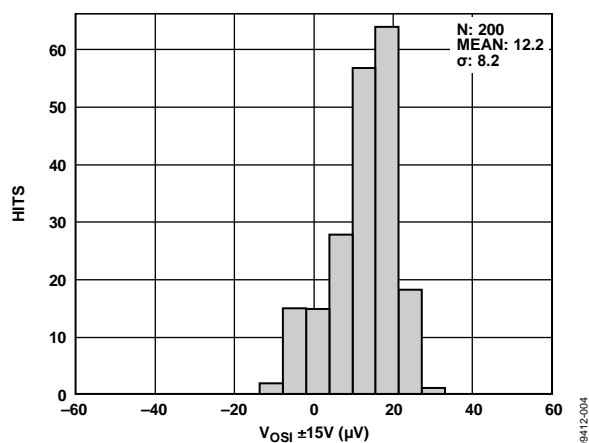


*Figure 5. Typical Distribution of Input Offset Voltage*



*Figure 6. Typical Distribution of Output Offset Voltage*



*Figure 7. Typical Distribution of Input Bias Current*



*Figure 8. Typical Distribution of Input Offset Current*



*Figure 9. Typical Distribution of Common Mode Rejection, G = 1*
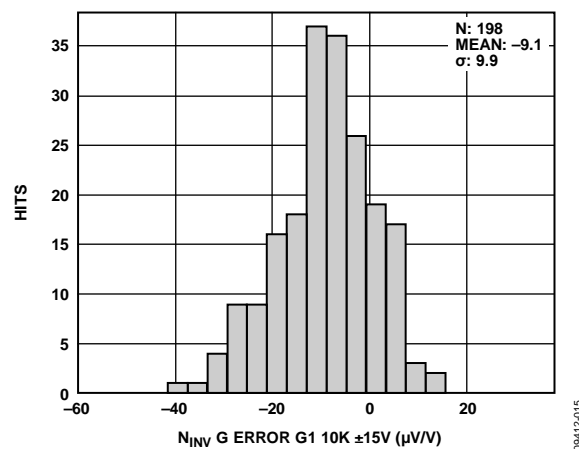


*Figure 10. Typical Distribution of Gain Error, G = 1*
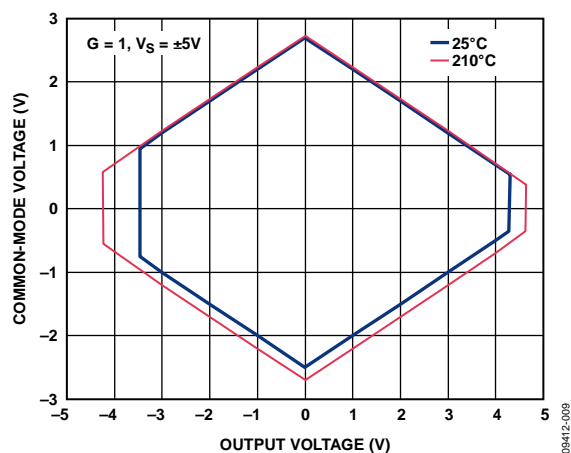
Figure 11. Input Common-Mode Voltage vs. Output Voltage, Dual Supply, $V_S = \pm5$ V; G = 1



Figure 12. Input Common-Mode Voltage vs. Output Voltage, Dual Supply, $V_S = \pm12$ V; G = 1



Figure 13. Input Common-Mode Voltage vs. Output Voltage, Dual Supply, $V_S = \pm15$ V; G = 1



Figure 14. Input Common-Mode Voltage vs. Output Voltage, Dual Supply, $V_S = \pm5$ V; G = 100



Figure 15. Input Common-Mode Voltage vs. Output Voltage, Dual Supply, $V_S = \pm12$ V; G = 100
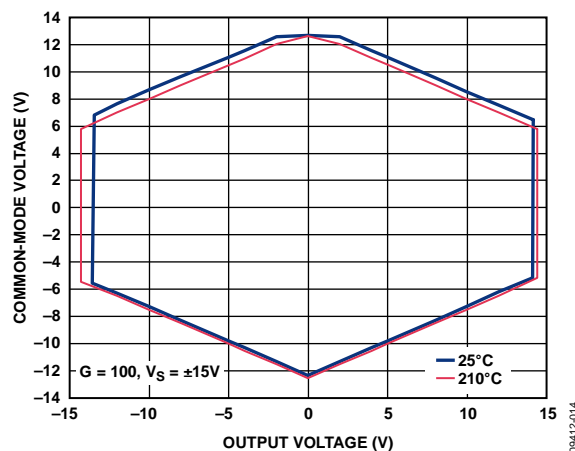


Figure 16. Input Common-Mode Voltage vs. Output Voltage, Dual Supply, $V_S = \pm15$ V; G = 100
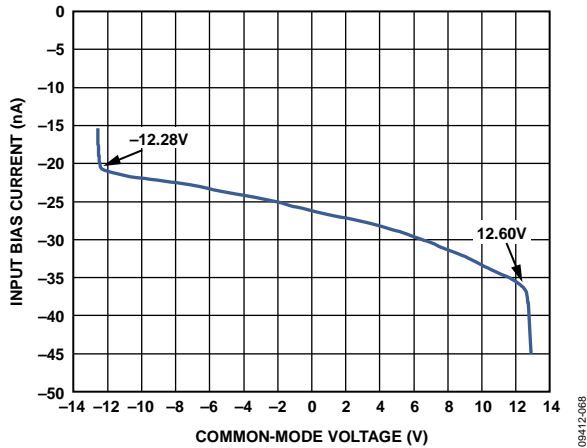
*Figure 17. Input Bias Current vs. Common-Mode Voltage*
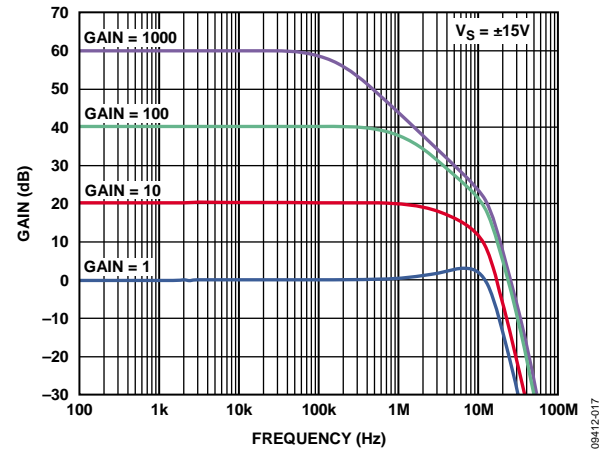


*Figure 20. Gain vs. Frequency*
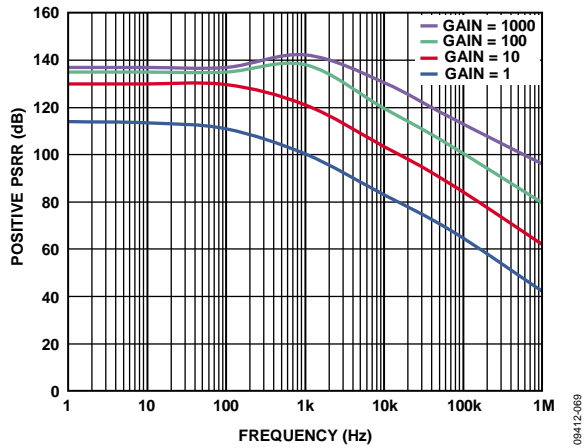


*Figure 18. Positive PSRR vs. Frequency*
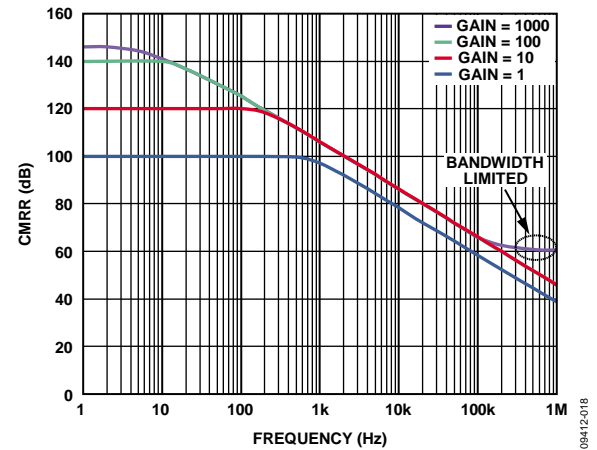


*Figure 21. CMRR vs. Frequency*
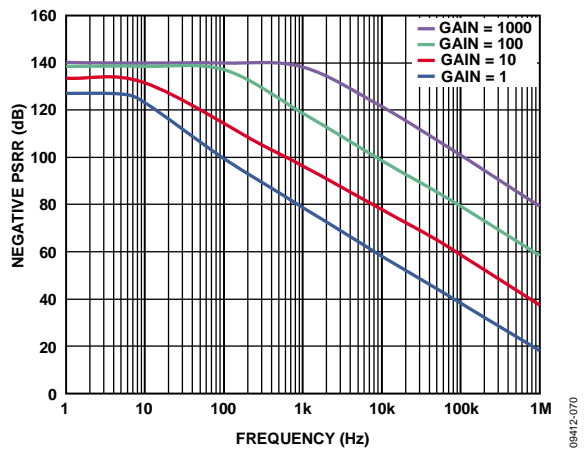


*Figure 19. Negative PSRR vs. Frequency*
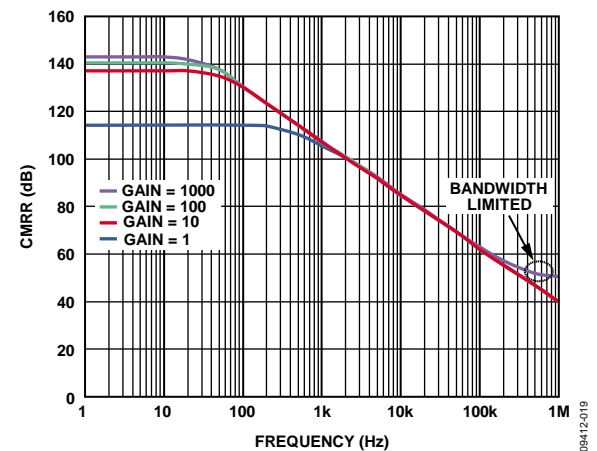


*Figure 22. CMRR vs. Frequency, 1 kΩ Source Imbalance*

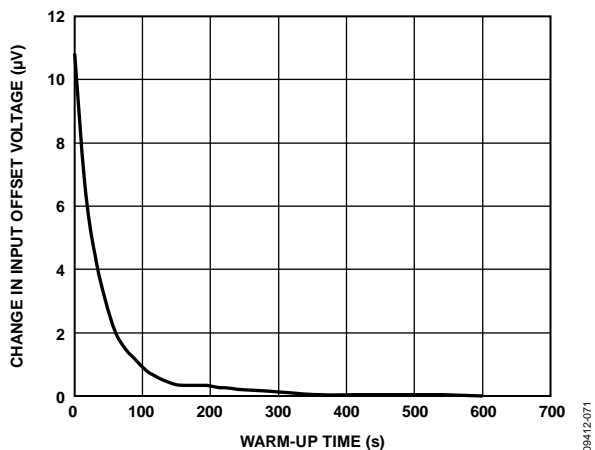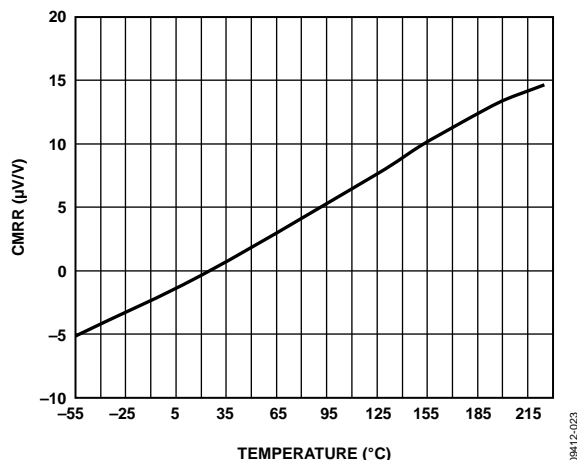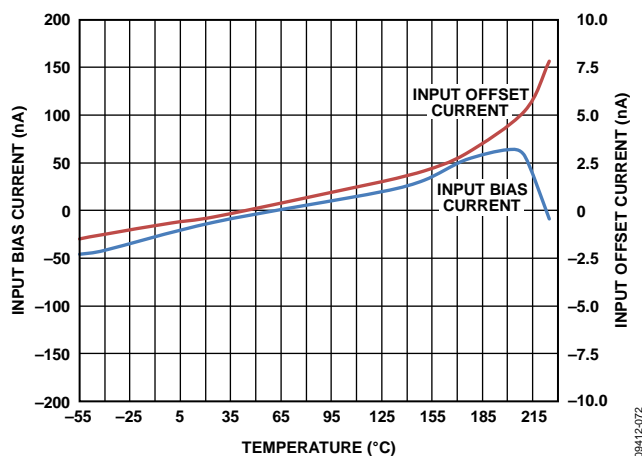*Figure 23. Change in Input Offset Voltage (V$_{OSI}$) vs. Warm-Up Time*



*Figure 24. Input Bias Current and Input Offset Current vs. Temperature*



*Figure 25. Gain Error vs. Temperature, G = 1, Normalized at 25°C*



*Figure 26. CMRR vs. Temperature, G = 1, Normalized at 25°C*



*Figure 27. Supply Current vs. Temperature, G = 1*
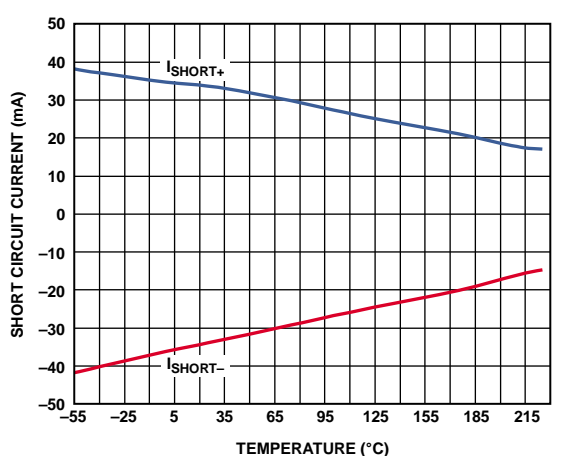


*Figure 28. Short-Circuit Current vs. Temperature, G = 1*
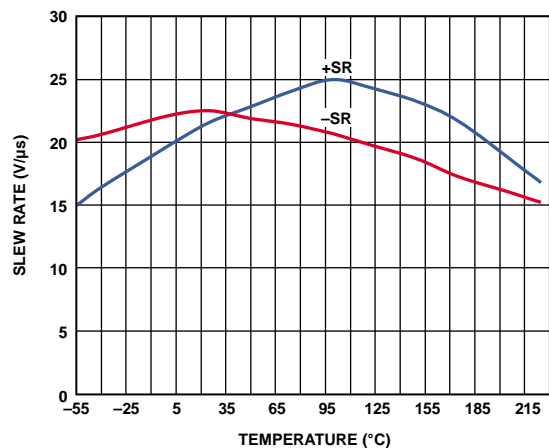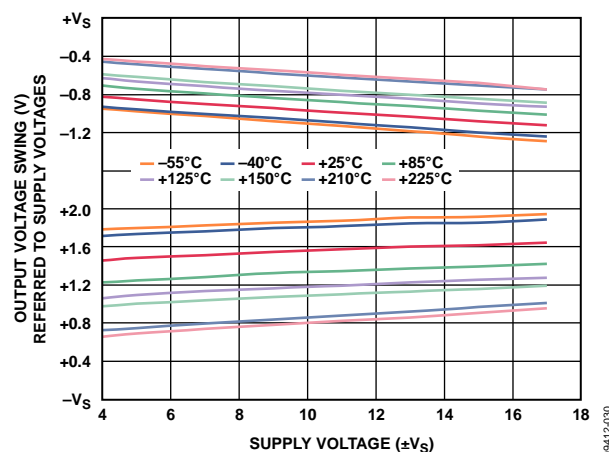
Figure 29. Slew Rate vs. Temperature, $V_S = \pm 15\ V$, $G = 1$
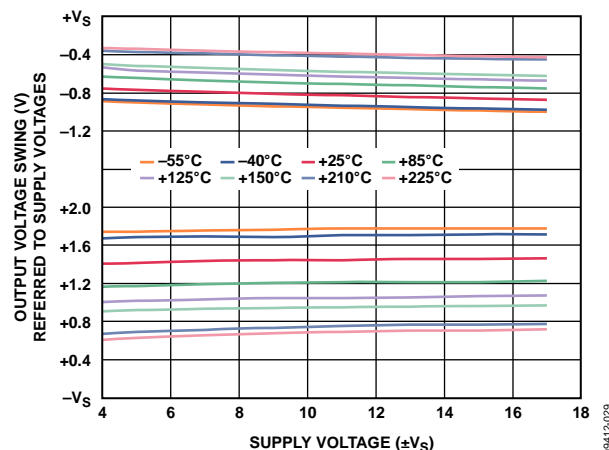


Figure 32. Output Voltage Swing vs. Supply Voltage, $R_L = 10\ k\Omega$
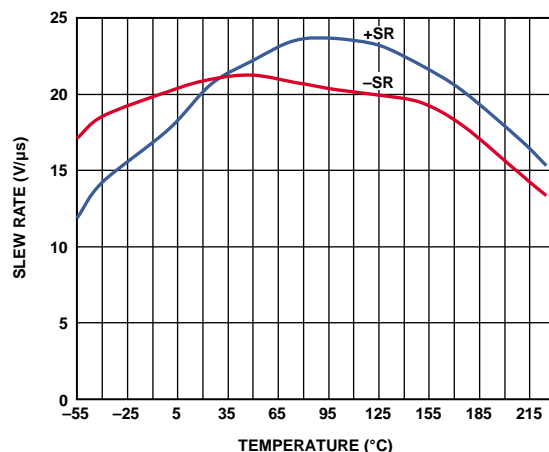


Figure 30. Slew Rate vs. Temperature, $V_S = \pm 5\ V$, $G = 1$



Figure 33. Output Voltage Swing vs. Supply Voltage, $R_L = 2\ k\Omega$
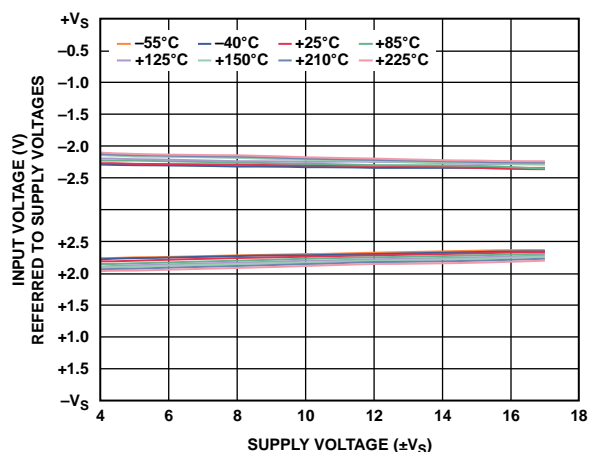


Figure 31. Input Voltage Limit vs. Supply Voltage



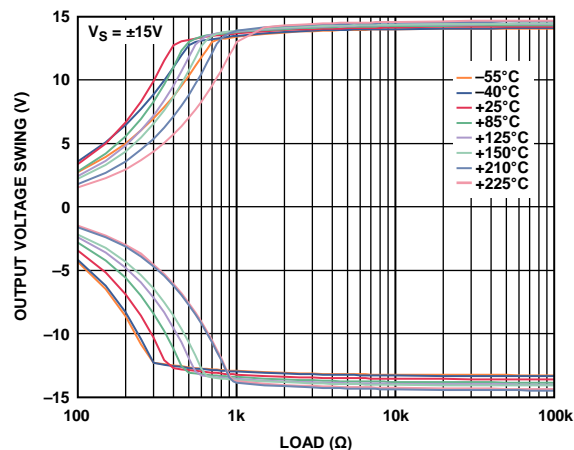Figure 34. Output Voltage Swing vs. Load Resistance
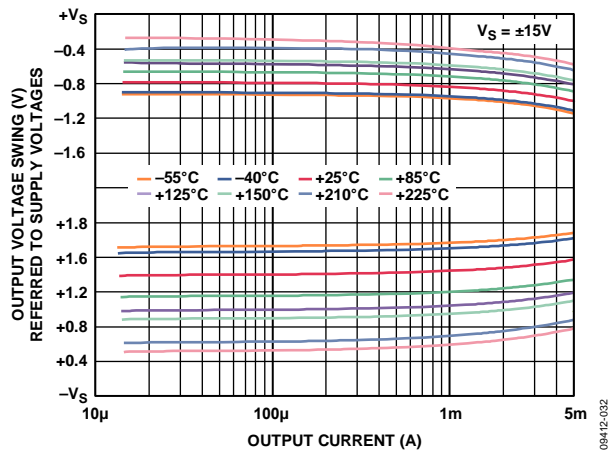
Figure 35. Output Voltage Swing vs. Output Current



Figure 36. Gain Nonlinearity, G = 1, $R_L$ = 10 kΩ
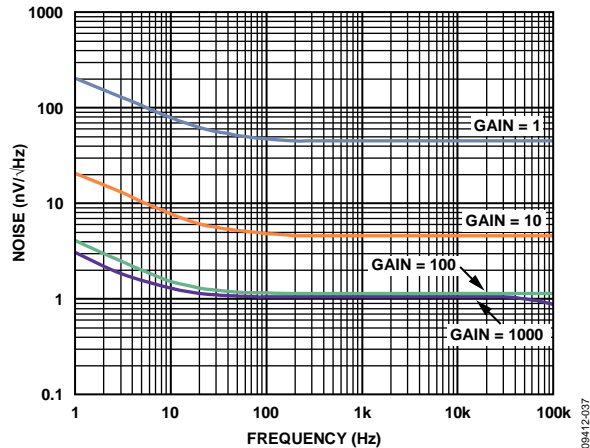


Figure 37. Gain Nonlinearity, G = 1000, $R_L$ = 10 kΩ



Figure 38. Voltage Noise Spectral Density vs. Frequency



Figure 39. 0.1 Hz to 10 Hz RTI Voltage Noise, G = 1, G = 1000
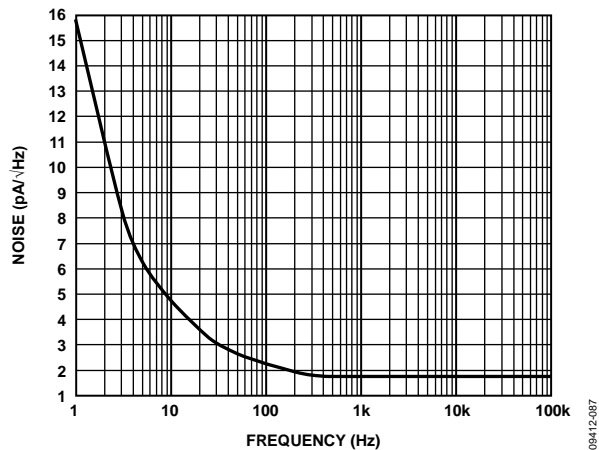


Figure 40. Current Noise Spectral Density vs. Frequency
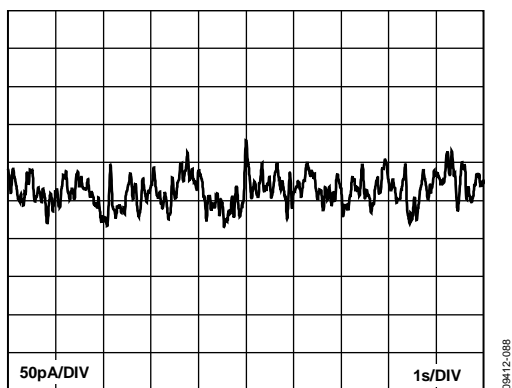
Figure 41. 1 Hz to 10 Hz Current Noise
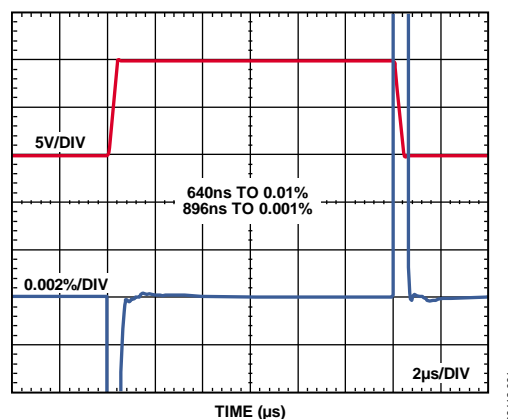


Figure 44. Large Signal Pulse Response and Settling Time (G = 10), 10 V Step, $V_S = \pm15$ V
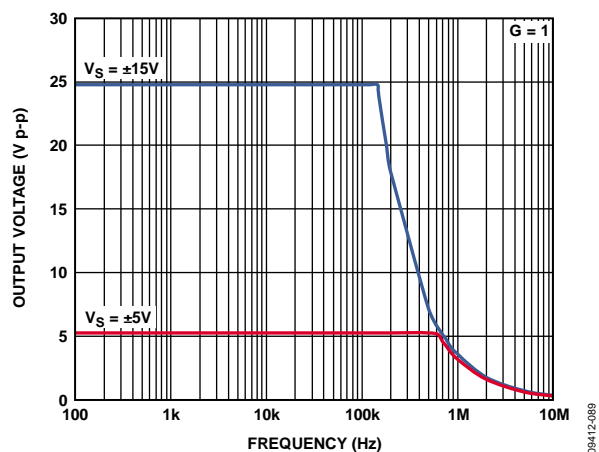


Figure 42. Large Signal Frequency Response
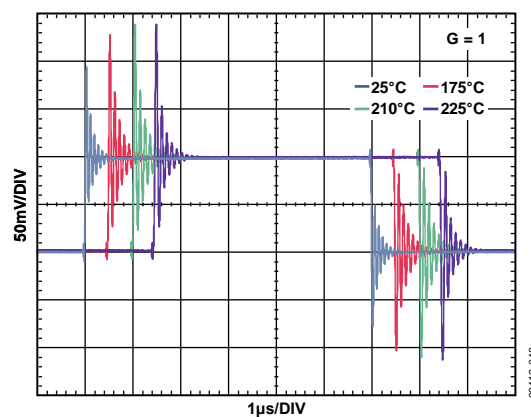


Figure 45. Small Signal Response, G = 1, $R_L$ = 10 kΩ, $C_L$ = 100 pF
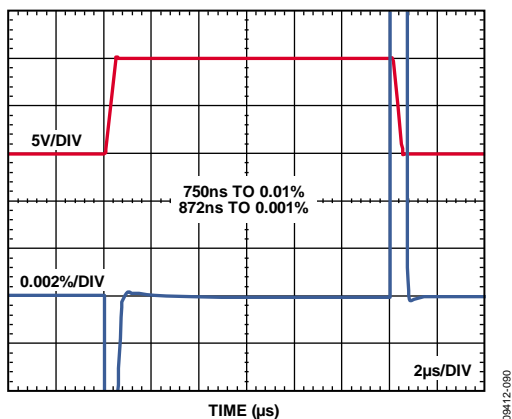


Figure 43. Large Signal Pulse Response and Settling Time (G = 1), 10 V Step, $V_S = \pm15$ V
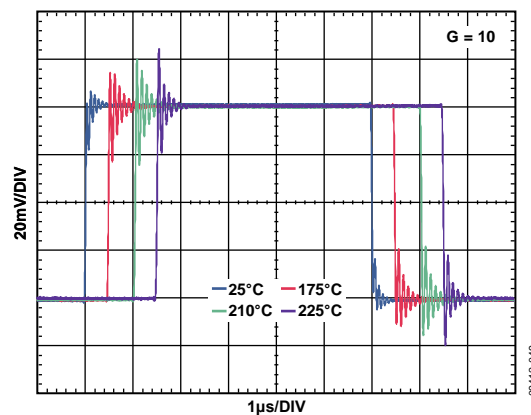


Figure 46. Small Signal Response, G = 10, $R_L$ = 10 kΩ, $C_L$ = 100 pF
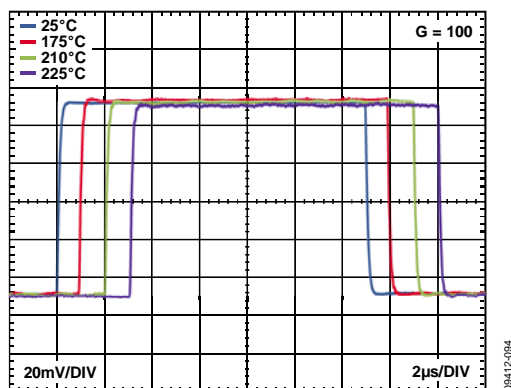
Figure 47. Small Signal Response, G = 100, R_L = 10 kΩ, C_L = 100 pF



Figure 48. Small Signal Response, G = 1000, R_L = 10 kΩ, C_L = 100 pF



Figure 49. Small Signal Response with Various Capacitive Loads, G = 1, R_L = Infinity



Figure 50. Settling Time vs. Step Size, G = 1



Figure 51. Second Harmonic Distortion vs. Frequency, G = 1
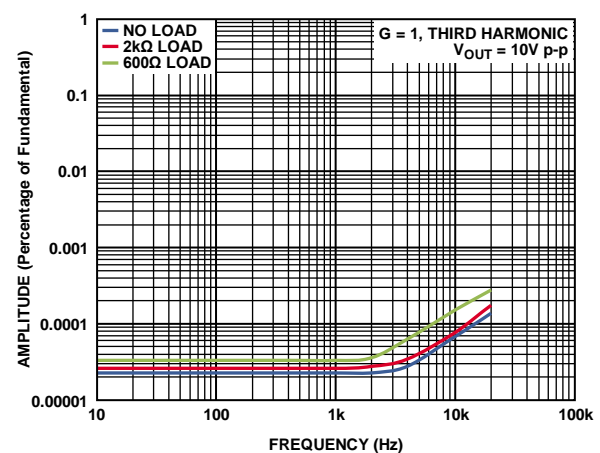


Figure 52. Third Harmonic Distortion vs. Frequency, G = 1
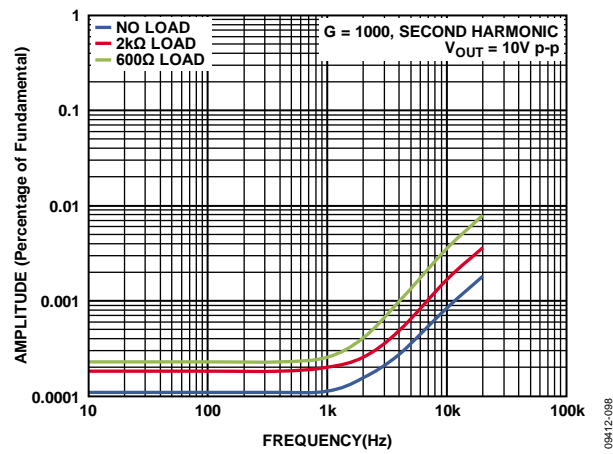
*Figure 53. Second Harmonic Distortion vs. Frequency, G = 1000*
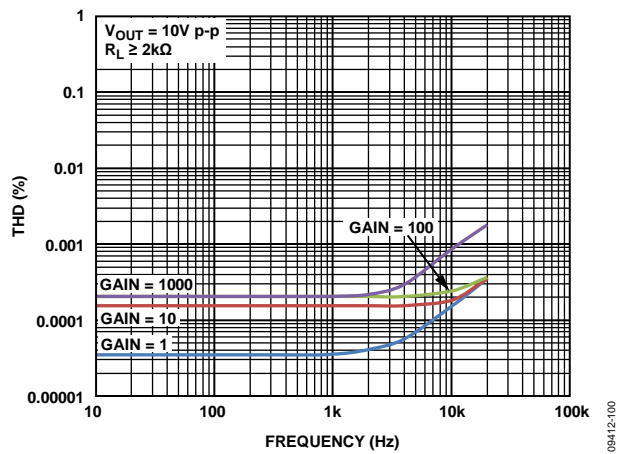


*Figure 55. THD vs. Frequency*
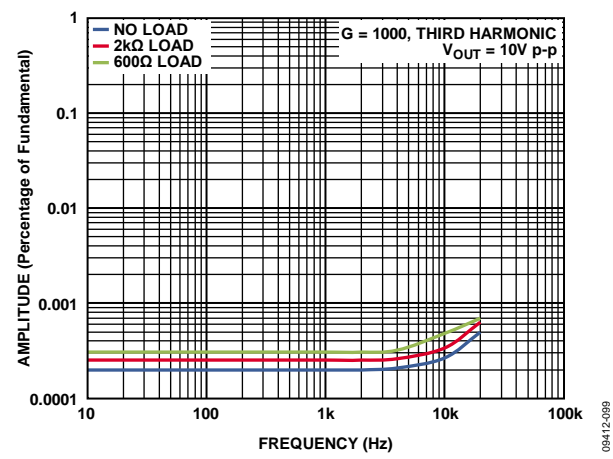


*Figure 54. Third Harmonic Distortion vs. Frequency, G = 1000*

# THEORY OF OPERATION
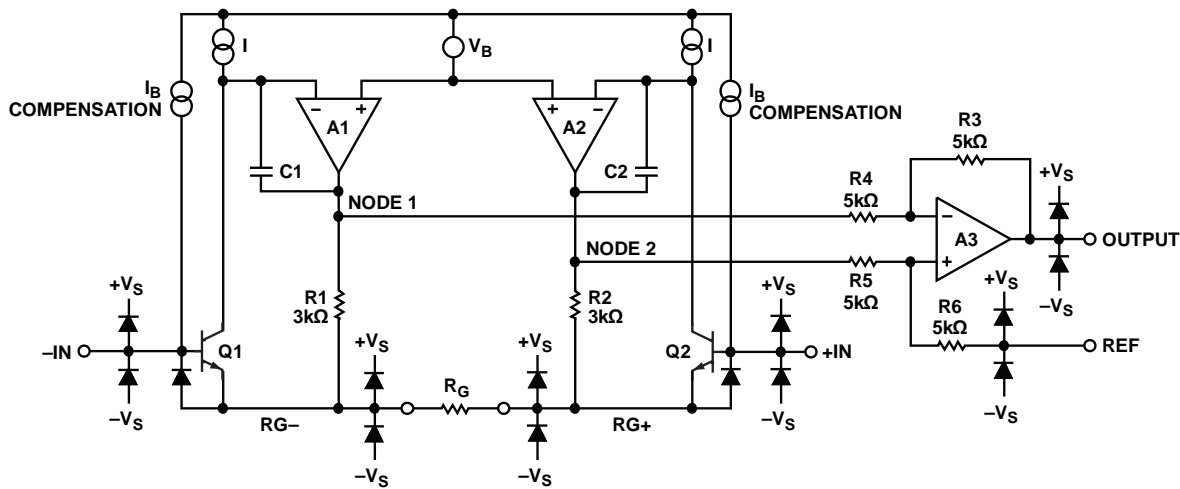


*Figure 56. Simplified Schematic*

## ARCHITECTURE

The AD8229 is based on the classic 3-op-amp topology. This topology has two stages: a preamplifier to provide differential amplification followed by a difference amplifier that removes the common-mode voltage and provides additional amplification. Figure 56 shows a simplified schematic of the AD8229.

The first stage works as follows. To keep its two inputs matched, Amplifier A1 must keep the collector of Q1 at a constant voltage. It does this by forcing RG− to be a precise diode drop from −IN. Similarly, A2 forces RG+ to be a constant diode drop from +IN. Therefore, a replica of the differential input voltage is placed across the gain setting resistor, $R_G$. The current that flows through this resistance must also flow through the R1 and R2 resistors, creating a gained differential signal between the A2 and A1 outputs.

The second stage is a G = 1 difference amplifier, composed of Amplifier A3 and the R3 through R6 resistors. This stage removes the common-mode signal from the amplified differential signal.

The transfer function of the AD8229 is

$$V_{OUT} = G \times (V_{IN+} - V_{IN-}) + V_{REF}$$

where:

$$G = 1 + \frac{6\,k\Omega}{R_G}$$

## GAIN SELECTION

Placing a resistor across the $R_G$ terminals sets the gain of the AD8229, which can be calculated by referring to Table 5 or by using the following gain equation:

$$R_G = \frac{6\,k\Omega}{G-1}$$

**Table 5. Gains Achieved Using 1% Resistors**

| 1% Standard Table Value of $R_G$ (Ω) | Calculated Gain |
|---|---|
| 6.04 k | 1.993 |
| 1.5 k | 5.000 |
| 665 | 10.02 |
| 316 | 19.99 |
| 121 | 50.59 |
| 60.4 | 100.34 |
| 30.1 | 200.34 |
| 12.1 | 496.9 |
| 6.04 | 994.4 |
| 3.01 | 1994.355 |

The AD8229 defaults to G = 1 when no gain resistor is used. The tolerance and gain drift of the $R_G$ resistor should be added to the AD8229's specifications to determine the total gain accuracy of the system. When the gain resistor is not used, gain error and gain drift are minimal.

### $R_G$ Power Dissipation

The AD8229 duplicates the differential voltage across its inputs onto the $R_G$ resistor. The $R_G$ resistor size should be chosen to handle the expected power dissipation.

## REFERENCE TERMINAL

The output voltage of the AD8229 is developed with respect to the potential on the reference terminal. This is useful when the output signal must be offset to a precise midsupply level. For example, a voltage source can be tied to the REF pin to level-shift the output so that the AD8229 can drive a single-supply ADC. The REF pin is protected with ESD diodes and should not exceed either $+V_S$ or $-V_S$ by more than 0.3 V.

For best performance, source impedance to the REF terminal should be kept well below 1 Ω. As shown in Figure 56, the reference terminal, REF, is at one end of a 5 kΩ resistor. Additional impedance at the REF terminal adds to this 5 kΩ resistor and results in amplification of the signal connected to the positive input. The amplification from the additional $R_{REF}$ can be calculated as follows:

$$2(5\text{ k}\Omega + R_{REF})/(10\text{ k}\Omega + R_{REF})$$

Only the positive signal path is amplified; the negative path is unaffected. This uneven amplification degrades CMRR.
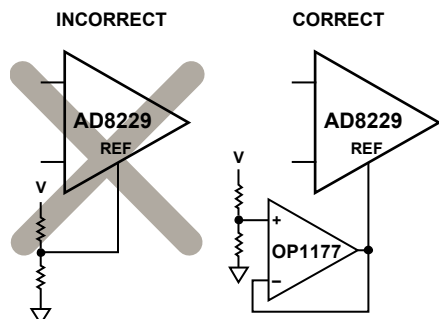


*Figure 57. Driving the Reference Pin*

## INPUT VOLTAGE RANGE

Figure 11 through Figure 16 show the allowable common-mode input voltage ranges for various output voltages and supply voltages. The 3-op-amp architecture of the AD8229 applies gain in the first stage before removing common-mode voltage with the difference amplifier stage. Internal nodes between the first and second stages (Node 1 and Node 2 in Figure 56) experience a combination of a gained signal, a common-mode signal, and a diode drop. This combined signal can be limited by the voltage supplies even when the individual input and output signals are not limited.

## LAYOUT

To ensure optimum performance of the AD8229 at the PCB level, care must be taken in the design of the board layout. The pins of the AD8229 are arranged in a logical manner to aid in this task.
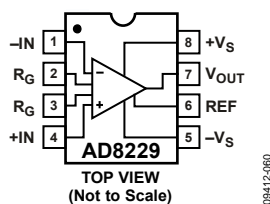


*Figure 58. Pinout Diagram*

### Common-Mode Rejection Ratio over Frequency

Poor layout can cause some of the common-mode signals to be converted to differential signals before reaching the in-amp. Such conversions occur when one input path has a frequency response that is different from the other. To keep CMRR over frequency high, the input source impedance and capacitance of each path should be closely matched. Additional source resistance in the input path (for example, for input protection) should be placed close to the in-amp inputs, which minimizes their interaction with parasitic capacitance from the PCB traces.

Parasitic capacitance at the gain setting pins can also affect CMRR over frequency. If the board design has a component at the gain setting pins (for example, a switch or jumper), the component should be chosen so that the parasitic capacitance is as small as possible.

### Power Supplies

A stable dc voltage should be used to power the instrumentation amplifier. Noise on the supply pins can adversely affect performance. See the PSRR performance curves in Figure 18 and Figure 19 for more information.

A 0.1 μF capacitor should be placed as close as possible to each supply pin. As shown in Figure 59, a 10 μF tantalum capacitor can be used farther away from the part. In most cases, it can be shared by other precision integrated circuits.



*Figure 59. Supply Decoupling, REF, and Output Referred to Local Ground*

### Reference Pin

The output voltage of the AD8229 is developed with respect to the potential on the reference terminal. Care should be taken to tie REF to the appropriate local ground.

## INPUT BIAS CURRENT RETURN PATH

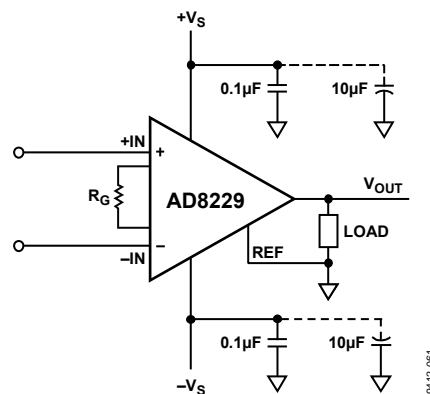The input bias current of the AD8229 must have a return path to ground. When using a floating source without a current return path, such as a thermocouple, a current return path should be created, as shown in Figure 60.
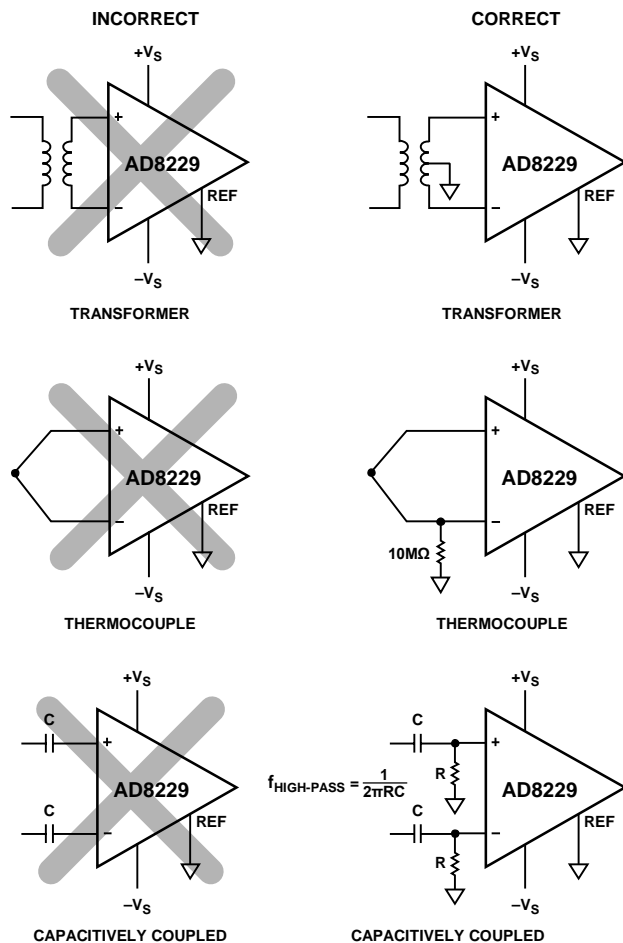


*Figure 60. Creating an Input Bias Current Return Path*

## INPUT PROTECTION

The inputs to the AD8229 should be kept within the ratings stated in the Absolute Maximum Ratings section. If this cannot be done, protection circuitry can be added in front of the AD8229 to limit the current into the inputs to a maximum current, I_MAX.

### Input Voltages Beyond the Rails

If voltages beyond the rails are expected, use an external resistor in series with each input to limit current during overload conditions. The limiting resistor at the input can be computed from

$$R_{PROTECT} \geq \frac{|V_{IN} - V_{SUPPLY}|}{I_{MAX}}$$

Noise-sensitive applications may require a lower protection resistance. Low leakage diode clamps, such as the BAV199, can be used at the inputs to shunt current away from the AD8229 inputs and therefore allow smaller protection resistor values. To ensure current flows primarily through the external protection diodes,

place a small value resistor, such as a 33 Ω, between the diodes and the AD8229.
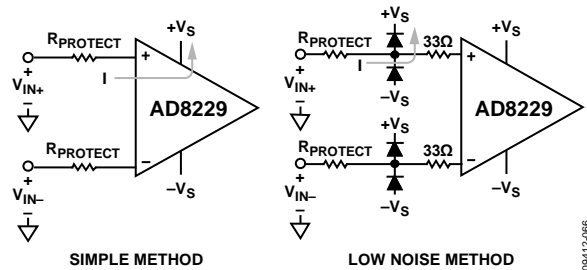


*Figure 61. Protection for Voltages Beyond the Rails*

### Large Differential Input Voltage at High Gain

If large differential voltages at high gain are expected, use an external resistor in series with each input to limit current during overload conditions. The limiting resistor at each input can be computed from

$$R_{PROTECT} \geq \frac{1}{2}\left(\frac{|V_{DIFF}| - 1V}{I_{MAX}} - R_G\right)$$

Noise-sensitive applications may require a lower protection resistance. Low leakage diode clamps, such as the BAV199, can be used across the inputs to shunt current away from the AD8229 inputs and therefore allow smaller protection resistor values.
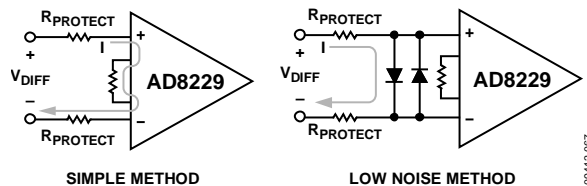


*Figure 62. Protection for Large Differential Voltages*

### I_MAX

The maximum current into the AD8229 inputs, I_MAX, depends on both time and temperature. At room temperature, the part can withstand a current of 10 mA for at least a day. This time is cumulative over the life of the part. At 210°C, limit current to 2 mA for the same period. The part can withstand 5 mA at 210°C for an hour, cumulative over the life of the part.

## RADIO FREQUENCY INTERFERENCE (RFI)

RF rectification is often a problem when amplifiers are used in applications that have strong RF signals. The disturbance can appear as a small dc offset voltage. High frequency signals can be filtered with a low-pass RC network placed at the input of the instrumentation amplifier, as shown in Figure 63. The filter limits the input signal bandwidth, according to the following relationship:

$$FilterFrequency_{DIFF} = \frac{1}{2\pi R(2C_D + C_C)}$$

$$FilterFrequency_{CM} = \frac{1}{2\pi RC_C}$$

where $C_D \geq 10\ C_C$.

*Figure 63. RFI Suppression*

$C_D$ affects the difference signal, and $C_C$ affects the common-mode signal. Values of R and $C_C$ should be chosen to minimize RFI. A mismatch between $R \times C_C$ at the positive input and $R \times C_C$ at the negative input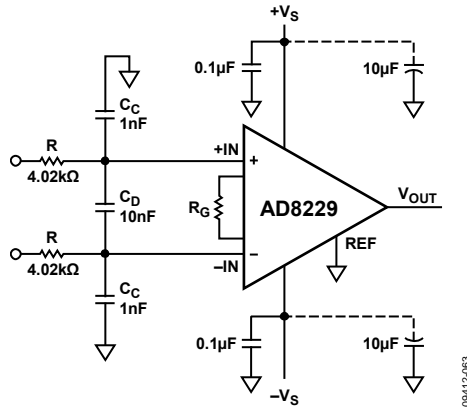 degrades the CMRR of the AD8229. By using a value of $C_D$ one magnitude larger than $C_C$, the effect of the mismatch is reduced, and performance is improved.

Resistors add noise; therefore, the resistor and capacitor values chosen depend on the desired tradeoff between noise, input impedance at high frequencies, and RFI immunity. The resistors used for the RFI filter can be the same as those used for input protection.

## CALCULATING THE NOISE OF THE INPUT STAGE

The total noise of the amplifier front end depends on much more than the 1 nV/√Hz headline specification of this data sheet. There are three main contributors: the source resistance, the voltage noise of the instrumentation amplifier, and the current noise of the instrumentation amplifier.

In the following calculations, noise is referred to the input (RTI). In other words, everything is calculated as if it appeared at the amplifier input. To calculate the noise referred to the amplifier output (RTO), simply multiple the RTI noise by the gain of the instrumentation amplifier.
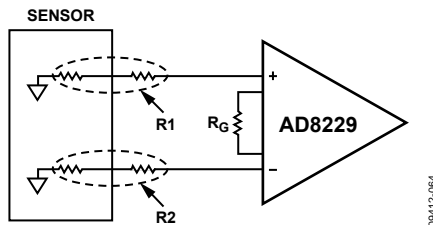


*Figure 64. AD8229 with Source Resistance from Sensor and Protection Resistors*

### Source Resistance Noise

Any sensor connected to the AD8229 has some output resistance. There may also be resistance placed in series with inputs for protection from either overvoltage or radio frequency interference. This combined resistance is labeled R1 and R2 in Figure 64. Any resistor, no matter how well made, has a minimum level of noise. This noise is proportional to the square root of the resistor value. At room temperature, the value is approximately equal to 4 nV/√Hz × √(resistor value in kΩ).

For example, assuming that the combined sensor and protection resistance on the positive input is 4 kΩ, and on the negative input is 1 kΩ, the total noise from the input resistance is

$$\sqrt{(4 \times \sqrt{4})^2 + (4 \times \sqrt{1})^2} \ = \ \sqrt{64 + 16} \ = 8.9 \text{ nV}/\sqrt{Hz}$$

### Voltage Noise of the Instrumentation Amplifier

The voltage noise of the instrumentation amplifier is calculated using three parameters: the part input noise, output noise, and the $R^G$ resistor noise. It is calculated as follows:

*Total Voltage Noise =*

$$\sqrt{(Output\ Noise/G)^2 + (Input\ Noise)^2 + (Noise\ of\ R_G\ Resistor)^2}$$

For example, for a gain of 100, the gain resistor is 60.4 Ω. Therefore, the voltage noise of the in-amp is

$$\sqrt{(45/100)^2 + 1^2 + (4 \times \sqrt{0.0604})^2} \ = 1.5 \text{ nV}/\sqrt{Hz}$$

### Current Noise of the Instrumentation Amplifier

Current noise is calculated by multiplying the source resistance by the current noise.

For example, if the R1 source resistance in Figure 64 is 4 kΩ, and the R2 source resistance is 1 k Ω, the total effect from the current noise is calculated as follows:

$$\sqrt{((4 \times 1.5)^2 + (1 \times 1.5)^2)} \ = 6.2 \text{ nV}/\sqrt{Hz}$$

### Total Noise Density Calculation

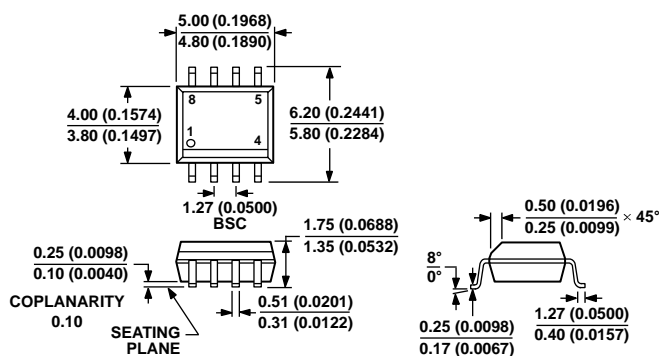To determine the total noise of the in-amp, referred to input, combine the source resistance noise, voltage noise, and current noise contribution by the sum of squares method.

For example, if the R1 source resistance in Figure 64 is 4 kΩ, the R2 source resistance is 1 k Ω, and the gain of the in-amps is 100, the total noise, referred to input, is

$$\sqrt{8.9^2 + 1.5^2 + 6.2^2)} \ = 11.0 \text{ nV}/\sqrt{Hz}$$

## OUTLINE DIMENSIONS



*Figure 65. 8-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP]*
*(D-8-1)*
*Dimensions shown in inches*



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

*Figure 66. 8-Lead Standard Small Outline Package [SOIC_N]*
*Narrow Body*
*(R-8)*
*Dimensions shown in millimeters and (inches)*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| AD8229HDZ | −40°C to +210°C | 8-Lead Side-Brazed Ceramic Dual In-Line Package [SBDIP] | D-8-1 |
| AD8229HRZ | −40°C to +175°C | 8-Lead Standard Small Outline Package [SOIC_N] | R-8 |
| AD8229HRZ-R7 | −40°C to +175°C | 8-Lead Standard Small Outline Package [SOIC_N] | R-8 |

[1] Z = RoHS Compliant Part.

## NOTES

**AD8229**

## NOTES

# NOTES

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