TQP3M9009

High Linearity LNA Gain Block

Applications

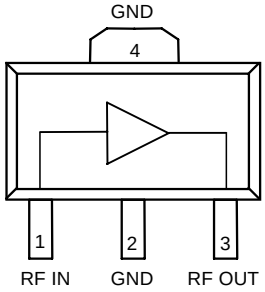
- Repeaters
- Mobile Infrastructure
- LTE / WCDMA / EDGE / CDMA
- General Purpose Wireless

3-pin SOT-89 Package

Product Features

- 50-4000 MHz
- 21.8 dB Gain @ 1.9 GHz
- +39.5 dBm Output IP3
- 1.3 dB Noise Figure @ 1.9 GHz
- 50 Ohm Cascadable Gain Block
- Unconditionally stable
- High input power capability
- +5V Single Supply, 125 mA Current
- SOT-89 Package

Functional Block Diagram



General Description

The TQP3M9009 is a cascadable, high linearity gain block amplifier in a low-cost surface-mount package. At 1.9 GHz, the amplifier is targeted to provide 21.8 dB gain, +39.5 dBm OIP3, and 1.3 dB Noise Figure while only drawing 125 mA current. The device is housed in a leadfree/green/RoHS-compliant industry-standard SOT-89 package using a NiPdAu plating to eliminate the possibility of tin whiskering.

The TQP3M9009 has the benefit of having high gain across a broad range of frequencies while also providing very low noise. This allows the device to be used in both receiver and transmitter chains for high performance systems. The amplifier is internally matched using a high performance E-pHEMT process and only requires an external RF choke and blocking/bypass capacitors for operation from a single +5V supply. The internal active bias circuit also enables stable operation over bias and temperature variations.

The TQP3M9009 covers the 0.05-4 GHz frequency band and is targeted for wireless infrastructure or other applications requiring high linearity and/or low noise figure.

Pin Configuration

Pin #	Symbol
1	RF Input
3	RF Output / Vcc
2, 4	Ground

Ordering Information

Part No.	Description
TQP3M9009	High Linearity LNA Gain Block
TQP3M9009-PCB_IF	TQP3M9009 EVB 0.05-0.5 GHz
TQP3M9009-PCB_RF	TQP3M9009 EVB 0.5-4 GHz

Standard T/R size = 1000 pieces on a 7” reel.

Specifications

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to +150 °C
RF Input Power,CW,50 Ω, T = 25ºC	+23 dBm
Device Voltage,V_{dd}	+7 V
Reverse Device Voltage	-0.3 V
Thermal Resistance (junction to case)	34 °C/W
Junction Temperature, T_J For 10^6 hours MTTF	190 °C

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{dd}	+4.75	+5	+5.25	V
T(case)	-40		85	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

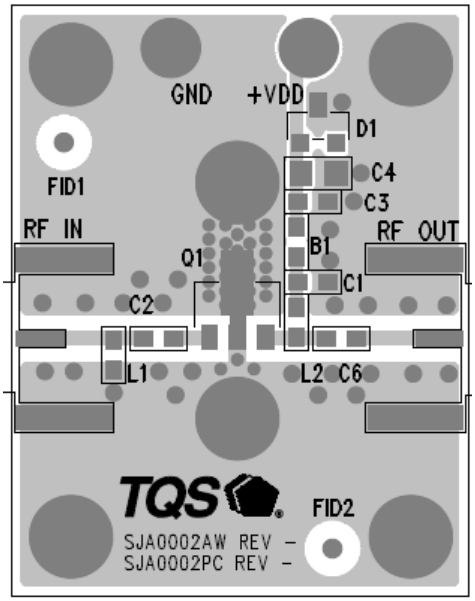
Electrical Specifications

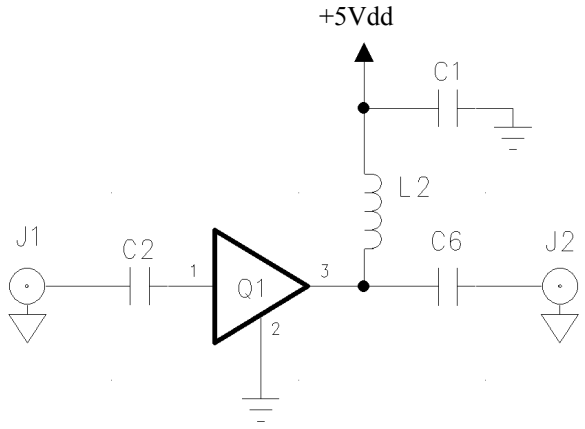
Test conditions unless otherwise noted: +25ºC, +5V Vsupply, 50 Ω system.

Parameter	Conditions	Min	Typical	Max	Units
Operational Frequency Range		50		4000	MHz
Test Frequency			1900		MHz
Gain			21.8		dB
Input Return Loss			13		dB
Output Return Loss			14		dB
Output P1dB			+22		dBm
Output IP3	See Note 1.		+39.5		dBm
Noise Figure			1.3		dB
Vdd			+5		V
Current, Idd			125		mA

Notes
1. OIP3 measured with two tones at an output power of +3 dBm / tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the OIP3 using 2:1 rule.

Application Circuit Configuration





Notes:
1. See PC Board Layout, page 8 for more information.
2. Components shown on the silkscreen but not on the schematic are not used.
3. B1 (0 Ω jumper) may be replaced with copper trace in the target application layout.
4. The recommended component values are dependent upon the frequency of operation.
5. All components are of 0603 size unless stated on the schematic.

Bill of Material

Reference Designation	Frequency (MHz)	
	TQP3M9009-PCB_IF	TQP3M9009-PCB_RF
	50 - 500	500 - 4000
Q1	TQP3M9009	
C2, C6	1000 pF	100 pF
C1	0.01 uF	0.01 uF
L2	330 nH	68 nH
L1, D1, C3, C4	Do Not Place	
B1	0 Ω	

Notes:
1. Performances can be optimized at frequency of interest by using recommended component values shown in the table below.

Reference Designation	Frequency (MHz)			
	500	2000	2500	3500
C2, C6	100 pF	22 pF	22 pF	22 pF
L2	82 nH	22 nH	18 nH	15 nH

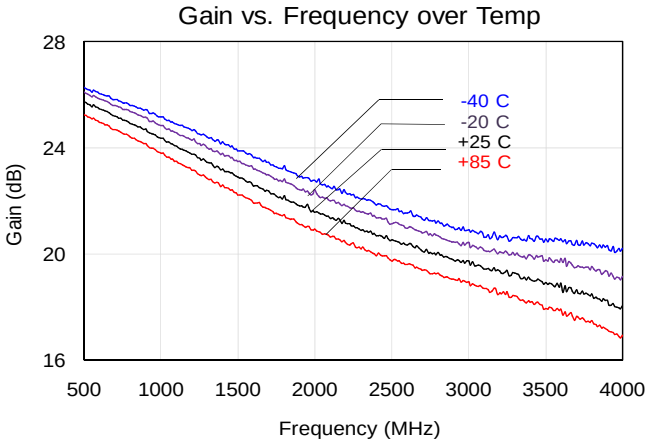
Typical Performance 500-4000 MHz

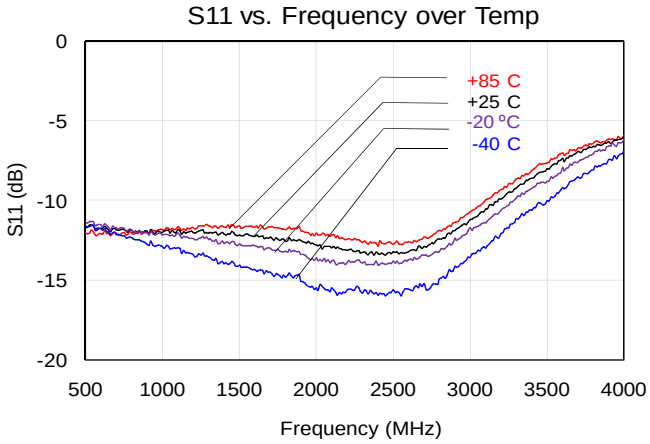
Test conditions unless otherwise noted: +25ºC, +5V, 125 mA, 50 Ω system. The data shown below is measured on TQP3M9009-PCB_RF.

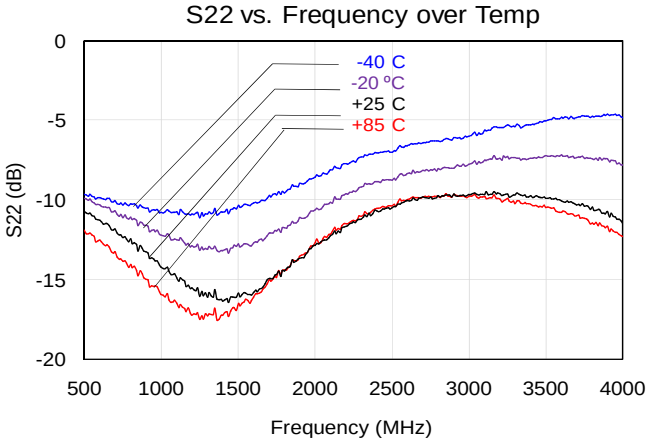
Frequency	MHz	500	900	1900	2700	3500	4000
Gain	dB	25.5	24.7	21.8	20	18.9	17.9
Input Return Loss	dB	11.5	12	13	13	8	6
Output Return Loss	dB	10.8	13	14	10	10	11.3
Output P1dB	dBm	+22.5	+21.8	+22	+21.6	+21.8	+20.7
OIP3 [1]	dBm	+41.4	+40.5	+39.5	+39	+37.9	+35.8
Noise Figure [2]	dB	0.9	0.9	1.3	1.7	2.1	2.4

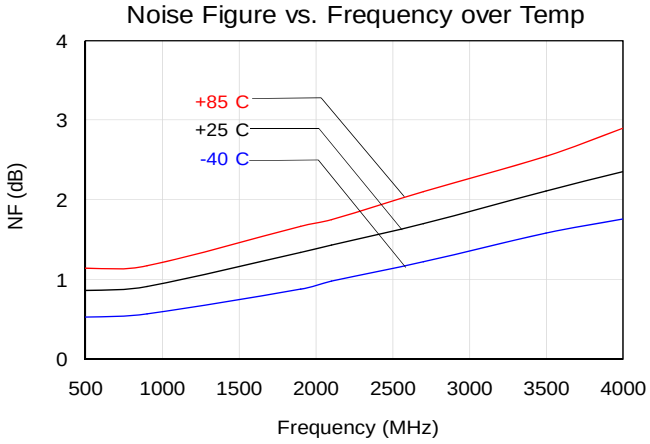
Notes:
1. OIP3 measured with two tones at an output power of +3 dBm / tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the OIP3 using 2:1 rule.
2. Noise figure data shown in the table above is measured on evaluation board which includes board losses of around 0.1 dB @ 2 GHz.

RF Performance Plots



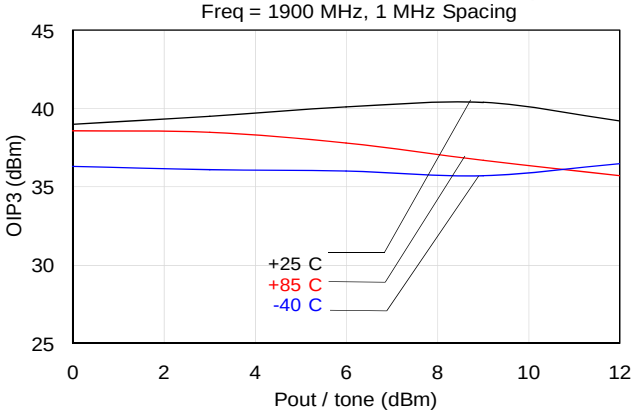




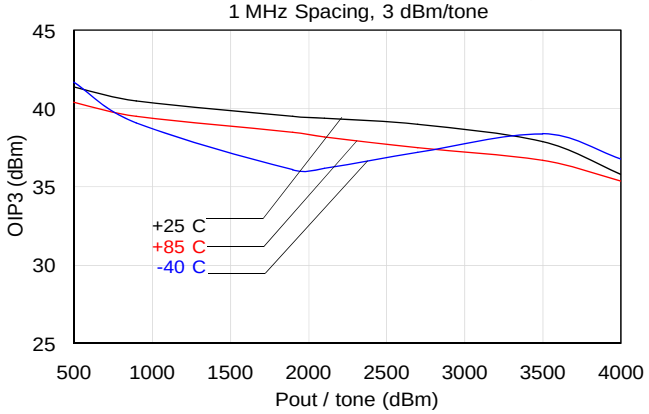


RF Performance Plots

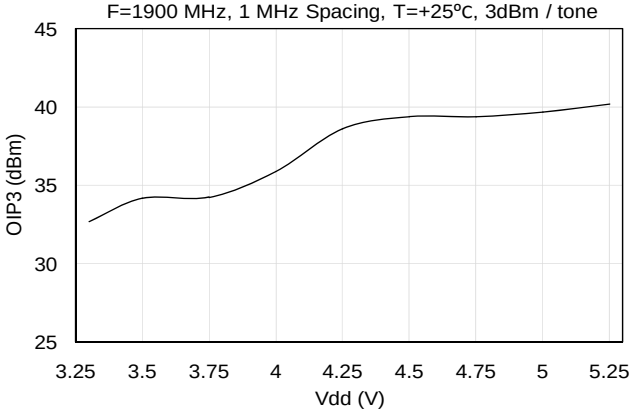
OIP3 vs. Pout / tone over Temp
Freq = 1900 MHz, 1 MHz Spacing



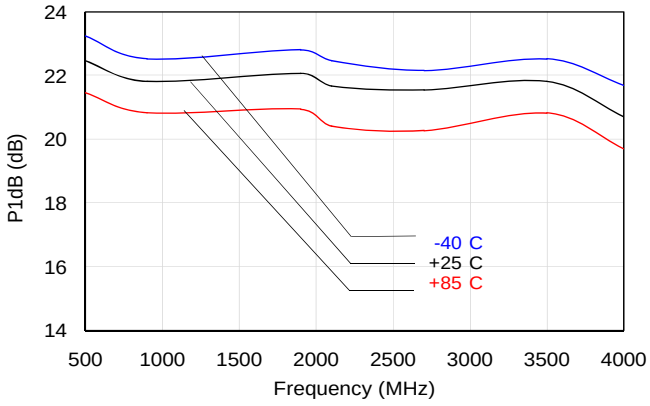
OIP3 vs. Frequency over Temp
1 MHz Spacing, 3 dBm/tone



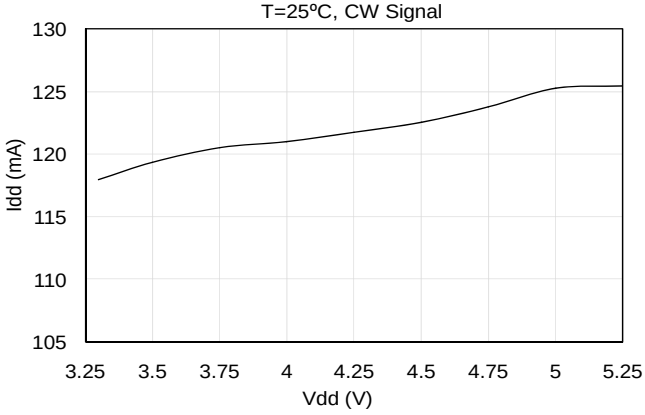
OIP3 vs. Vdd
F=1900 MHz, 1 MHz Spacing, T=+25ºC, 3dBm / tone



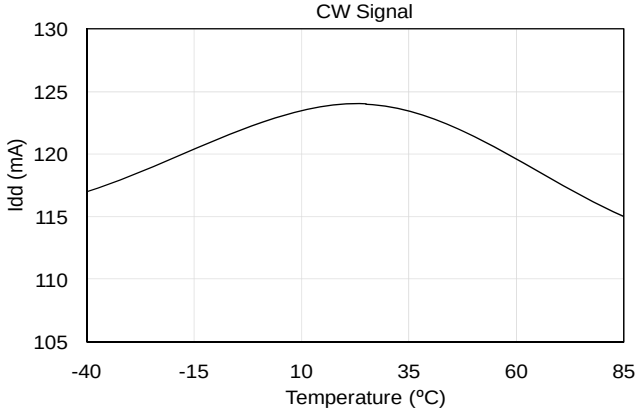
P1dB vs. Frequency over Temp



Idd vs. Vdd
T=25ºC, CW Signal



Idd vs. Temperature
CW Signal



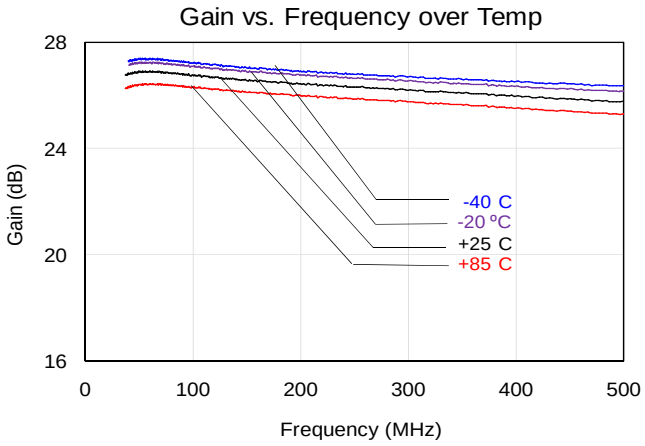
Typical Performance 50-500 MHz

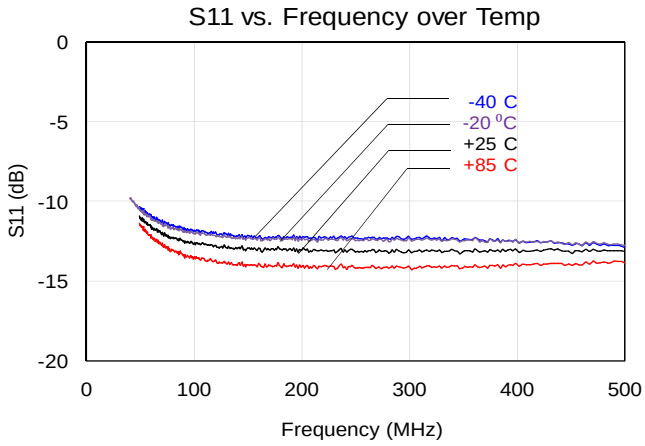
Test conditions unless otherwise noted: +25ºC, +5V, 125 mA, 50 Ω system. The data shown below is measured on TQP3M9009-PCB_IF.

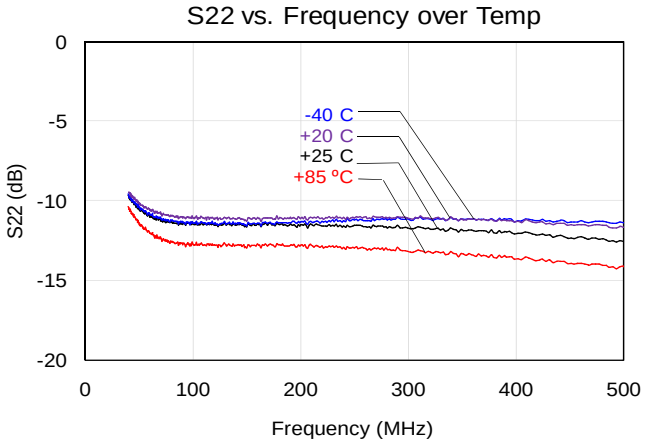
Frequency	MHz	70	100	200	500
Gain	dB	27	26.8	26.4	25.8
Input Return Loss	dB	12	13	13	13
Output Return Loss	dB	11	12	12	13
Output P1dB	dBm	+21.6	+21.9	+21.9	+22.2
OIP3 [1]	dBm	+37.6	+38.8	+39	+41.4
Noise Figure [2]	dB	1.4	1.3	0.9	0.9

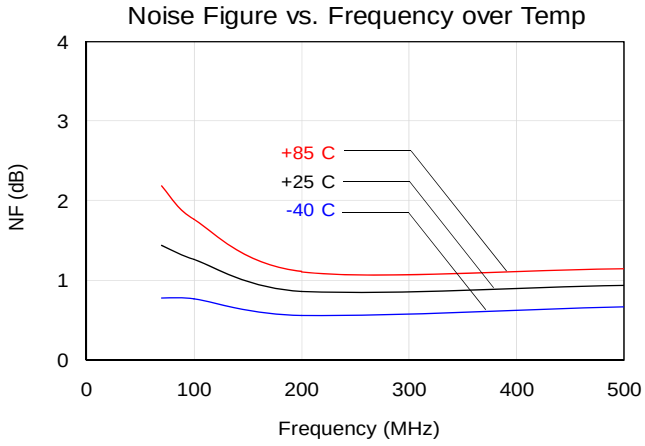
Notes:
1. OIP3 measured with two tones at an output power of +3 dBm / tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the OIP3 using 2:1 rule.
2. Noise figure data shown in the table above is measured on evaluation board which includes board losses of around 0.1 dB @ 2 GHz.

IF Performance Plots

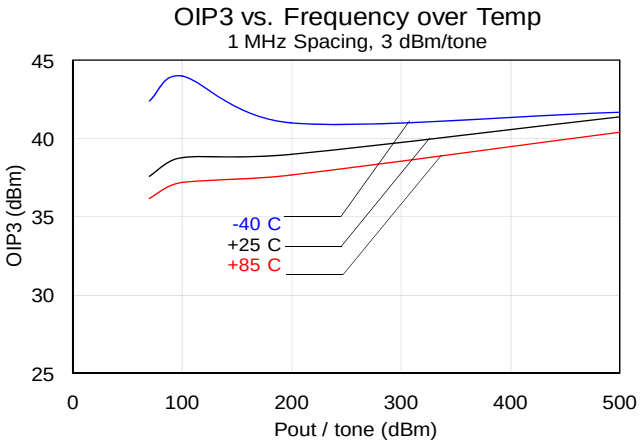


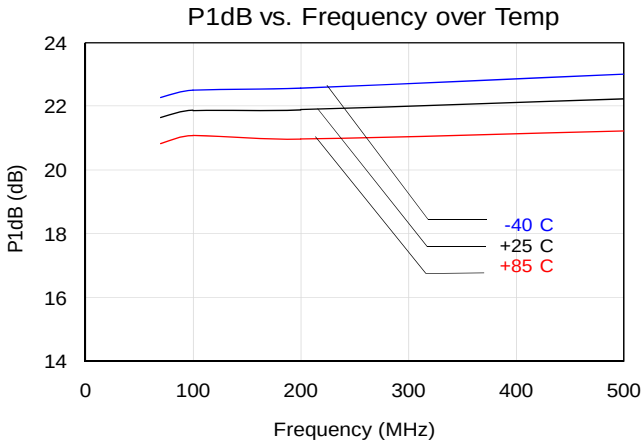




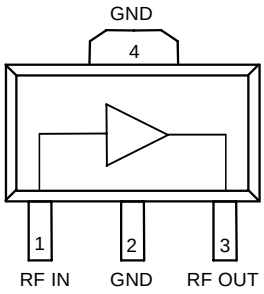


IF Performance Plots





Pin Configuration and Description



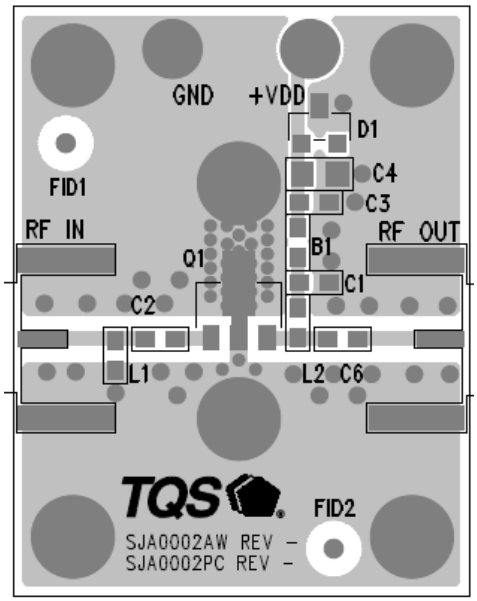
Pin	Symbol	Description
1	RF IN	Input, matched to 50 ohms, External DC block is required.
2, 4	GND	Needed for RF and the thermal path
3	RFout / Vdd	Output, matched to 50 ohms, External DC Block is required and supply voltage

Applications Information

PC Board Layout

Top RF layer is .014" NELCO N4000-13, ϵ_r = 3.9, 4 total layers (0.062" thick) for mechanical rigidity. Metal layers are 1-oz copper. 50 ohm Microstrip line details: width = .029", spacing = .035".

The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from supplier to supplier, careful process development is recommended.

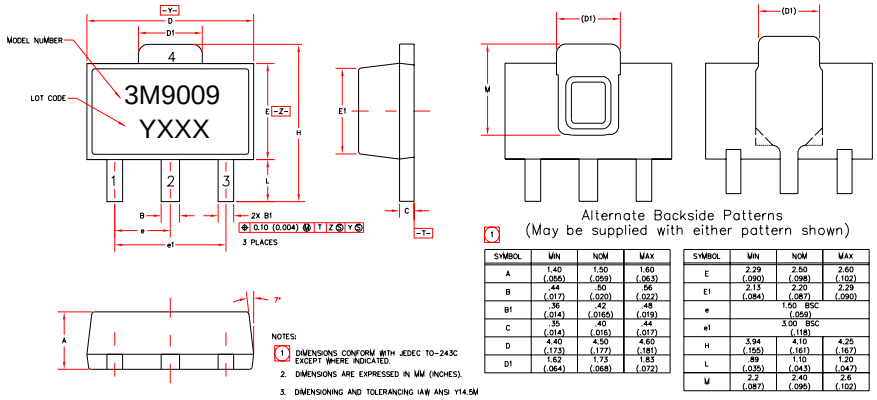


Mechanical Information

Package Information and Dimensions

This package is lead-free/RoHS-compliant. The plating material on the leads is NiPdAu. It is compatible with both lead-free (maximum 260 °C reflow temperature) and lead (maximum 245 °C reflow temperature) soldering processes.

The component will be marked with a "3M9009" designator with an alphanumeric lot code on the top surface of package. The "Y" represents the last digit of the year the part was manufactured; the "XXX" is an auto generated number.

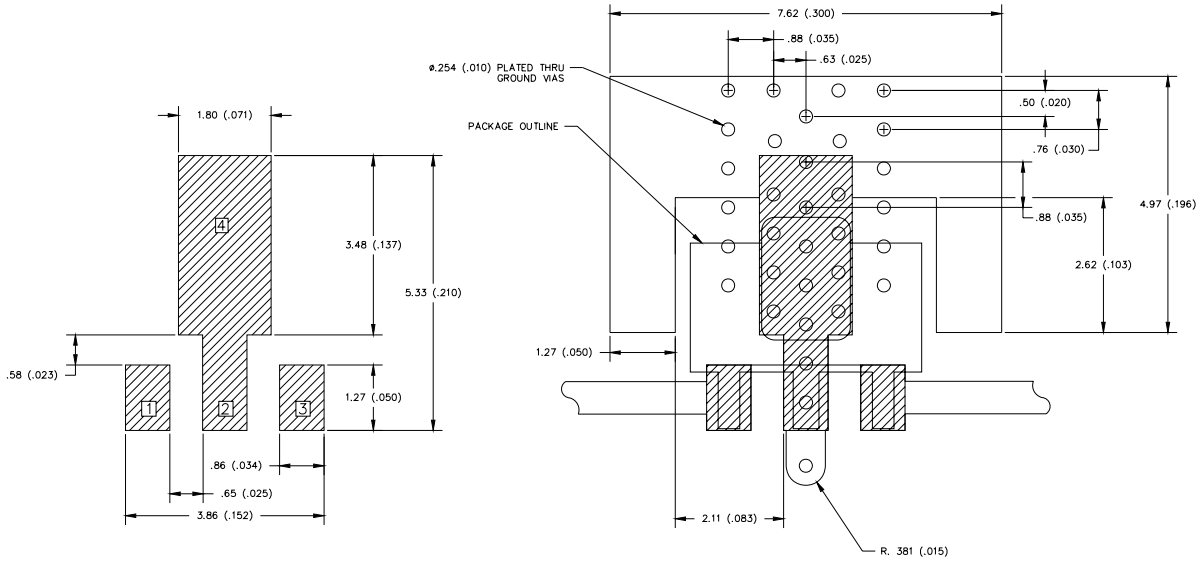


SYMBOL	MIN	NOM	MAX
A	1.40 (.055)	1.50 (.059)	1.60 (.063)
B	.44 (.017)	.50 (.020)	.56 (.022)
B1	.36 (.014)	.42 (.0165)	.48 (.019)
C	.35 (.014)	.40 (.016)	.44 (.017)
D	4.40 (.173)	4.50 (.177)	4.60 (.181)
D1	1.62 (.064)	1.73 (.068)	1.83 (.072)

SYMBOL	MIN	NOM	MAX
E	2.29 (.090)	2.50 (.098)	2.60 (.102)
E1	2.13 (.084)	2.20 (.087)	2.29 (.090)
e		1.50 BSC (.059)	
e1		3.00 BSC (.118)	
H	3.94 (.155)	4.10 (.161)	4.25 (.167)
L	.89 (.035)	1.10 (.043)	1.20 (.047)
M	2.2 (.087)	2.40 (.095)	2.6 (.102)

Mounting Configuration

All dimensions are in millimeters (inches). Angles are in degrees.



Notes:

1. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
3. RF trace width depends upon the PC board material and construction.
4. Use 1 oz. Copper minimum.

Product Compliance Information

ESD Information

Caution! ESD-Sensitive Device

ESD Rating:	Class 1A
Value:	Passes ≥ 250 V to < 500 V.
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114

ESD Rating:	Class IV
Value:	Passes ≥ 1000 V
Test:	Charged Device Model (CDM)
Standard:	JEDEC Standard JESD22-C101

MSL Rating

Level 3 at +260 °C convection reflow
The part is rated Moisture Sensitivity Level 3 at 260°C per JEDEC standard IPC/JEDEC J-STD-020.

Solderability

Compatible with the latest version of J-STD-020, Lead free solder, 260°

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

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