PCF8883

Capacitive touch/proximity switch with auto-calibration, large voltage operating range, and very low power consumption

Rev. 4.1 — 14 September 2016 Product data sheet

1. General description

The integrated circuit PCF8883 is a capacitive touch and proximity switch that uses a patented (EDISEN) digital method to detect a change in capacitance on a remote sensing plate. Changes in the static capacitance (as opposed to dynamic capacitance changes) are automatically compensated using continuous auto-calibration. Remote sensing plates (e.g. conductive foil) can be connected directly to the IC[1] or remotely using a coaxial cable.

2. Features and benefits

- Dynamic proximity switch
- Digital processing method
- Adjustable sensitivity, can be made very high
- Adjustable response time
- Wide input capacitance range (10 pF to 60 pF)
- Automatic calibration
- A large distance (several meters) between the sensing plate and the IC is possible
- Open-drain output (P-type MOSFET, external load between pin and ground)
- Designed for battery powered applications (I_{DD} = 3 μA, typical)
- Output configurable as push-button, toggle, or pulse
- Wide voltage operating range (V_{DD} = 3 V to 9 V)
- Large temperature operating range (T_{amb} = −40 °C to +85 °C)
- Internal voltage regulator
- Available in SOIC8 and wafer level chip-size package

3. Applications

- Proximity detection
- Proximity sensing in
  - Mobile phones
  - Portable entertainment units
- Switch for medical applications
- Switch for use in explosive environments
- Vandal proof switches
- Transportation: Switches in or under upholstery, leather, handles, mats, and glass

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 21.

- Buildings: switch in or under carpets, glass, or tiles
- Sanitary applications: use of standard metal sanitary parts (e.g. tap) as switch
- Hermetically sealed keys on a keyboard

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF8883T	SOIC8	plastic small outline package; 8 leads; body width 3.9 mm	PCF8883T
PCF8883US	WLCSP8	wafer level chip-size package; 8 bumps	PCF8883US

4.1 Ordering options

Table 2. Ordering options

Product type number	Orderable part number	Sales item (12NC)	Delivery form	IC revision
PCF8883T/1	PCF8883T/1,118	935289766118	tape and reel, 13 inch	1
PCF8883US/7EA/1	PCF8883US/7EA/1Y	935300777518	dry pack, tape and reel, 13 inch	1

5. Marking

Table 3. Marking codes

Product type number	Marking code
PCF8883T	PCF8883
PCF8883US	PC 8883-1

6. Block diagram

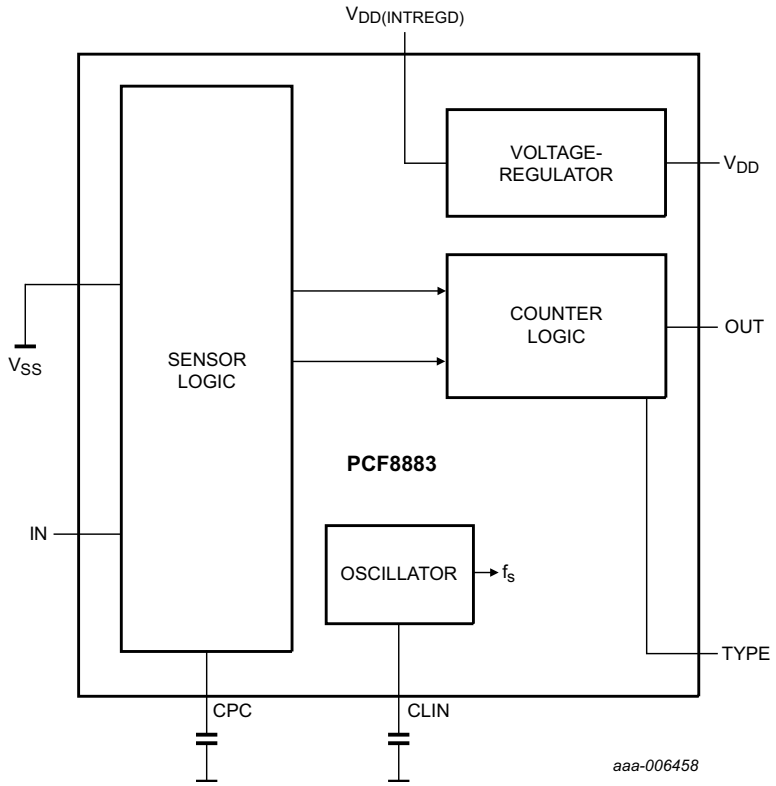
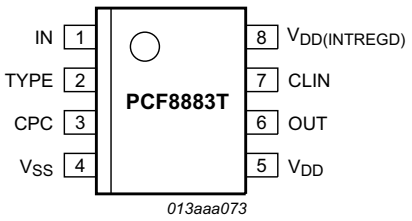


Fig 1. Block diagram of PCF8883

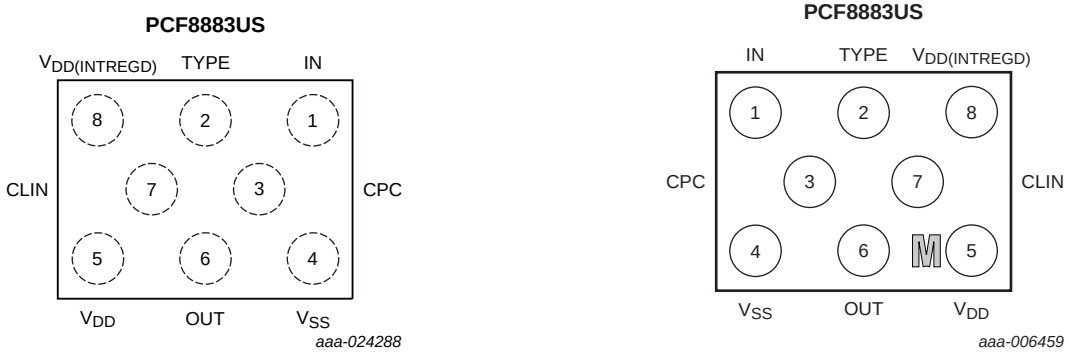
7. Pinning information

7.1 Pinning



Top view. For mechanical details, see Figure 17.

Fig 2. Pin configuration of PCF8883T (SOIC8)



Top side view **Bump view (bottom) side**

Fig 3. Pin configuration of PCF8883US (WLCSP8); for mechanical details, see Figure 18

7.2 Pin description

Table 4. Pin description

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin		Type	Description
	PCF8883T	PCF8883US		
IN	1	1	analog input/output	sensor input
TYPE	2	2	input	pin OUT behavior configuration input
CPC	3	3	analog input/output	sensitivity setting
V_{SS}[1]	4	4	supply	ground supply voltage
V_{DD}	5	5	supply	supply voltage
OUT	6	6	output	switch output
CLIN	7	7	analog input/output	sampling rate setting
$V_{DD(INTREGD)}$[2]	8	8	supply	internal regulated supply voltage output

[1] The substrate (rear side of the die) is connected to V_{SS} and should be electrically isolated.

[2] The internal regulated supply voltage output must be decoupled with a decoupling capacitor to V_{SS}.

8. Functional description

Figure 4 and Figure 5 show the functional principle of the PCF8883.

The discharge time (t_{dch}) of a chip-internal RC timing circuit, to which the external sensing plate is connected via pin IN, is compared to the discharge time ($t_{dch(ref)}$) of a second chip-internal reference RC timing circuit. Both RC timing circuits are periodically charged from $V_{DD(INTREGD)}$ via identical switches and then discharged via a resistor to ground (V_{SS}). Both switches are synchronized.

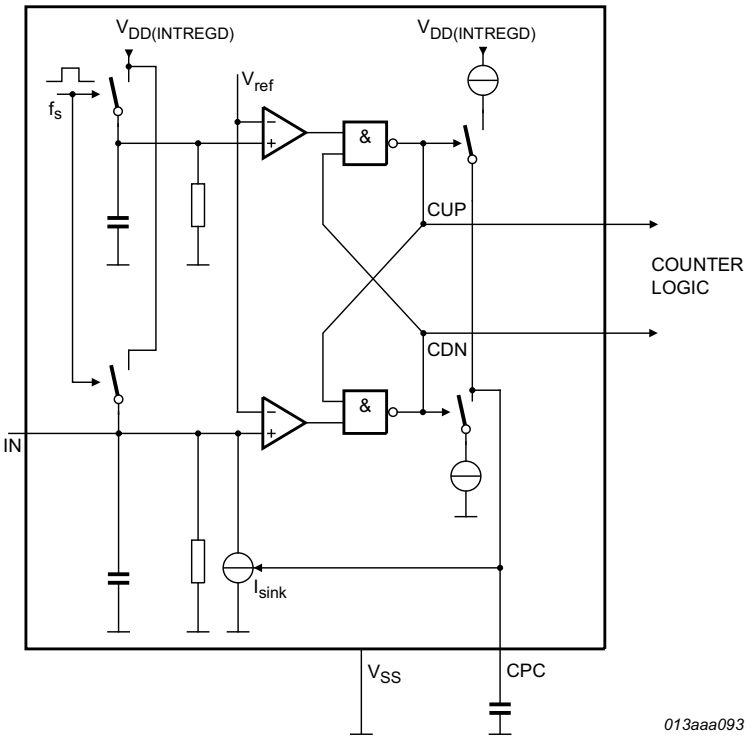


Fig 4. Functional diagram of the sensor logic

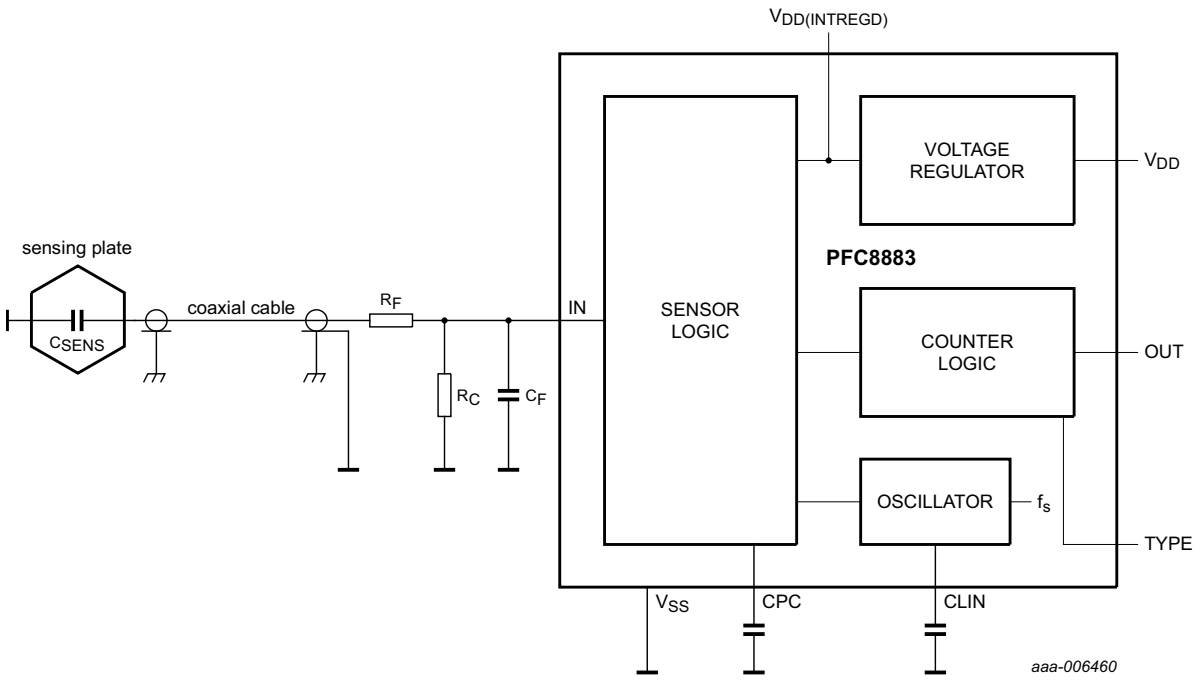
The charge-discharge cycle is governed by the sampling rate (f_s). If the voltage of one of the RC timing circuits falls below the internal reference voltage V_{ref}, the respective comparator output becomes LOW. The logic following the comparators determines which comparator switches first. If the upper (reference) comparator switches, then a pulse is given on CUP. If the lower (input) comparator switches first, then a pulse is given on CDN (see Figure 4).

The pulses control the charge on the external capacitor C_{CPC} on pin CPC. Every time a pulse is given on CUP, capacitor C_{CPC} is charged from $V_{DD(INTREGD)}$ for a fixed time causing the voltage on C_{CPC} to rise. Likewise when a pulse occurs on CDN, capacitor C_{CPC} is connected to a current sink to ground for a fixed time causing the voltage on C_{CPC} to fall.

If the capacitance on pin IN increases, the discharge time t_{dch} increases too. Therefore it takes longer for the voltage on the corresponding comparator to drop below V_{ref}. Only once this happens, the comparator output becomes LOW and this results in a pulse on CDN discharging the external capacitor C_{CPC} slightly. Thus most pulses will now be given by CUP. Without further action, capacitor C_{CPC} would then fully charge.

However, a chip-internal automatic calibration mechanism that is based on a voltage controlled sink current (I_{sink}) connected to pin IN attempts to equalize the discharge time t_{dch} with the internal reference discharge time $t_{dch(ref)}$. The current source is controlled by the voltage on C_{CPC} which causes the capacitance on pin IN to be discharged more quickly in the case that the voltage on C_{CPC} is rising, thereby compensating for the increase in capacitance on input pin IN. This arrangement constitutes a closed-loop control system that constantly attempts to equalize the discharge time t_{dch} with $t_{dch(ref)}$. This allows compensating for slow changes in capacitance on input pin IN. Fast changes due to an approaching hand for example will not be compensated. In the equilibrium state, the discharge times are equal and the pulses alternate between CUP and CDN.

From this also follows, that an increase in capacitor value C_{CPC} results in a smaller voltage change per pulse CUP or CDN. Thus the compensation due to internal current sink source I_{sink} is slower and therefore the sensitivity of the sensor increases. Likewise a decrease in capacitor C_{CPC} results in a lower sensitivity. (For further information see Section 14.)



C_{SENS} = sensing plate capacitance.

R_C = external discharge (pull-down) resistor.

R_F = low pass filter resistor.

C_F = low pass filter capacitor.

Fig 5. Functional principle of the PCF8883

The counter, following the sensor logic depicted in Figure 4, counts the pulses of CUP or CDN respectively. The counter is reset every time the pulse sequence changes from CUP to CDN or the other way around. Pin OUT will only be activated when enough consecutive CUP or CDN pulses occur. Low-level interference or slow changes in the input capacitance do not cause the output to switch.

Various measures, such as asymmetrical charge and discharge steps, are taken to ensure that the output switches off correctly. A special start-up circuit ensures that the device reaches equilibrium quickly when the supply is attached.

Pin OUT is an open-drain output capable of pulling an external load R_{ext} (at maximum current of 20 mA) up to V_{DD}. The load resistor must be dimensioned appropriately, taking the maximum expected V_{DD} voltage into account. The output is automatically deactivated (short circuit protection) for loads in excess of 30 mA. Pin OUT can also drive a CMOS input without connection of the external load.

A small internal 150 nA current sink I_{sink} enables a full voltage swing to take place on pin OUT, even if no load resistor is connected. This is useful for driving purely capacitive CMOS inputs. The falling slope can be fairly slow in this mode, depending on load capacitance.

The sampling rate (f_s) corresponds to half of the frequency used in the RC timing circuit. The sampling rate can be adjusted within a specified range by selecting the value of C_{CLIN}. The oscillator frequency is internally modulated by 4 % using a pseudo random signal. This prevents interference caused by local AC-fields.

8.1 Output switching modes

The output switching behavior can be selected using pin TYPE (see Figure 6).

- Push-button (TYPE connected to V_{SS}): The output OUT is active as long as the capacitive event[2] lasts.
- Toggle (TYPE connected to $V_{DD(INTREGD)}$): The output OUT is activated by the first capacitive event and deactivated by a following capacitive event.
- Pulse (C_{TYPE} connected between TYPE and V_{SS}): The output OUT is activated for a defined time at each capacitive event. The pulse duration is determined by the value of C_{TYPE} and is approximately 2.5 ms/nF.

A typical value for C_{TYPE} is 4.7 nF which results in an output pulse duration of about 10 ms. The maximum value of C_{TYPE} is 470 nF which results in a pulse duration of about 1 s. Capacitive events are ignored that occur during the time the output is active.

Figure 6 illustrates the switching behavior for the output switching modes. Additionally the graph illustrates, that short-term disturbances on the sensor are suppressed by the circuit.

2. A capacitive event is a dynamic increase of capacitance at the sensor input pin IN.

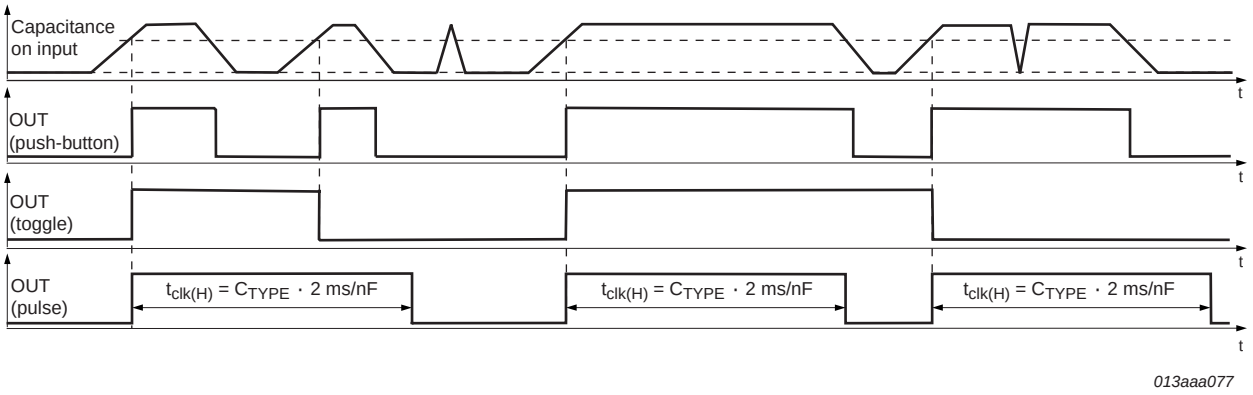


Fig 6. Switching modes timing diagram of PCF8883

8.2 Voltage regulator

The PCF8883 implements a chip-internal voltage regulator supplied by pin V_{DD} that provides an internal supply ($V_{DD(INTREGD)}$) limited to a maximum of 4.6 V. The lock-in voltage V_{lockin} on V_{DD} is typically 4.0 V. Figure 7 shows the relationship between V_{DD} and $V_{DD(INTREGD)}$.

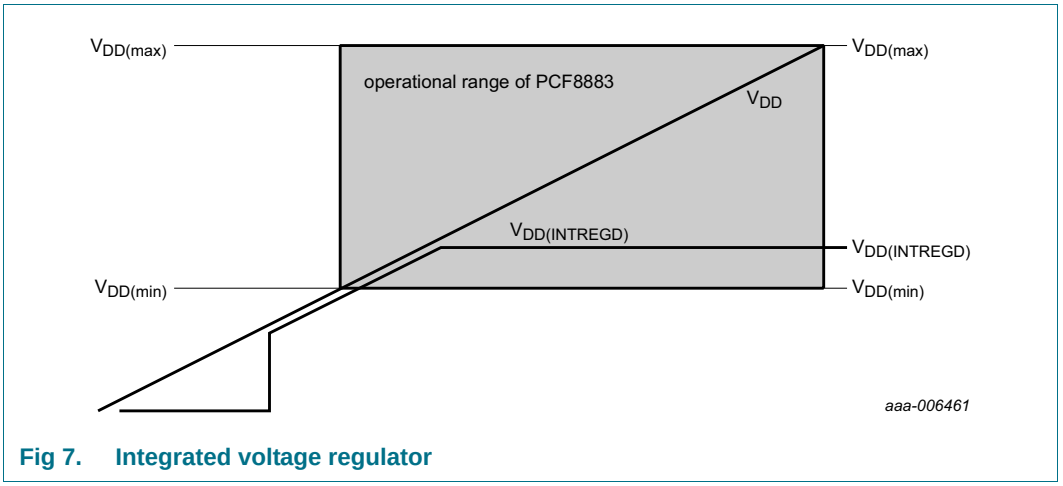


Fig 7. Integrated voltage regulator

9. Safety notes

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

CAUTION

Semiconductors are light sensitive. Exposure to light sources can cause the IC to malfunction. The IC must be protected against light. The protection must be applied to all sides of the IC.

10. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+9	V
V_I	input voltage	on pins IN, TYPE, CPC	–0.5	$V_{DD(INTREGD)}$ + 0.5	V
I_O	output current	on pin OUT	–10	+50	mA
I_{SS}	ground supply current		–10	+50	mA
I_I	input current	on any other pin	–10	+10	mA
P_{tot}	total power dissipation		-	100	mW
V_{ESD}	electrostatic discharge voltage	HBM [1]	-	±2500	V
		MM [2]	-	±200	V
I_{lu}	latch-up current	[3]	-	100	mA
T_{stg}	storage temperature	[4]	–60	+125	°C
T_{amb}	ambient temperature	operating device	–40	+85	°C

[1] Pass level; Human Body Model (HBM) according to Ref. 9 “JESD22-A114”.

[2] Pass level; Machine Model (MM), according to Ref. 10 “JESD22-A115”.

[3] Pass level; latch-up testing, according to Ref. 11 “JESD78” at maximum ambient temperature ($T_{amb(max)}$).

[4] According to the store and transport requirements (see Ref. 14 “UM10569”) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.

11. Static characteristics

Table 6. Static characteristics

V_{DD} = 5 V, T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage	10 pF ≤ C_i ≤ 40 pF; −40 °C ≤ T_{amb} ≤ +85 °C [1]	3.0	-	9.0	V
		10 pF ≤ C_i ≤ 35 pF; −20 °C ≤ T_{amb} ≤ +85 °C [2]	2.8	-	9.0	V
$V_{DD(INTREGD)}$	internal regulated supply voltage		3.0	4.0	4.6	V
$\Delta V_{DD(INTREGD)}$	internal regulated supply voltage variation	regulator voltage drop	-	10	50	mV
I_{DD}	supply current	idle state; f_s = 1 kHz [3]				
		V_{DD} = 5.0 V	-	3	5	µA
		V_{DD} = 3.0 V	-	2.2	3.5	µA
I_{sink}	sink current	internal constant current to V_{SS}	-	150	-	nA
V_O	output voltage	on pin OUT; pull-up voltage	0	V_{DD}	9.0	V
I_O	output current	P-MOS [4]	0	10	20	mA
		short circuit protection $V_O \geq 0.6$ V	20	30	50	mA
V_{sat}	saturation voltage	on pin OUT; I_O = +10 mA				
		V_{DD} = 5.0 V	0.1	0.2	0.4	V
		V_{DD} = 3.0 V	0.1	0.3	0.5	V
C_{dec}	decoupling capacitance	on pin $V_{DD(INTREGD)}$ [5]	100	-	220	nF
$V_{I(CPC)}$	input voltage on pin CPC		0.6	-	$V_{DD(INTREGD)}$ − 0.5	V

[1] Alternatively an external discharge resistor R_C can be used (see Section 14).

[2] Tested on sample basis.

[3] Idle state is the steady state after completed power-on without any activity on the sensor plate and the voltage on the reservoir capacitor C_{CPC} settled.

[4] For reliability reasons, the average output current must be limited to 4.6 mA at 70 °C and 3.0 mA at 85 °C.

[5] External ceramic chip capacitor recommended (see Figure 16).

12. Dynamic characteristics

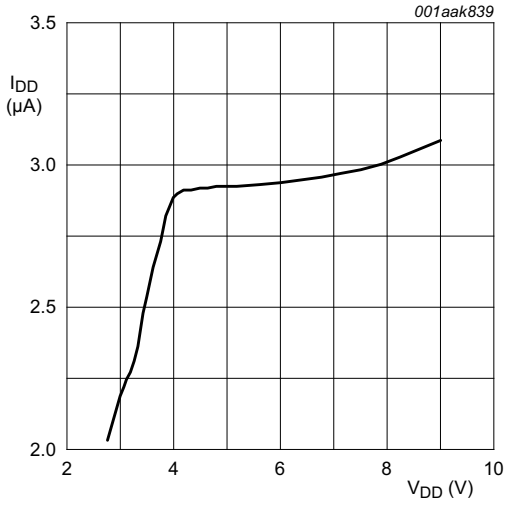
Table 7. Dynamic characteristics

V_{DD} = 5 V, C_{CLIN} = 22 pF, C_{CPC} = 470 nF, T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{CLIN}	capacitance on pin CLIN		0	22	100	pF
C_{CPC}	capacitance on pin CPC	X7R ceramic chip capacitor	90	470	2500	nF
$N_{res(dig)eq}$	equivalent digital resolution		-	14	-	bit
C_{TYPE}	capacitance on pin TYPE		0.1	-	470	nF
C_i	input capacitance	sensing plate and connecting cable				
		V_{DD} = 5.0 V	10	-	60	pF
		T_{amb} = −40 °C to +85 °C; V_{DD} = 3.0 V	10	-	40	pF
$t_{startup}$	start-up time	until normal operation is established	-	0.5	-	s
t_p	pulse duration	on pin OUT; in pulse mode; $C_{TYPE} \geq 10$ nF	-	2.5	-	ms/nF
f_s	sampling frequency	C_{CLIN} = 0 pF	-	3.3	-	kHz
		C_{CLIN} = 22 pF (typical value)	-	1	-	kHz
		C_{CLIN} = 100 pF	-	275	-	Hz
t_{sw}	switching time	at f_s = 1 kHz	-	64	-	ms

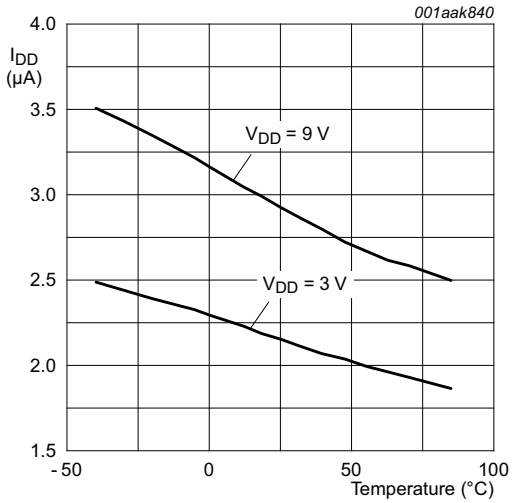
13. Characteristic curves

13.1 Power consumption



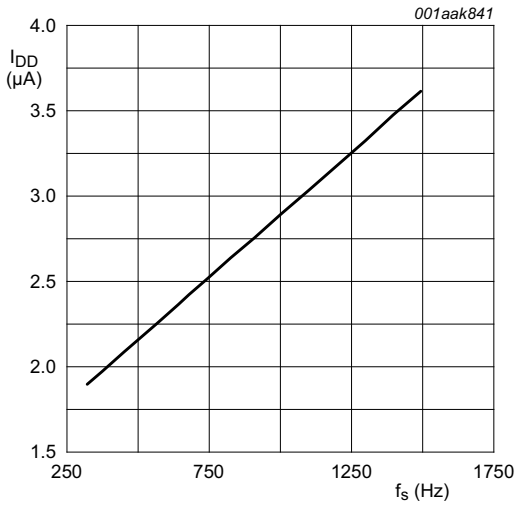
Idle state; f_s = 1 kHz; T_{amb} = 25 °C.

Fig 8. I_{DD} with respect to V_{DD}



Idle state; f_s = 1 kHz.

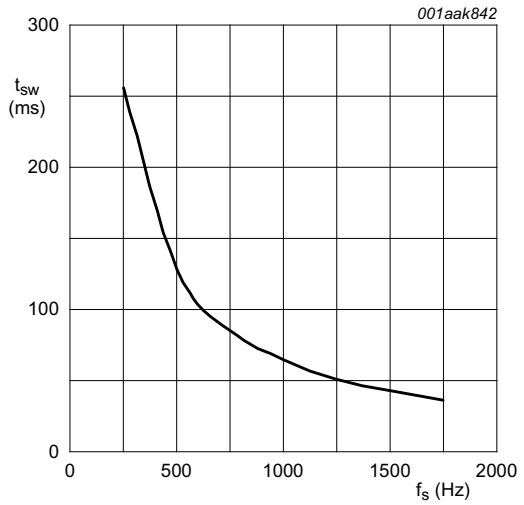
Fig 9. I_{DD} with respect to temperature



Idle state; V_{DD} = 6 V; T_{amb} = 25 °C.

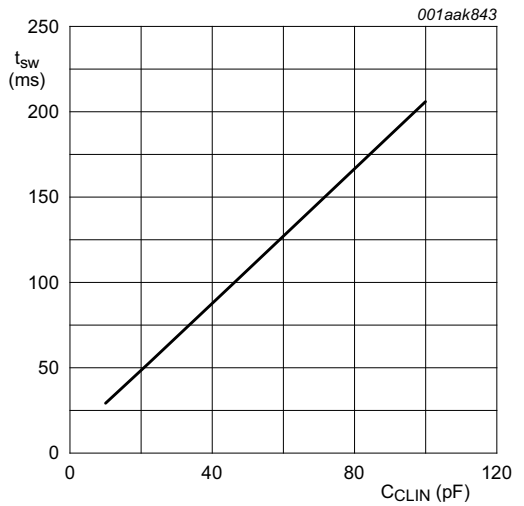
Fig 10. I_{DD} with respect to sampling frequency (f_s)

13.2 Typical reaction time



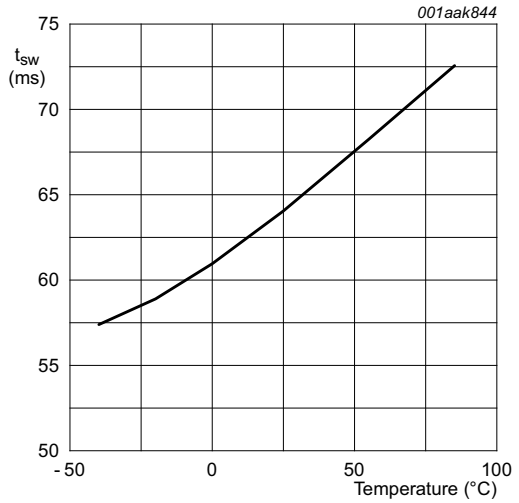
V_{DD} = 6 V; T_{amb} = 25 °C.

Fig 11. Switching time (t_{sw}) with respect to sampling frequency (f_s)



V_{DD} = 6 V; T_{amb} = 25 °C.

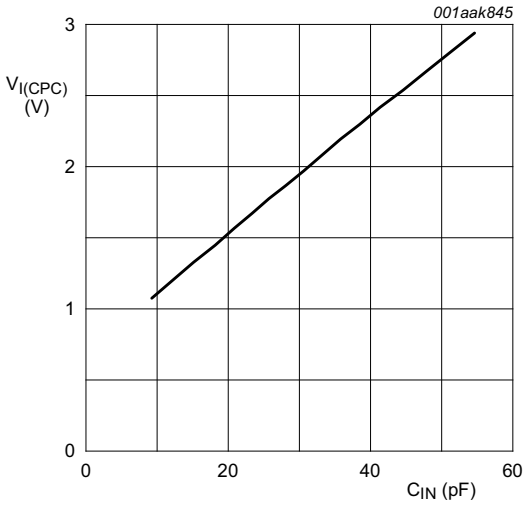
Fig 12. Switching time (t_{sw}) with respect to capacitor on pin CLIN (C_{CLIN})



V_{DD} = 6 V.

Fig 13. Switching time (t_{sw}) with respect to temperature

13.3 Reservoir capacitor voltage

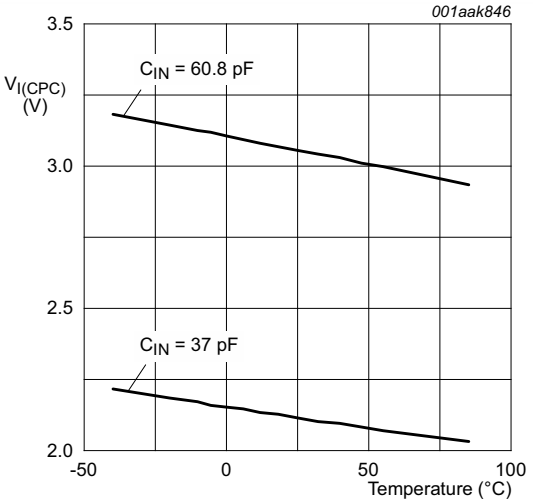


V_{DD} = 6 V; T_{amb} = 25 °C.

$V_{I(CPC)}$ = input voltage on pin CPC.

C_{IN} = capacitor on pin IN.

Fig 14. Input voltage on pin CPC ($V_{I(CPC)}$) with respect to capacitor on pin IN (C_{IN})



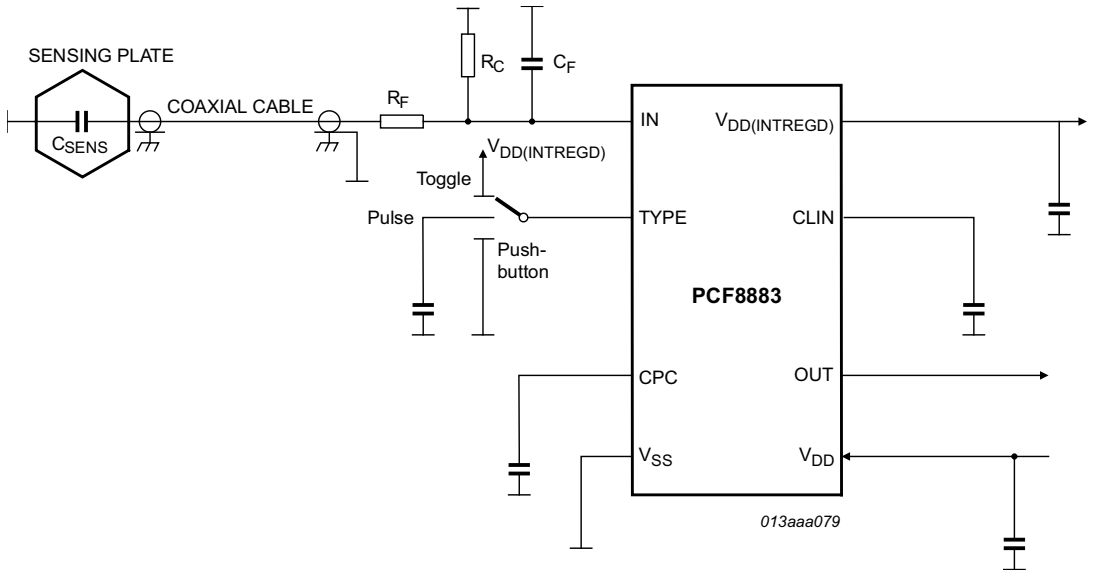
V_{DD} = 6 V.

$V_{I(CPC)}$ = input voltage on pin CPC.

Fig 15. Input voltage on pin CPC ($V_{I(CPC)}$) with respect to temperature

14. Application information

Figure 16 shows the typical connections for a general application[3]. The positive supply is connected to pin V_{DD}. It is recommended to connect smoothing capacitors to ground to both V_{DD} and $V_{DD(INTREGD)}$ (values for C_{dec}, see Table 6).



C_{SENS} = sensing plate capacitance.

The coaxial cable is optional.

Fig 16. Typical application

The sampling rate is determined by the capacitance C_{CLIN} on pin CLIN. A higher sampling rate reduces the reaction time and increases the current consumption.

The sensing plate capacitance C_{SENS} may consist of a small metal area, for example behind an isolating layer. The sensing plate can be connected to a coaxial cable (C_{CABLE}) which in turn is connected to the input pin IN. Alternatively, the sensing plate can be directly connected to the input pin IN. An internal low pass filter is used to reduce RF interference. An additional low pass filter consisting of a resistor R_F and capacitor C_F can be added to the input to further improve RF immunity as required. For good performance, the total amount of capacitance on the input (C_{SENS} + C_{CABLE} + C_F) should be in the proper range, the optimum point being around 30 pF. These conditions allow the control loop to adapt to the static capacitance on C_{SENS} and to compensate for slow changes in the sensing plate capacitance. A higher capacitive input loading is possible if an additional discharge resistor R_C is placed as shown in Figure 16. Resistor R_C simply reduces the discharge time such that the internal timing requirements are fulfilled.

The sensitivity of the sensor can be influenced by the sensing plate area and capacitor C_{CPC}. The sensitivity is significantly reduced when C_{CPC} is reduced. When maximum sensitivity is desired C_{CPC} can be increased, but this also increases sensitivity to interference. Pin CPC has high-impedance and is sensitive to leakage currents.

3. For further information, see Ref. 4 “AN10832”. Information about the appropriate evaluation board can be found in Ref. 13 “UM10370”.

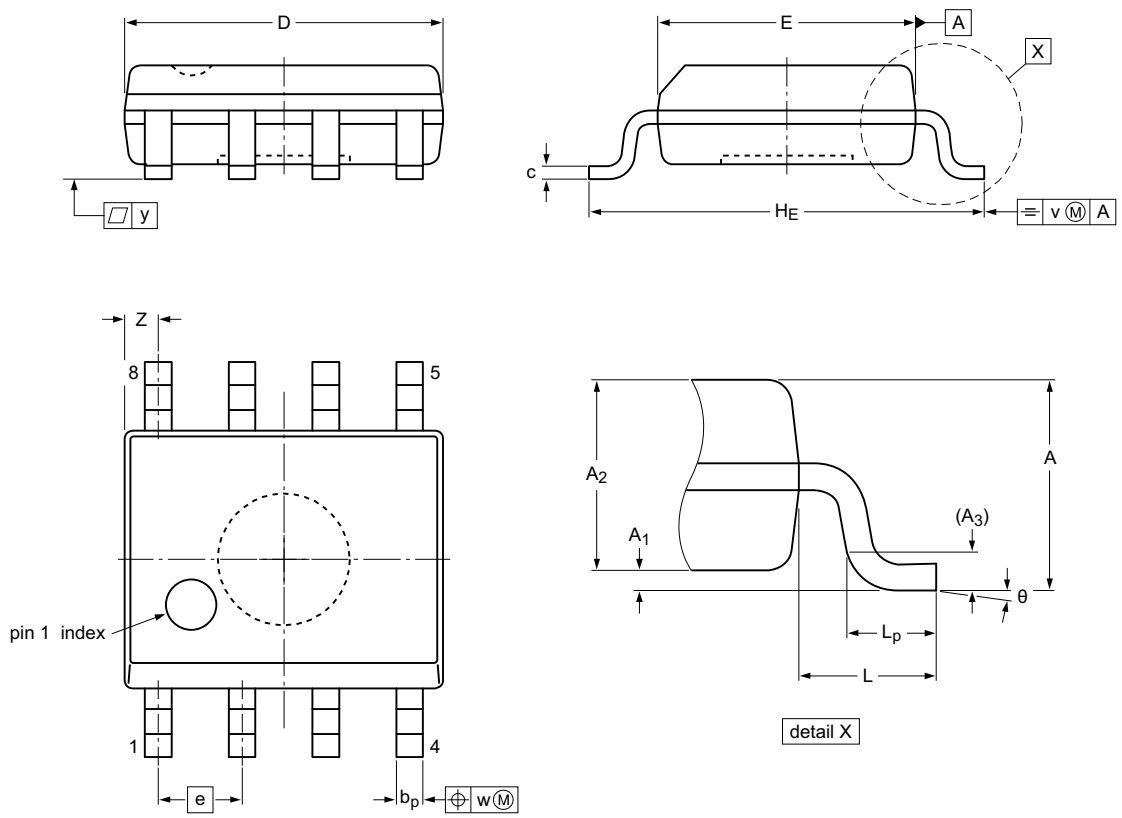
Remark: C_{CPC} should be a high-quality foil or ceramic capacitor, for example an X7R type.

When limiting the maximum input capacitance to 35 pF and the minimum operating temperature to −20 °C then the minimum operating voltage can be reduced to 2.8 V. The main limitation when lowering the supply voltage is a reduction in the range of the $V_{I(CPC)}$ voltage, which is specified from 0.6 V to V_{DD} − 0.3 V. Reducing the $V_{I(CPC)}$ working range is equivalent to reducing the input capacitance range. Additionally, $V_{I(CPC)}$ increases with decreasing temperature, as illustrated in Figure 14 and Figure 15. This means that it is possible to lower the supply voltage if the minimum temperature will be raised accordingly.

For the choice of proper component values for a given application, the component specifications in Table 6 and Table 7 must be followed.

15. Package outline

SOIC8: plastic small outline package; 8 leads; body width 3.9 mm PCF8883T



Dimensions

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	max	1.73	0.25	1.48		0.49	0.249	5.0	3.99		6.2		0.86				0.7	8°
	nom				0.25					1.27		1.05		0.25	0.25	0.1		
	min	1.37	0.10	1.27		0.36	0.190	4.8	3.82		5.8		0.41				0.3	0°
inches	max	0.068	0.0098	0.0582		0.019	0.0098	0.196	0.157		0.244		0.034				0.028	8°
	nom				0.01					0.05		0.041		0.01	0.01	0.004		
	min	0.054	0.0040	0.0500		0.014	0.0075	0.189	0.150		0.229		0.016				0.012	0°

Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

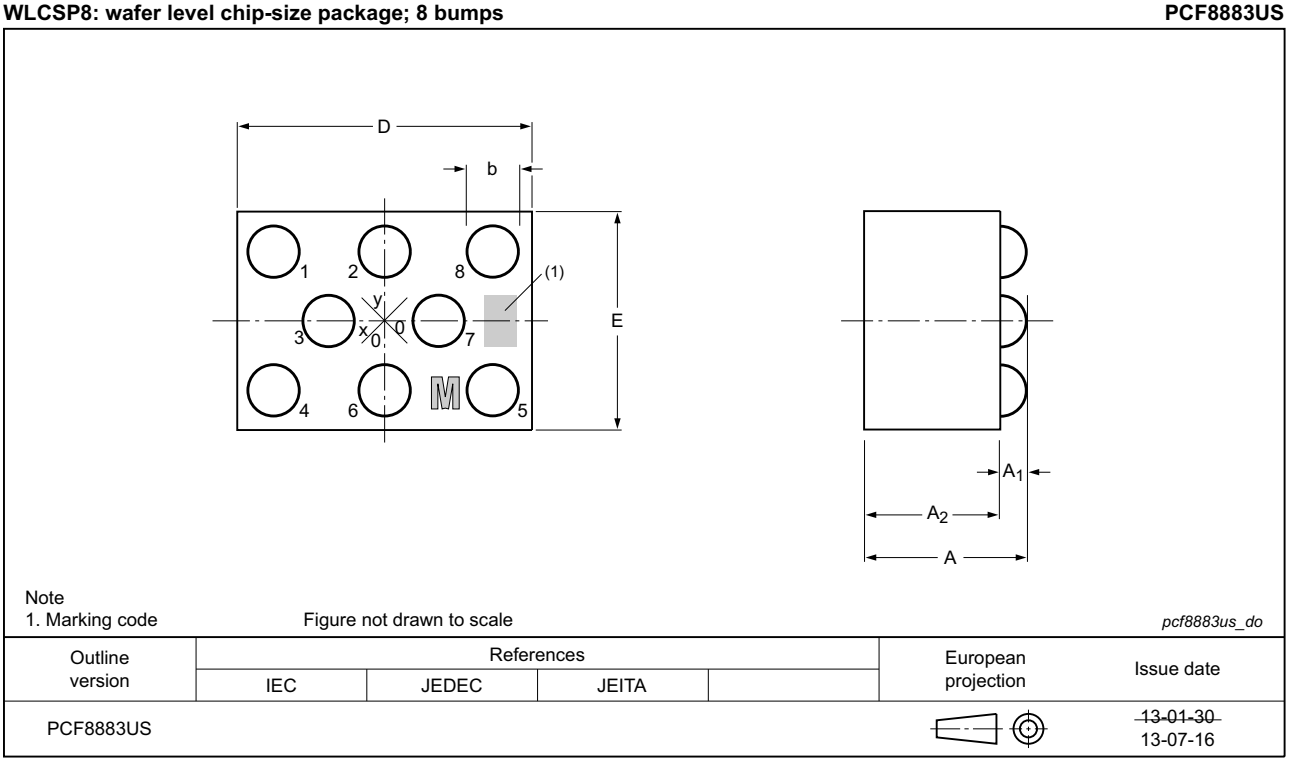
pcf8883t_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
PCF8883T		MS-012-AA				~~09-06-03~~ 11-11-04

Fig 17. Package outline of PCF8883T (SOIC8)

16. Bare die outline

WLCSP8: wafer level chip-size package; 8 bumps **PCF8883US**



Note
1. Marking code

Figure not drawn to scale

pcf8883us_do

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
PCF8883US						~~13-01-30~~ 13-07-16

Fig 18. WLCSP8 outline of PCF8883US

Table 8. Dimension of PCF8883US

Original dimensions are in mm.

Unit (mm)	A	A_1	A_2	b	D	E
max	-	-	-	-	1.19	0.89
nom	0.55	0.11	0.44	0.2	1.16	0.86
min	-	-	-	-	1.13	0.83

Table 9. Solder bump locations

All coordinates are in μm and referenced to the center of the die (see Figure 18).

Symbol	Pin	X	Y	Type	Description
IN	1	–430	280	analog input/ output	sensor input
TYPE	2	0	280	input	pin OUT behavior configuration input
CPC	3	–225	0	analog input/ output	sensitivity setting
V_{SS}	4	–430	–280	supply	ground supply voltage
V_{DD}	5	430	–280	supply	supply voltage
OUT	6	0	–280	output	switch output
CLIN	7	225	0	analog input/ output	sampling rate setting
$V_{DD(INTREGD)}$	8	430	280	supply	internal regulated supply voltage output

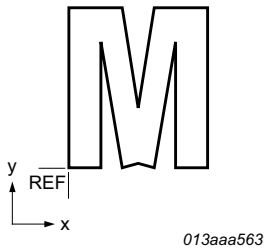


Fig 19. Alignment mark of the PCF8883US die (for location and dimension see Table 10)

Table 10. Alignment mark dimension and location

Coordinates	
x	**y**
Location[1]	
172 μm	−371 μm
Dimension[2]	
117 μm	131 μm

[1] The x/y coordinates of the alignment mark location represent the position of the REF point (see Figure 19) with respect to the center (x/y = 0) of the chip.

[2] The x/y values of the dimensions represent the extensions of the alignment mark in direction of the coordinate axis (see Figure 19).

17. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

18. Packing information

18.1 Tape and reel information

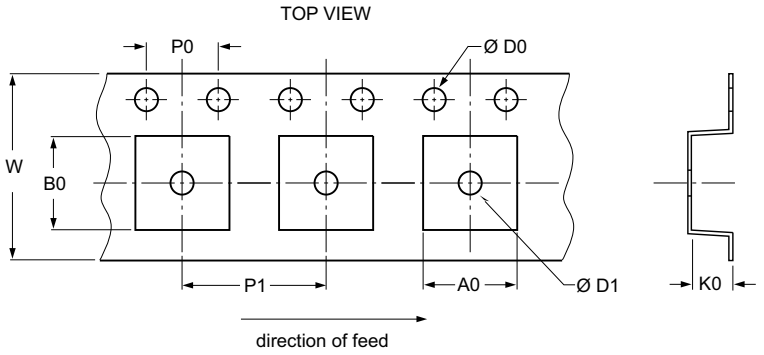


Fig 20. Tape and reel details for PCF8883T

Table 11. Carrier tape dimensions of PCF8883T

Nominal values without production tolerances.

Symbol	Description	Value	Unit
Compartments			
A0	pocket width in x direction	6.3 to 6.5	mm
B0	pocket width in y direction	5.4	mm
K0	pocket depth	2.05 to 2.1	mm
P1	pocket hole pitch	8	mm
D1	pocket hole diameter	1.5	mm
Overall dimensions			
W	tape width	12	mm
D0	sprocket hole diameter	1.5 to 1.55	mm
P0	sprocket hole pitch	4	mm

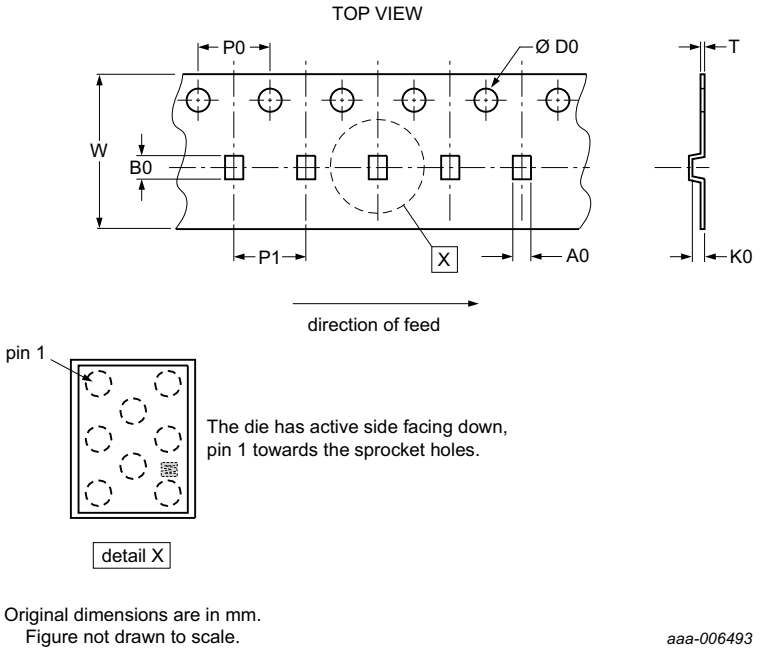


Fig 21. Tape and reel details for PCF8883US

Table 12. Carrier tape dimensions of PCF8883US

Nominal values without production tolerances.

Symbol	Description	Value	Unit
Compartments			
A0	pocket width in x direction	0.96	mm
B0	pocket width in y direction	1.37	mm
K0	pocket depth	0.77	mm
Overall dimensions			
W	tape width	8	mm
T	tape thickness	0.2	mm
D0	sprocket hole diameter	1.5	mm
P0	sprocket hole pitch	4	mm

19. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

19.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

19.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

19.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

19.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 22) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 13 and 14

Table 13. SnPb eutectic process (from J-STD-020D)

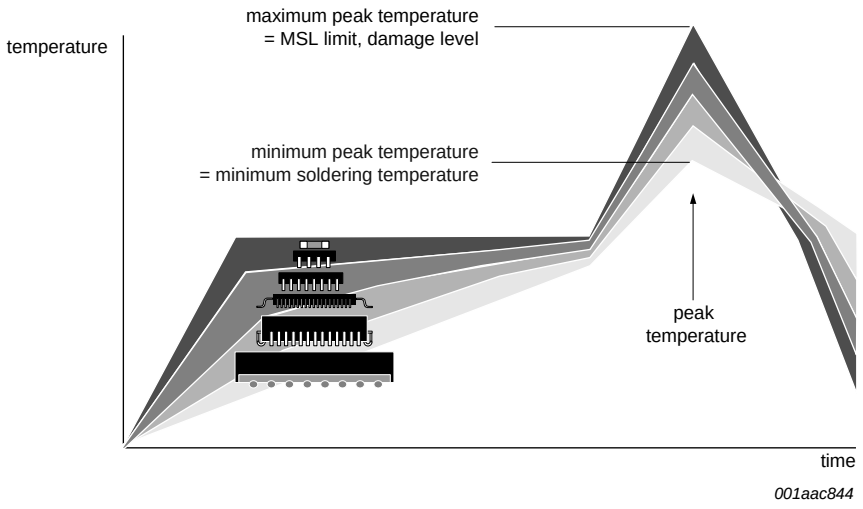
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 14. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 22.



MSL: Moisture Sensitivity Level

Fig 22. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

20. Soldering of WLCSP packages

20.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note *AN10439 "Wafer Level Chip Scale Package"* and in application note *AN10365 "Surface mount reflow soldering description"*.

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

20.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

20.3 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 23) than a SnPb process, thus reducing the process window

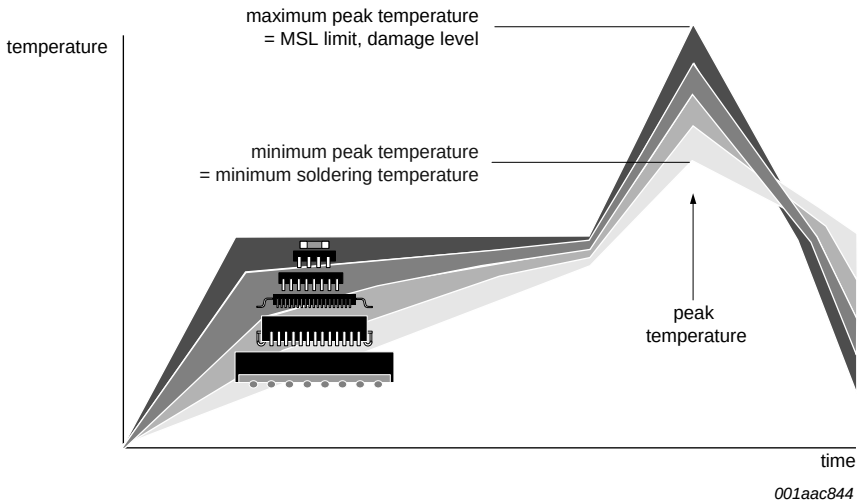
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 15.

Table 15. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 23.



MSL: Moisture Sensitivity Level

Fig 23. Temperature profiles for large and small components

For further information on temperature profiles, refer to application note *AN10365 "Surface mount reflow soldering description"*.

20.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate

- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

20.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

20.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note *AN10365 “Surface mount reflow soldering description”*.

20.3.4 Cleaning

Cleaning can be done after reflow soldering.

21. Abbreviations

Table 16. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
HBM	Human Body Model
IC	Integrated Circuit
MM	Machine Model
MOS	Metal Oxide Semiconductor
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
MSL	Moisture Sensitivity Level
PCB	Printed-Circuit Board
RC	Resistance-Capacitance
RF	Radio Frequency
SMD	Surface Mount Device

22. References

[1] **AN10365 —** Surface mount reflow soldering description

[2] **AN10439 —** Wafer Level Chip Size Package

[3] **AN10706 —** Handling bare die

[4] **AN10832 —** PCF8883 - capacitive proximity switch with auto-calibration

[5] **AN11122 —** Water and condensation safe touch sensing with the NXP capacitive touch sensors

[6] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[7] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[8] **IPC/JEDEC J-STD-020D —** Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

[9] **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[10] **JESD22-A115 —** Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)

[11] **JESD78 —** IC Latch-Up Test

[12] **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[13] **UM10370 —** PCF8883 evaluation board

[14] **UM10569 —** Store and transport requirements

23. Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF8883 v.4.1	20160914	Product data sheet	-	PCF8883 v.4
Modifications:	• Figure 3: Clarified top/bottom view of WLCSP8			
PCF8883 v.4	20140317	Product data sheet	-	PCF8883 v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Emphasized the X7R statement (Section 14) • Added Section 9 • Added Input or input/output statement in Table 4			
PCF8883 v.3	20130423	Product data sheet	-	PCF8883 v.2
PCF8883 v.2	20110308	Product data sheet	-	PCF8883_1
PCF8883 v.1	20091016	Product data sheet	-	-

24. Legal information

24.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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ICs with capacitive sensing functionality

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