64-Channel Serial to Parallel Converter With High Voltage Push-Pull Outputs

Features

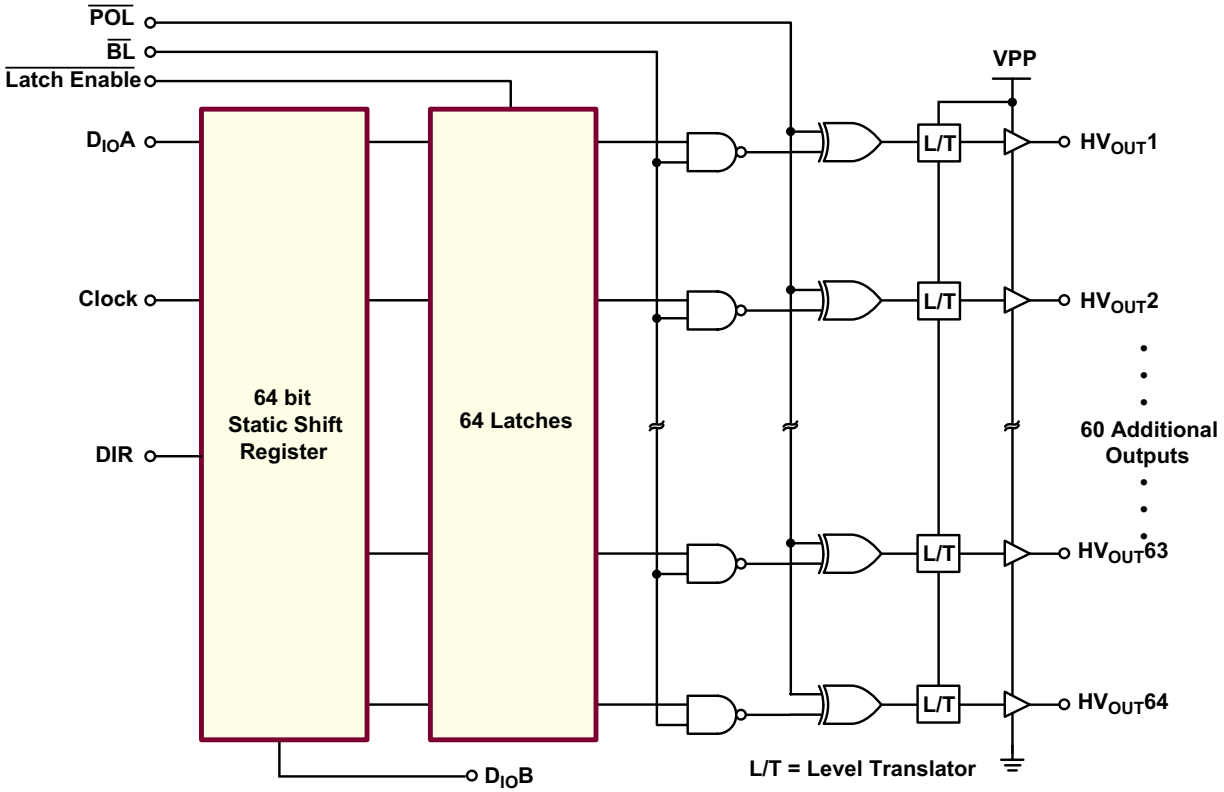
- Processed with HVCMOS® technology
- Operating output voltages to 300V
- Low power level shifting from 5.0 to 300V
- Shift register speed: 8.0MHz @ V_{DD} = 5.0V
- 64 latched data outputs
- Output polarity and blanking
- CMOS compatible inputs
- Foreward and reverse shifting options

General Description

The HV507 is a low voltage serial to high voltage parallel converter with 64 push-pull outputs. This device has been designed for use as a printer driver for electrostatic applications. It can also be used in any application requiring multiple output, high voltage, low current sourcing and sinking capabilities.

The device consists of a 64-bit shift register, 64 latches, and control logic to perform the polarity select and blanking of the outputs. A DIR pin controls the direction of data shift through the device. With DIR grounded, $D_{IO}A$ is Data-In and $D_{IO}B$ is Data-Out; data is shifted from $HV_{OUT}64$ to $HV_{OUT}1$. When DIR is at logic high, $D_{IO}B$ is Data-In and $D_{IO}A$ is Data-Out: data is then shifted from $HV_{OUT}1$ to $HV_{OUT}64$. Data is shifted through the shift register on the low to high transition of the clock. Data output buffers are provided for cascading devices. Operation of the shift register is not affected by the $\overline{LE}$ (latch enable), $\overline{BL}$ (blanking), or the $\overline{POL}$(polarity) inputs. Transfer of data from the shift register to the latch occurs when the $\overline{LE}$ is high. The data in the latch is stored during $\overline{LE}$ transition from high to low.

Functional Block Diagram



Ordering Information

Device	Package Option
	80-Lead Quad Plastic Gullwing *20.00x14.00mm body* *3.40mm height (max)* *0.65mm pitch*
HV507	HV507PG-G

-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

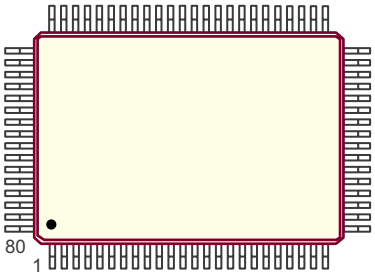
Parameter	Value
Supply voltage, V_{DD}	-0.5V to +6.0V
Supply voltage, V_{PP}	V_{DD} to +320V
Logic input levels	-0.5V to V_{DD} +0.5V
Ground current[2]	0.5A
High voltage supply current[1]	0.5A
Continuous total power dissipation[2]	1200mW
Operating temperature range	0°C to +70°C
Storage temperature range	-65°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to GND.

Notes:

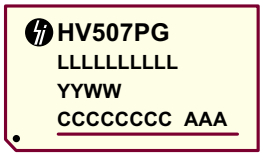
1. *Connection to all power and ground pads is required. Duty cycle is limited by the total power dissipated in the package.*
2. *For operation above 25°C ambiant derate linearly to 70°C at 26.7mW/°C.*

Pin Configuration



80-Lead Quad Plastic Gullwing (PG)
(top view)

Product Marking



L = Lot Number
YY = Year Sealed
WW = Week Sealed
C = Country of Origin
A = Assembler ID
____= "Green" Packaging

80-Lead Quad Plastic Gullwing (PG)

Recommended Operating Conditions

Sym	Parameter	Min	Typ	Max	Units
V_{DD}	Logic supply voltage	4.5	5.0	5.5	V
V_{PP}	High voltage supply	60	-	300	V
V_{IH}	High-level input voltage	V_{DD}-0.9	-	V_{DD}	V
V_{IL}	Low-level input voltage	0	-	0.9	V
T_A	Operating free-air temperature	0	-	+70	°C

Power-up sequence should be the following:

1. *Connect ground*
2. *Apply V_{DD}*
3. *Set all inputs (Data, CLK, Enable, etc.) to a known state*
4. *Apply V_{PP}*
5. *The V_{PP} should not drop below V_{DD} or float during operation.*

Power-down sequence should be the reverse of the above.

Electrical Characteristics

DC Characteristics *(For V_{DD} = 5.0V, V_{PP} = 300V, T_A = 25°C)*

Sym	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current		-	15	mA	f_{CLK} = 8.0MHz, F_{DATA} = 4.0MHz, $\overline{LE}$ = low
I_{DDQ}	Quiescent V_{DD} supply current		-	200	µA	All V_{IN} = 0 or V_{DD}
I_{PP}	High voltage supply current		-	0.50	mA	V_{PP} = 300V. All outputs high.
			-	0.50		V_{PP} = 300V. All outputs low.
I_{IH}	High-level logic input current		-	10	µA	V_{IH} = V_{DD}
I_{IL}	Low-level logic input current		-	-10	µA	V_{IL} = 0V
V_{OH}	High level output	HV_{OUT}	265	-	V	V_{PP} = 300V, IHV_{OUT} = -1.0mA, ID_{OUT} = -100µA
		Data Out	V_{DD} -1.0V	-		
V_{OL}	Low level output	HV_{OUT}	-	35	V	V_{DD} = 5.0V, IHV_{OUT} = +1.0mA,
		Data Out	-	1.0		ID_{OUT} = +100µA
V_{OC}	HV_{OUT} clamp voltage		-	V_{PP} +1.5V	V	I_{OC} = +1.0mA
			-	-30		I_{OC} = -1.0mA

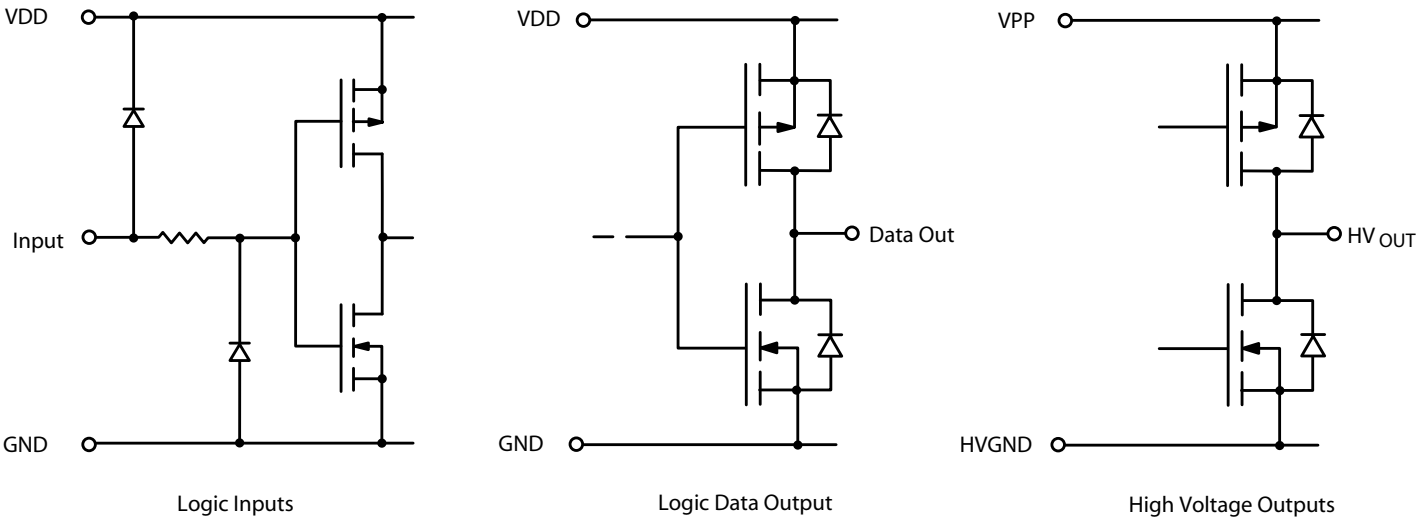
AC Characteristics[1] *(For V_{DD} = 5.0V, V_{PP} = 300V, T_A = 25°C)*

Sym	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency	-	8.0	MHz	---
t_W	Clock width high or low	62	-	ns	---
t_{SU}	Data set-up time before clock rises	35	-	ns	---
t_H	Data hold time after clock rises	30	-	ns	---
t_{WLE}	$\overline{LE}$ pulse width	80	-	ns	---
t_{DLE}	Delay time clock to $\overline{LE}$ high to low	35	-	ns	---
t_{SLE}	$\overline{LE}$ set-up time before clock rises	40	-	ns	---
t_{ON}, t_{OFF}	Time from $\overline{LE}$ to HV_{OUT}	-	4.0	µs	C_L = 20pF
t_{DHL}	Delay time clock to data high to low	-	125	ns	C_L = 20pF
t_{DLH}	Delay time clock to data low to high	-	125	ns	C_L = 20pF
t_R, t_F	All logic inputs	-	5.0	ns	---

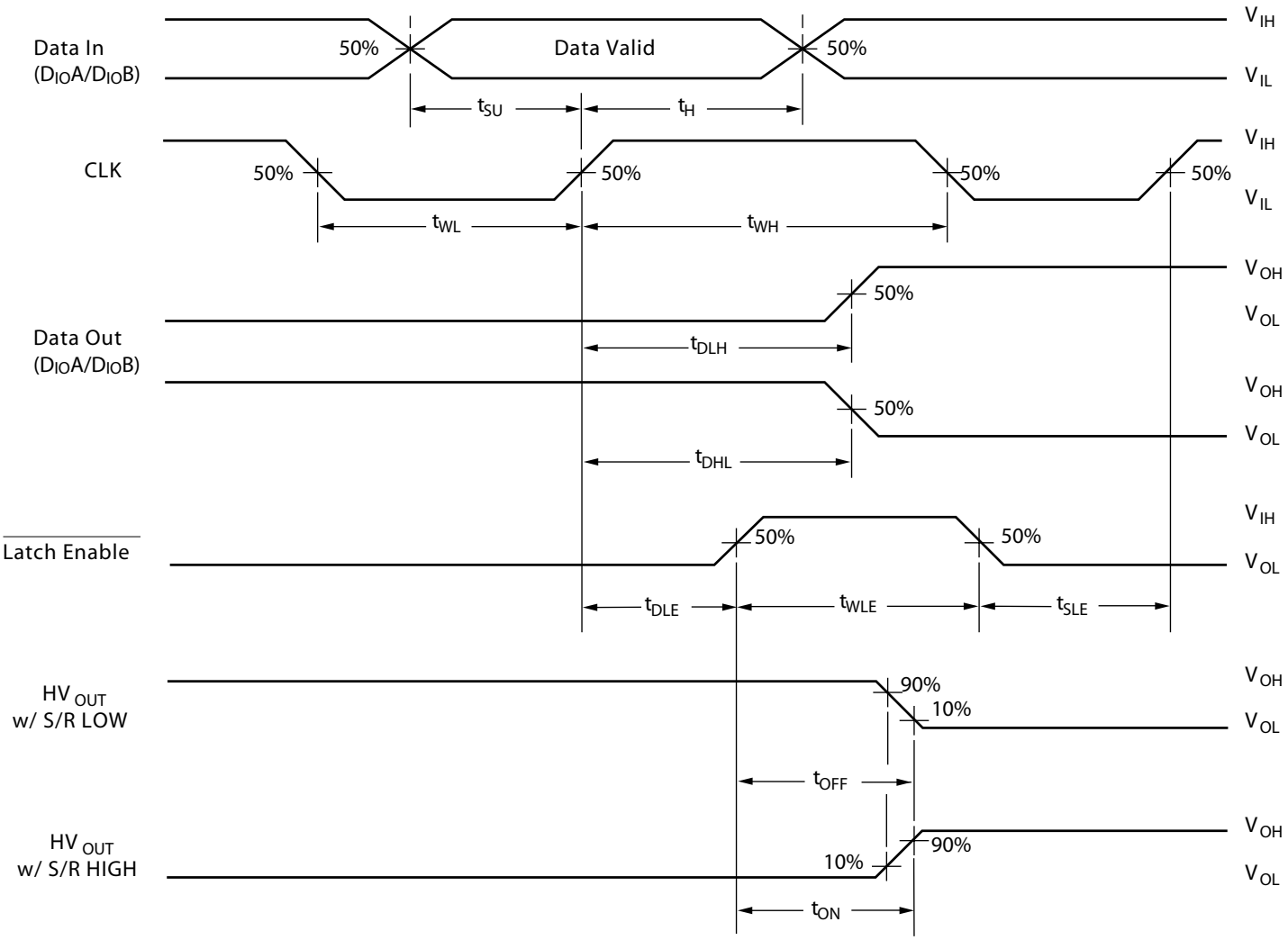
Note:

1. *Shift register speed can be as low as DC as long as data set-up and hold time meet the spec.*

Input and Output Equivalent Circuits



Switching Waveforms



Function Table

Function	Inputs						Outputs				
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	DIR	Shift Reg		HV Outputs		Data Out
							1	2...64	1	2...64	*
All on	X	X	X	L	L	X	*	*...*	H	H...H	*
All off	X	X	X	L	H	X	*	*...*	L	L...L	*
Invert mode	X	X	L	H	L	X	*	*...*	$\overline{*}$	$\overline{*...*}$	*
Load S/R	H or L	↑	L	H	H	X	H or L	*...*	*	*...*	*
Store data in latches	X	X	↓	H	H	X	*	*...*	*	*...*	*
	X	X	↓	H	L	X	*	*...*	$\overline{*}$	$\overline{*...*}$	*
Transparent latch mode	L	↑	H	H	H	X	L	*...*	L	*...*	*
	H	↑	H	H	H	X	H	*...*	H	*...*	*
I/O Relation	$D_{IO}A$	↑	X	X	X	L	$Q_N\rightarrow$	Q_{N+1}	-		$D_{IO}B$
	$D_{IO}B$	↑	X	X	X	H	$Q_N\rightarrow$	Q_{N+1}	-		$D_{IO}A$

Notes:

H = high level, L = low level = 0V, X = irrelevant, ↓ = high-to-low transition, ↑ = low-to-high transition.

* = dependent on previous stage's state before the last CLK high-to-low transition or last $\overline{LE}$ high.

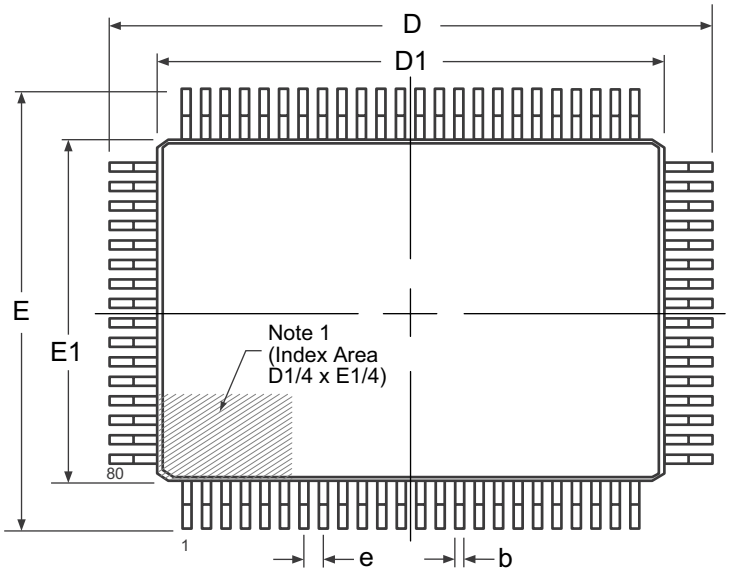
Pin Description (80-Lead PQFP)

Pin #	Function
1	$HV_{OUT}41$
2	$HV_{OUT}42$
3	$HV_{OUT}43$
4	$HV_{OUT}44$
5	$HV_{OUT}45$
6	$HV_{OUT}46$
7	$HV_{OUT}47$
8	$HV_{OUT}48$
9	$HV_{OUT}49$
10	$HV_{OUT}50$
11	$HV_{OUT}51$
12	$HV_{OUT}52$
13	$HV_{OUT}53$
14	$HV_{OUT}54$
15	$HV_{OUT}55$
16	$HV_{OUT}56$
17	$HV_{OUT}57$
18	$HV_{OUT}58$
19	$HV_{OUT}59$
20	$HV_{OUT}60$
21	$HV_{OUT}61$
22	$HV_{OUT}62$
23	$HV_{OUT}63$
24	$HV_{OUT}64$
25	VPP
26	$D_{IO}A$
27	N/C
28	N/C
29	$\overline{BL}$
30	$\overline{POL}$
31	VDD
32	DIR
33	GND
34	HVGND
35	N/C
36	N/C
37	CLK
38	$\overline{LE}$
39	$D_{IO}B$
40	VPP

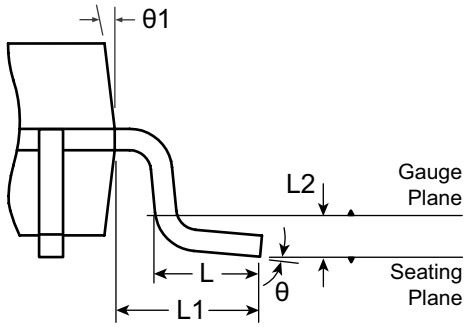
Pin #	Function
41	$HV_{OUT}1$
42	$HV_{OUT}2$
43	$HV_{OUT}3$
44	$HV_{OUT}4$
45	$HV_{OUT}5$
46	$HV_{OUT}6$
47	$HV_{OUT}7$
48	$HV_{OUT}8$
49	$HV_{OUT}9$
50	$HV_{OUT}10$
51	$HV_{OUT}11$
52	$HV_{OUT}12$
53	$HV_{OUT}13$
54	$HV_{OUT}14$
55	$HV_{OUT}15$
56	$HV_{OUT}16$
57	$HV_{OUT}17$
58	$HV_{OUT}18$
59	$HV_{OUT}19$
60	$HV_{OUT}20$
61	$HV_{OUT}21$
62	$HV_{OUT}22$
63	$HV_{OUT}23$
64	$HV_{OUT}24$
65	$HV_{OUT}25$
66	$HV_{OUT}26$
67	$HV_{OUT}27$
68	$HV_{OUT}28$
69	$HV_{OUT}29$
70	$HV_{OUT}30$
71	$HV_{OUT}31$
72	$HV_{OUT}32$
73	$HV_{OUT}33$
74	$HV_{OUT}34$
75	$HV_{OUT}35$
76	$HV_{OUT}36$
77	$HV_{OUT}37$
78	$HV_{OUT}38$
79	$HV_{OUT}39$
80	$HV_{OUT}40$

80-Lead PQFP Package Outline (PG)

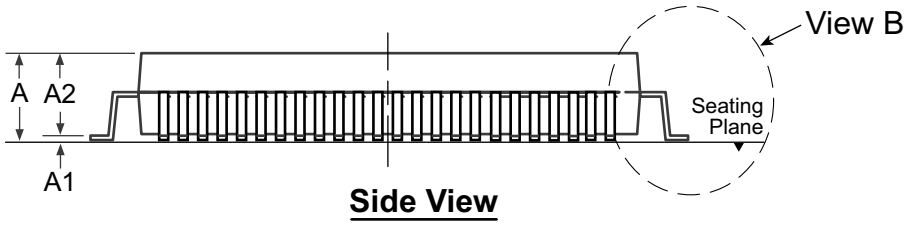
20.00x14.00mm body, 3.40mm height (max), 0.80mm pitch, 3.90mm footprint



Top View



View B



Side View

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ	θ1
Dimen-sion (mm)	MIN	2.80*	0.25	2.55	0.30	23.65*	19.80*	17.65*	13.80*	0.80 BSC	0.73	1.95 REF	0.25 BSC	0°	5°
	NOM	-	-	2.80	-	23.90	20.00	17.90	14.00		0.88			3.5°	-
	MAX	3.40	0.50*	3.05	0.45	24.15*	20.20*	18.15*	14.20*		1.03			7°	16°

JEDEC Registration MO-112, Variation CB-1, Issue B, Sept.1995.
** This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.*
Drawings not to scale.
***Supertex Doc. #:** DSPD-80PQFPPG, Version B101708.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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