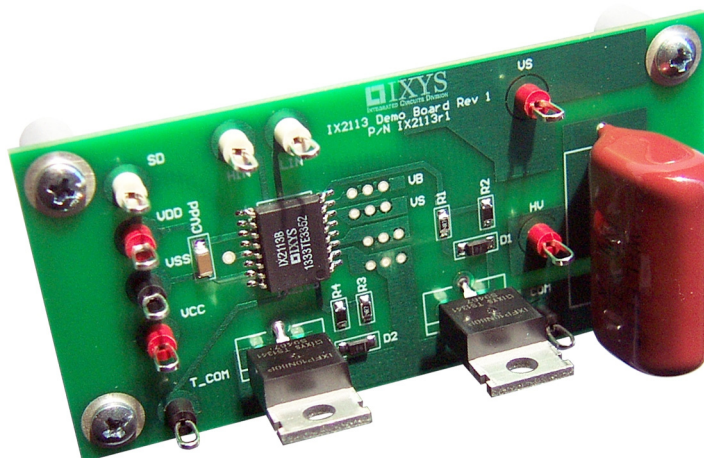


1. Introduction



IXYS Integrated Circuits Division's IX2113 Evaluation Board contains all the necessary circuitry to demonstrate the features of a high voltage gate driver configured as a half-bridge driver. The IX2113 has independent high-side and low-side referenced output channels, both of which are capable of sourcing and sinking 2A peak current. The floating high-side channel can drive MOSFETs or IGBTs up to 600V from the common reference. In addition, when a fault or an over-current condition is detected, the shutdown (SD) pin can be used to terminate gate drive to the high-side or the low-side switch.

1.1 Features:

- Floating Channel for Bootstrap Operation up to 600V
- Outputs Capable of Sourcing and Sinking 2A Peak Current
- Gate Drive Supply Range: from 10V to 20V
- 3.3V Logic Compatibility Enables Seamless Interfacing with Microcontrollers
- Independent Under-voltage Lockout (UVLO) for High-side and Low-side Outputs
- Input Pins HIN, SD, LIN Include Schmitt Trigger for Better Noise Immunity
- High dV/dt Capability: 50V/ns
- Negative Voltage Transient Protection: -5V

Figure 1. Evaluation Board, Top View

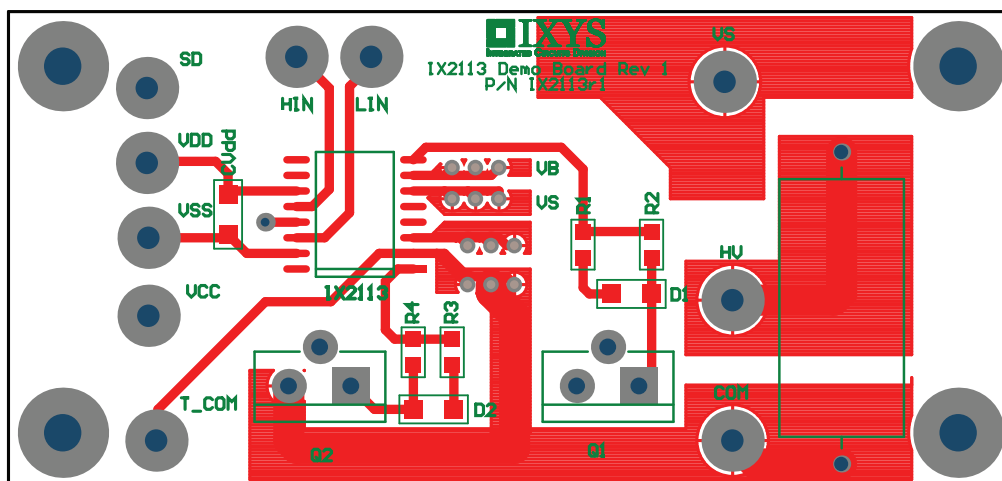
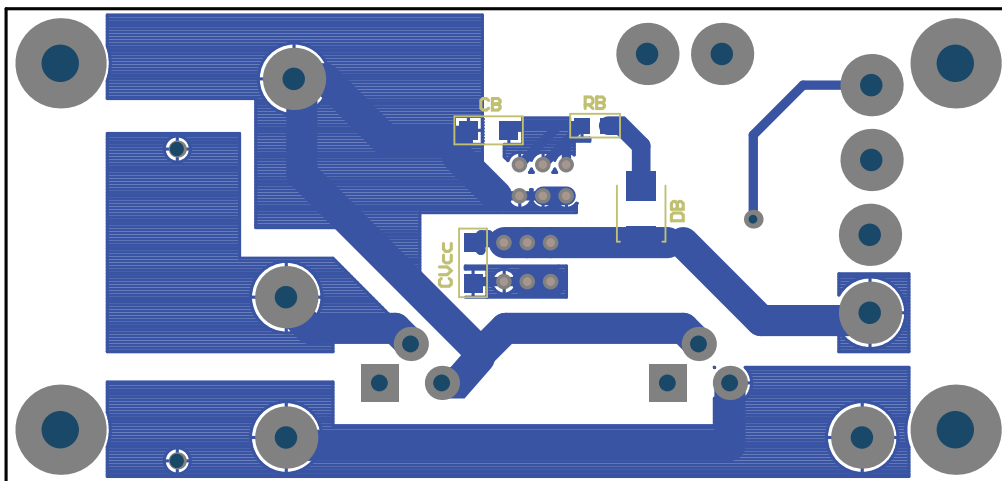


Figure 2. Evaluation Board, Bottom View



1.2 Evaluation Board Pin Descriptions

| Pin Name | Description |
|-----------------|---|
| HV | High Voltage Bus |
| V _S | High Side Floating Supply Return |
| V _{DD} | Logic Supply Voltage |
| V _{SS} | Logic Ground |
| V _{CC} | Low Side Fixed Supply Voltage |
| SD | Logic Input for Shutdown |
| HIN | Logic Input for High Side Gate Driver Output (HO) |
| LIN | Logic Input for Low Side Gate Driver Output (LO) |
| COM | Low Side Return |
| T_COM | Test Point Low Side Return |

1.3 Evaluation Board Bill of Materials

| Ref. Des. | Qty. | Description | Manufacturer | Mfr. P/N |
|--|------|----------------------------------|------------------|---------------------|
| U1 | 1 | High and Low Side Gate Driver | IXYS IC Division | IX2113B |
| Q1, Q2 | 2 | Polar HV MOSFET 800V 10A TO-220 | IXYS | IXFP10N80P |
| R2, R4 | 2 | RES 47 Ohm 1/8W 5% 0805 SMD | YAGEO | RC0805JR-0747RL |
| R1, R3, R _B | 3 | RES 4.7 Ohm 1/8W 5% 0805 SMD | YAGEO | RC0805JR-074R7L |
| D1, D2 | 2 | DIODE Fast Recovery 30V 1A Mini2 | PANASONIC | DB2230400L |
| D _B | 1 | DIODE Super Fast 600V 1A | Diodes Inc. | MURS160-13-F |
| CV _{CC} , CV _{DD} , C _B | 3 | CAP CER 0.33μF X7R 1206 | TDK | C3216X7R1H334K160AA |
| CVBUS | 1 | CAP FILM 0.56μF 630VDC Radial | Panasonic | P12270 |

2. Functional Description

The IX2113 demo board features a very inexpensive bootstrap circuit that provides power to the high-side drive channel. It consists of resistor, R_B , super-fast-recovery diode, D_B , and capacitor, C_B .

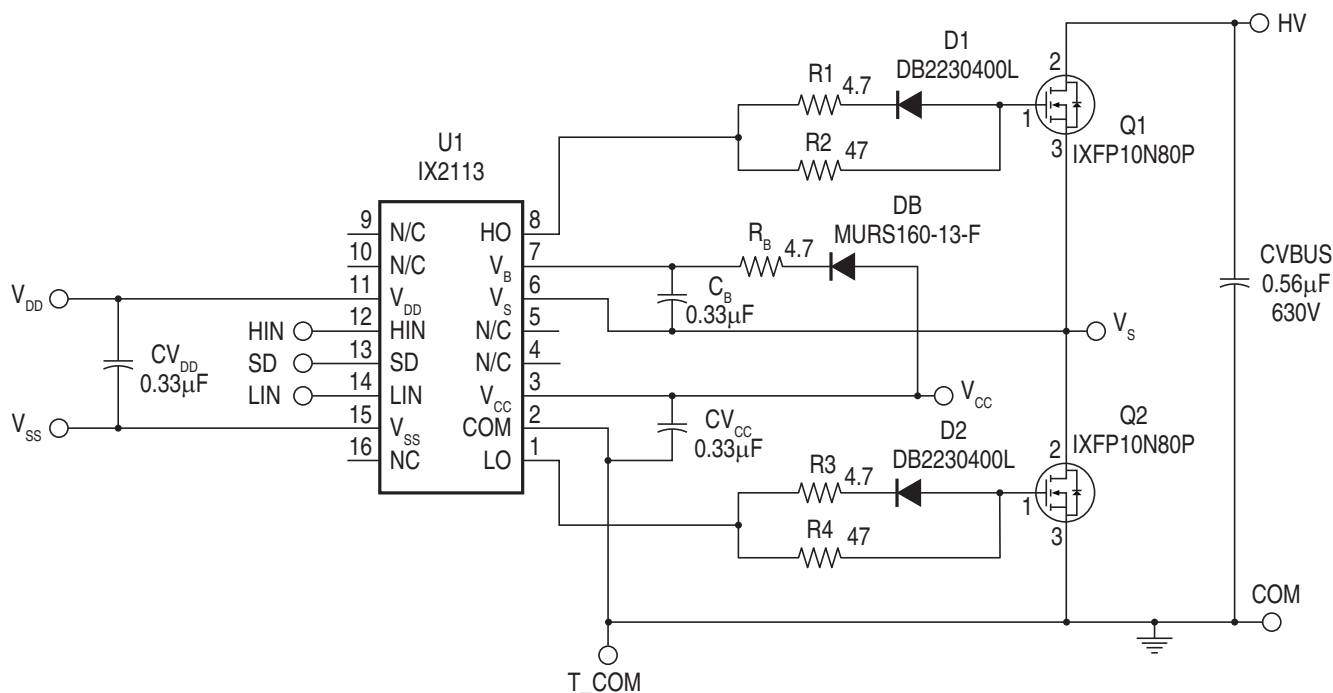
The sequence of bootstrap charging is as follows: When the V_S high side floating supply return is pulled below V_{CC} or is pulled down to COM by the load, the C_B bootstrap capacitor begins to charge through the R_B resistor and D_B diode from the V_{CC} supply. This charge continues until V_S is pulled up to a higher voltage than V_{CC} by the external high-side power MOSFET. V_{BS} (the difference voltage between V_B and V_S) starts to float, and the bootstrap diode begins to reverse bias and block the high HV voltage.

To start the Evaluation Board, provide necessary voltages to V_{CC} , V_{DD} , and HV and refer to the IX2113 data sheet for proper operating conditions. Connect the SD pin to a microcontroller or another logic device that can pull the SD pin high when the shutdown function is desired. If the SD pin is not to be used, then it should be connected to T_COM. Provide a PWM logic input signal to LIN and HIN making sure that signals have adequate dead time in order to prevent shorting HV to COM.

The IX2113 demo board includes R2 and R4 gate resistors, and, for fast turn off, D1/R1/R2 and D2/R3/R4 diode-resistor networks.

Note: The evaluation board does not have input reverse polarity protection. Applying a negative voltage at the HV Bus Supply or V_{CC} or V_{DD} may permanently damage the components on the board. In addition, when probing the high-side output, scope probe GND has to be isolated to prevent shorting the high-side output to GND.

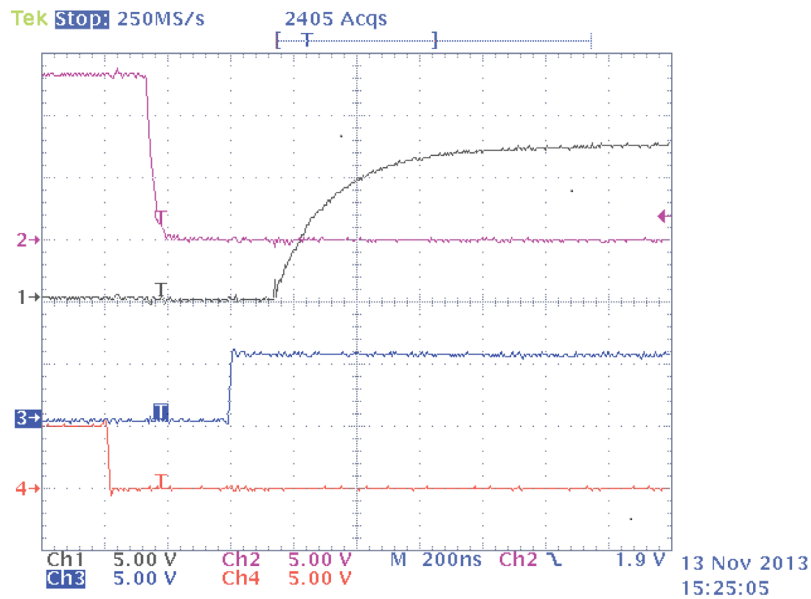
Figure 3. Evaluation Board Schematic



3. Operating Waveforms

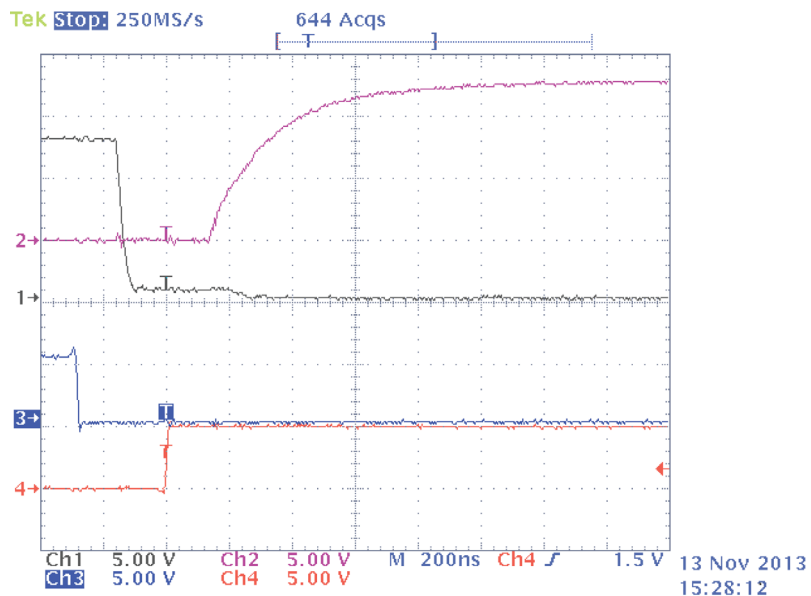
Waveforms 1: CH1: Q1 gate, CH2: Q2 gate, CH3: LIN Signal, CH4: HIN Signal

This scope capture shows the rising edge of the high-side MOSFET, Q1, and the falling edge of the low-side MOSFET, Q2. LIN and HIN waveforms have 400nS dead time.



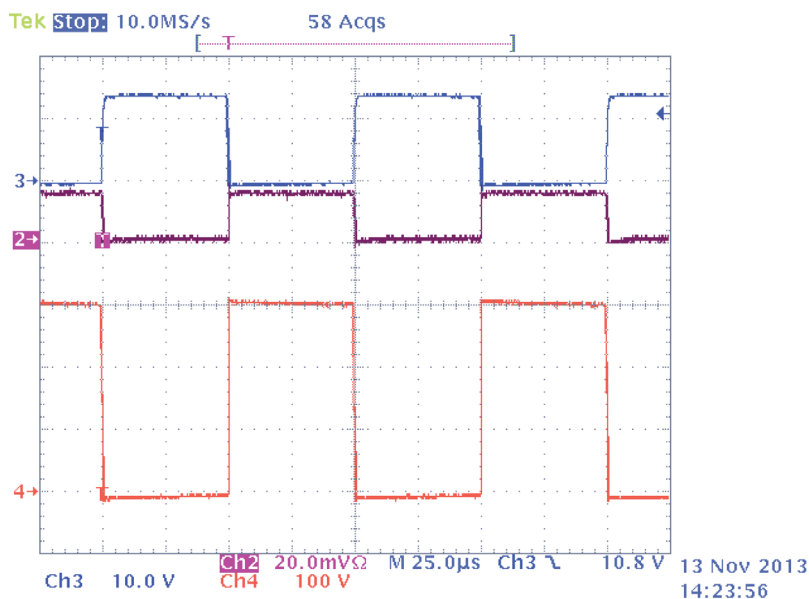
Waveforms 2: CH1: Q1 gate, CH2: Q2 gate, CH3: LIN Signal CH4: HIN Signal

This scope capture shows the falling edge of the high-side MOSFET, Q1, and the rising edge of the low-side MOSFET, Q2. LIN and HIN waveforms have 280nS dead time.



Waveforms 3: CH2: Load Current, CH3: Low Side MOSFET signal, CH4: VS High Side Floating Supply Return.

Scope capture demonstrating approximately 9W of power. A 10k Ω load resistor is attached from V_S to COM.



For additional information please visit www.ixysic.com

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