IES5501

Fast Dual Bi-Directional Bus Buffer

1 FEATURES

- Dual, bi-directional unity gain buffer
- Fast switching times allow operation in excess of 1MHz
- Supports I²C(1) bus (standard and fast mode), SMBus (standard and high power mode), PMbus and IPMB.
- Enable allows bus segments to be disconnected
- Low current stand-by mode when not enabled
- Application/removal of power to IC will not interfere with other bus activity
- 4 mA (static) pull-down capability supports a wide range of bus standards
- Low noise susceptibility
- Low input-output offset voltage
- Threshold and offset parameters allow the connection of several devices in series.
- Bus levels independent of supply voltage
- Operating voltages from 2.7 V to 5.5 V
- Wide range of bus voltages from 1.8 V to 15 V
- Level shifting between different bus voltages
- Achieves superior response times without the need for rise time accelerators

2 BLOCK DIAGRAM

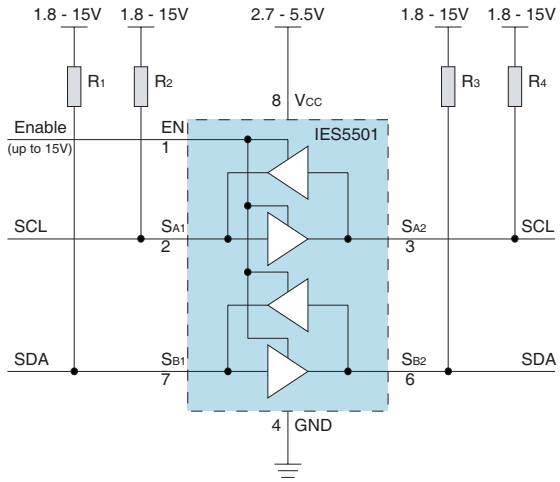

Fig.1 Block diagram

3 GENERAL DESCRIPTION

The IES5501 is a monolithic bipolar integrated circuit for bus buffering in applications including I²C, SMBus, PMbus, and other systems based on similar principles.

The buffer extends the bus load limit by buffering both the SCL and SDA lines. It supports up to 400 pF loads on each side of the buffer at 400kHz. Higher capacitance is supported at lower speeds, and lower capacitance at higher speeds up to 1MHz.

The enable function allows sections of the bus to be isolated. Individual parts of the system can be brought on-line sucessively. This means a controlled start-up using a diverse range of components, operating speeds and loads is easily achieved. Systems employing removable components on a back-plane (e.g. telecommunications racks) can use the enable pin and the high impedance ports on power-down to safely install and remove components in active systems.

Bus level translation between a very wide range of bus voltages, from 1.8 V to 15 V, is supported. This feature provides enormous flexibility in interfacing systems of different technologies.

The unique operation of the IES5501 provides one of the fastest response times of such bi-directional buffers, ensuring any glitches (common to other buffers) are kept well within the 50 ns I²C specification. Additionally, it does this without the need for “rise-time accelerators” which, combined with low noise margins, may cause glitches outside of the I²C specification.

4 APPLICATIONS

- Power Management Systems
- Telecommunications Systems including ATCA
- Desktop and Portable Computers including RAID
- Automotive Accessories (up to 15V)
- Building Automation
- TV / Projector / Monitor interconnection
- Game Consoles / Boxes
- CompactPCI
- Medical Systems
- Gaming Machine Networks
- Backplane Management / Interconnect

(1) I²C is a trademark of NXP Semiconductors

5 PINNING INFORMATION

5.1 Pinning layout

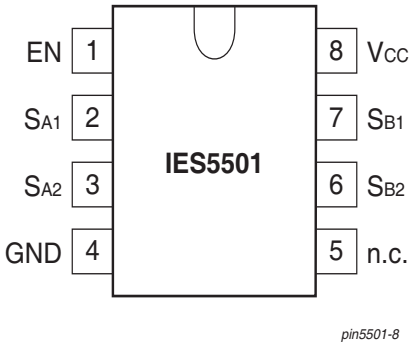

Fig.2 Pinning diagram (SO8 / MSOP8)

5.2 Pin description

SYMBOL	PIN	DESCRIPTION
EN	1	Enable
S_{A1}	2	Buffer A, Port 1 (SCLOUT)*
S_{A2}	3	Buffer A, Port 2 (SCLIN)*
GND	4	Supply Ground
n.c.	5	not connected
S_{B2}	6	Buffer B, Port 2 (SDAIN)*
S_{B1}	7	Buffer B, Port 1 (SDAOUT)*
V_{CC}	8	Positive supply

* Recommended I^2C bus orientation for device family compatibility.

6 FUNCTIONAL DESCRIPTION

6.1 V_{CC}, GND - DC supply pins

The power supply voltage for the IES5501 may be any voltage in the range 2.7 V to 5.5 V. The threshold level below which the output will begin to match the input is 33% of V_{CC}. Hence, the operating voltage should be chosen with the required bus voltage, switching threshold, and noise margins, in mind.

6.2 S_{A1}, S_{A2}, S_{B1}, S_{B2} - Buffer inputs/outputs

The two buffers (S_A and S_B) are identical and symmetrical. The buffers can be driven from either direction, with the same response. When port 1 of the buffer is being driven low (<0.33V_{CC}) by another device on the bus, port 2 will be driven low by the IC to provide the buffered output.

The “input” side is determined by the lowest externally driven signal. Therefore if port 1 is externally pulled to V_{Sx1} = 250 mV, and port 2 is externally pulled to V_{Sx2} = 500 mV, the buffer will pull port 2 down further such that it becomes $V_{Sx2} = V_{Sx1} + V_{OFFSET}$. Should port 2 subsequently become lower than port 1 by the amount of the offset voltage ($V_{Sx2} + V_{OFFSET} < V_{Sx1}$) by means of an external device pulling it low, control of the buffering operation will switch, and port 2 will become the “input”. The voltage at port 1 will then become $V_{Sx1} = V_{Sx2} + V_{OFFSET}$. When both ports are being held almost equal (less than an offset voltage) the external devices are effectively in control.

6.3 Enable - Activate Buffer Operations

The Enable input is used to disable the buffer, for the purpose of isolating sections of the bus. The IC should only be disabled when the bus is idle. This prevents truncation of commands which may confuse other devices on the bus.

Enable may also be used to progressively activate sections of the bus during system start-up. Bus sections slow to respond on power-up can be kept isolated from the main system to avoid interference and collisions.

The Enable pin may be pulled up higher than the Vcc of the buffer, further enhancing the capability of the IES5501 in a level shifting role. For example, a microprocessor could drive Enable, S_{A1} and S_{B1} at 5V, while the buffer V_{CC}, S_{A2} and S_{B2} ports are at 3.3V.

Similarly, the threshold level of the Enable pin allows a 1.8V device to disable an IES5501 with a V_{CC} of 3.3V.

The Enable pin includes an internal 2µA pull-down current which will act to disable the device, should the pin be left floating.

7 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134) Voltages are specified with respect to pin 4 (GND)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	Supply voltage range (V_{CC})		–0.3	+7	V
V_{Sxx}	Voltage range (S_{A1}, S_{A2}, S_{B1}, S_{B2})		–0.3	+16	V
V_{EN}	Voltage range (EN)		–0.3	+16	V
I	DC current (any pin)		–	20	mA
P_{tot}	total power dissipation		–	300	mW
T_{stg}	storage temperature		–55	+125	°C
T_{amb}	operating ambient temperature		–40	+85	°C

8 CHARACTERISTICS

All specifications apply over the full operating temperature range of T_{amb} = -40°C to +85°C;
Voltages are specified with respect to pin 4 (GND)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power supply						
V_{CC}	supply voltage (operating)		2.7	–	5.5	V
I_{CC}	supply current (operating)	V_{CC}= V_{EN}= 5.5V	–	4.3	5.9	mA
	supply current (stand-by)	V_{CC}= 5.5V, V_{EN} = 0V	–	150	210	µA
Buffer Ports						
V_{Sxx}	Bus voltage		1.8	-	15	V
V_{TL}	Input low threshold voltage		0.30V_{CC}	0.33V_{CC}	0.41V_{CC}	V
I_{IL}	Input low drive current	V_{Sxx} < V_{CC}	-	-8	-20	µA
I_{OL}	Output low sink current	$V_{Sxx(out)}$ = 0.4V	4	-	-	mA
V_{OFFSET}	Input-output offset voltage	I_{OL} = 4mA, $V_{Sxx(in)}$ = 50mV	-	140	220	mV
	(V_{CC} = 3.3V)	I_{OL} = 500µA, $V_{Sxx(in)}$ = 50mV	-	50	90	mV
		I_{OL} = 1.2mA, $V_{Sxx(in)}$ = 200mV	-	30	60	mV
I_{LEAK}	Leakage current	$V_{Sxx} \geq V_{CC}$	-	-	±5	µA
C_{Sxx}	Pin Capacitance	Note 1	-	-	10	pF
Enable						
V_{EN}	Enable active voltage		1.2	–	–	V
$V_{DISABLE}$	Disable (stand-by) voltage		–	–	0.8	V
I_{EN}	Input current	V_{EN} > 1.2V	1	-	3	µA
Timing Characteristics						
td	Response Delay	V_{CC} = 5V, V_{Sxx} = 5V,	–	90	–	ns
tf	Fall Time	$R_{Sxx(PULLUP)}$ = 1kohm	–	20	–	ns
f_{Sxx}	I^2C Operating Frequency		0	–	400	kHz
	Max. Operating Frequency		1000	–	–	kHz
t_{ENH}	Enable High to Sxx Active	Note 1	–	0.6	1.5	µs
t_{ENL}	Enable Low to Sxx Disabled	Note 1	–	0.4	1	µs

Note: 1) Guaranteed by design (Not subject to test)

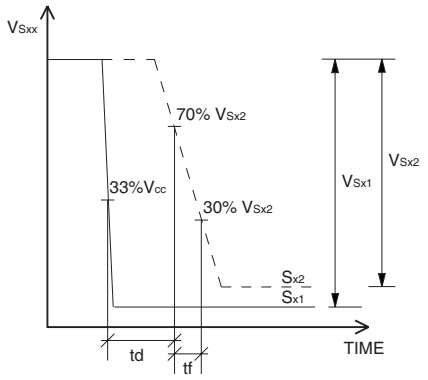

Fig.3 Timing Parameters

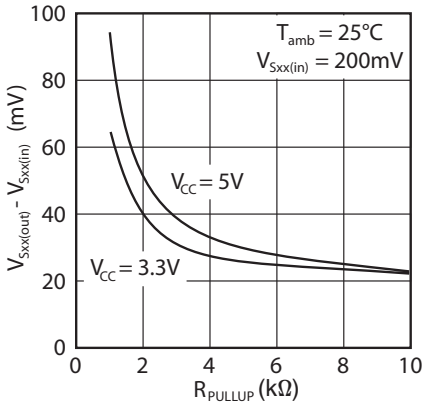

Fig.4 Offset Voltage, Vout - Vin

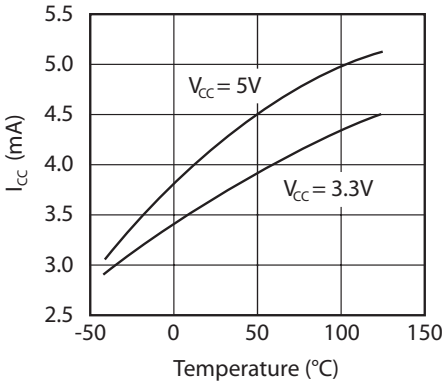

Fig.5 Supply Current vs Temperature

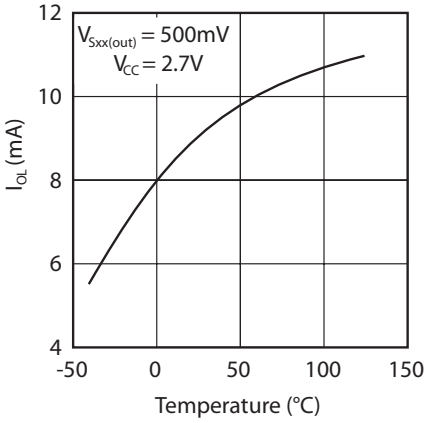

Fig.6 Output Low Sink Current vs Temperature

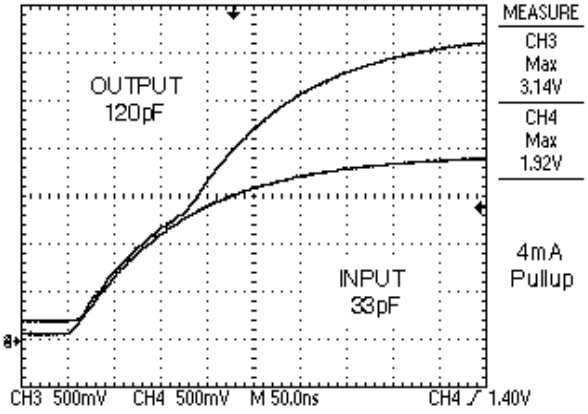

Fig.7 Rise time

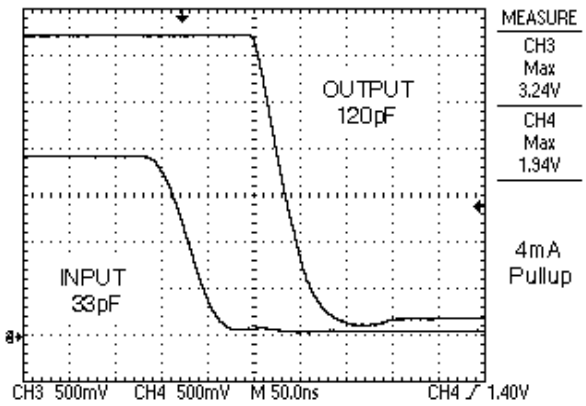

Fig.8 Fall time

9 APPLICATION INFORMATION

9.1 Design Considerations

Figure 9 shows the IES5501 level shifting signals from 1.8V to 3.3V at 1MHz clock speed. The IES5501 has excellent application to extending loads and providing interfaces to connectors on high speed microprocessor cards, well in excess of the "fast mode" 400kHz I²C bus specification(1). Rise times are determined simply by the side of the buffer with the slowest RC time constant.

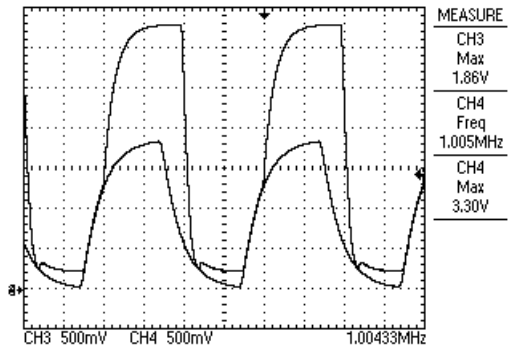

Fig.9 1.8V to 3.3V Level Shifting at 1MHz

Figure 10 shows a typical application for the IES5501. The IC can level shift between different bus voltages, without the need for external components. Higher bus voltages and currents outside the range of the standard I²C bus specification can be catered for, providing a longer range capability and higher noise immunity.

The enable pin can be used to interface buses of different operating frequencies. When certain bus sections are enabled the system frequency may be limited by a bus section having a slave device specified only to 100 kHz. When that bus section is disabled, the slow slave is isolated and the remaining bus can be run at 400 kHz. The timing performance and current sinking capability will allow the IES5501 to run well in excess of the 400 kHz maximum limit of the I²C fast mode.

Figure 11 shows the IES5501 used in a radial (star) configuration on an AdvancedTCA(2) Shelf Management Controller board (ShMC). The IES5501 is highly suited to this and other backplane applications, providing excellent noise margins and I2C compliant switching levels.

(1) "UM10204: I2C-bus Specification and User Manual", Rev 03, 19 June 2007, NXP B.V.

(2) Trademark of the PCI Industrial Computer Manufacturers Group (PICMG)

Peripheral cards (or Field Replaceable Units, FRU) and backplanes operating at a range of voltages can be interfaced together using a minimum of components.The IES5501 can be teamed with the IES5502 to achieve substantial noise margin gains across a system.

Multiplexers such as the PCA9544A are simple analog switches which provide no capacitive load isolation between connected branches. Figure 13 shows the IES5501 enhancing an I²C multiplexer application, by isolating the load capacitance of each branch. Figures 14 and 15 show alternate forms of bus multiplexing.

Similarly, the P82B715 I²C bus extender, which is commonly used for line driver applications, provides a "10x impedance transformation"(3) but does not isolate either side of the buffer. Figure 12 shows the IES5501 used to isolate the bus loading due to the P82B715. This greatly simplifies calculation of the pull-ups, increases the total system loading capability in extender applications, will meet the Fast Mode release requirement (when IES5501 and P82B715 V_{CC}'s share a common supply), and ensures the 300 ns risetime requirement can easily be met even if the cable bus rise is relatively slow.

Buffers are intended to extend total system capacitance above 400pF so anticipate high capacitance on each side. When loading on one side is small, adding 47pF is suggested to avoid any waveform ripple, should it occur.

9.2 Input to Output Offset Voltage Calculation

The offset voltage between the side acting as the output ($S_{xx(out)}$) and the side acting as the input ($S_{xx(in)}$) of the IES5501 can be calculated using the relationship:

$$V_{Sxx(out)} = V_{Sxx(in)} + 15mV + (V_{BUS}/R) \bullet 15[\Omega]$$

This calculation is valid for $V_{Sxx(in)} \geq 200mV$, as below this point the saturation voltage of the open collector output drive transistor will begin to affect the characteristic. Input and output voltages are shown in millivolts, V_{BUS} (the supply voltage to the bus) is in volts, and R is in ohms.

An example calculation for VBUS = 3.3V, V_{SA1} = 200mV, the resistance R pulling up S_{A2} is 2k, then the voltage on S_{A2} is typically:

$$V_{SA2} = 200mV + 15mV + (3.3/2000) \bullet 15$$
$$= 240mV$$

This can be compared with the offset characteristic shown in Figure 4.

(3) P82B715 I2C bus extender datasheet, 2 December 2003, Philips Electronics N.V.

9.3 Application circuits

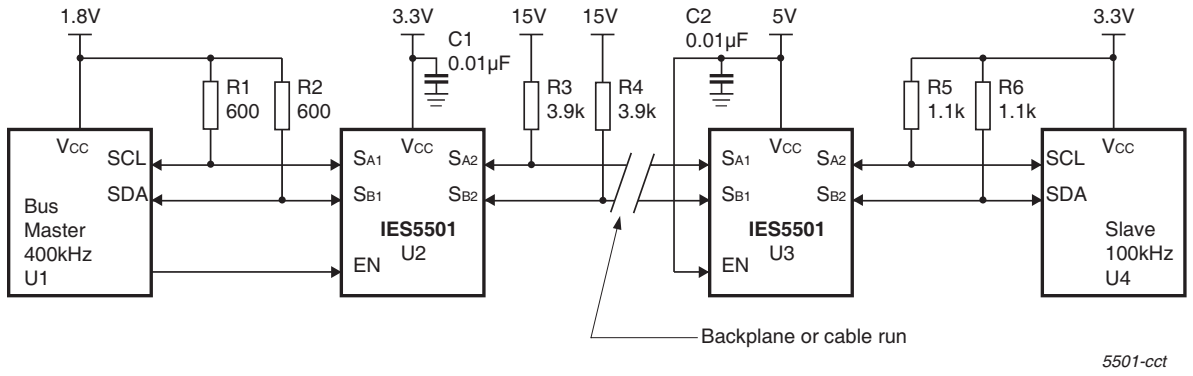

Fig.10 IES5501 typical buffer application

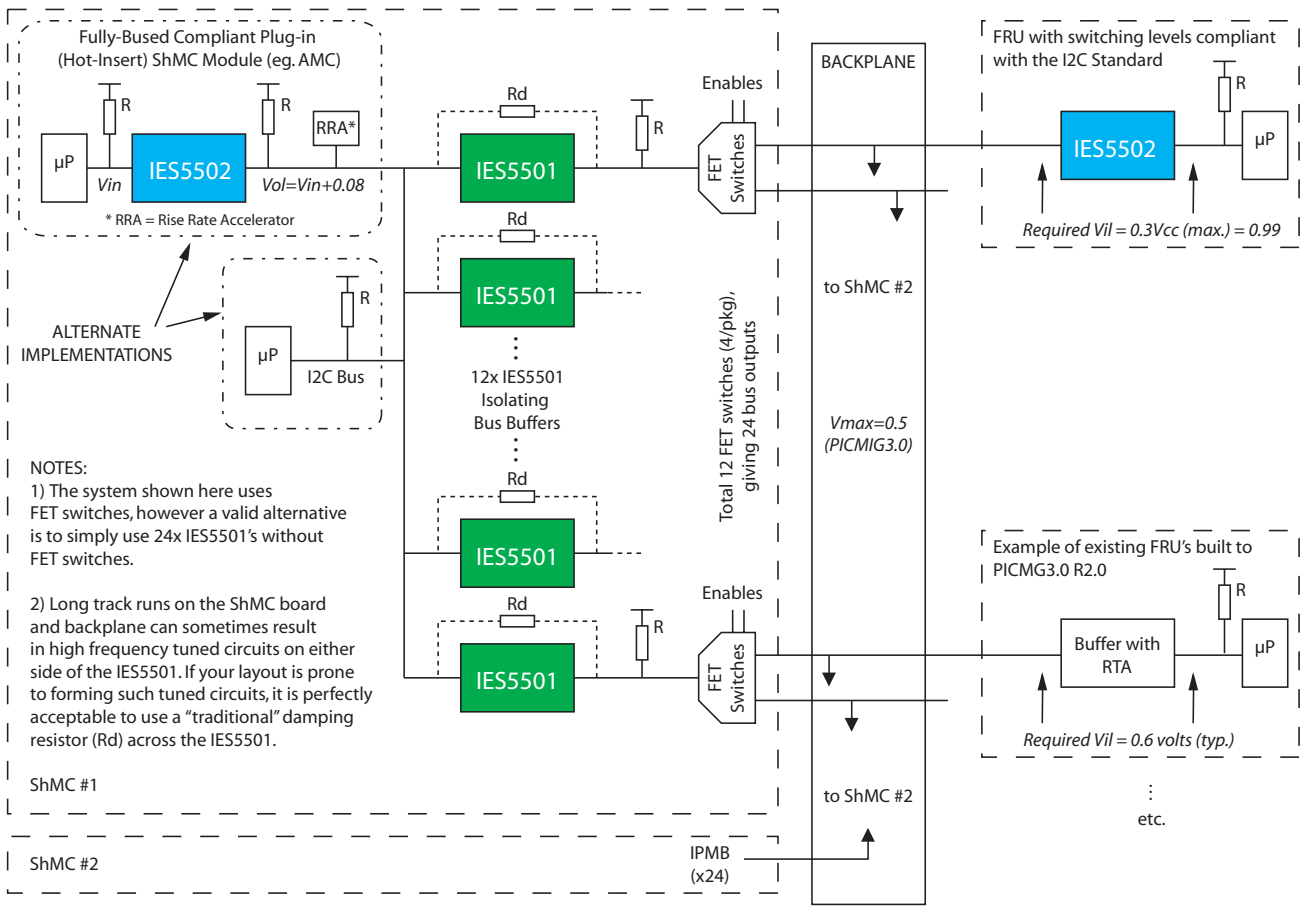

Fig.11 AdvancedTCA style backplane application using IES5501 in a radial Shelf Manager configuration

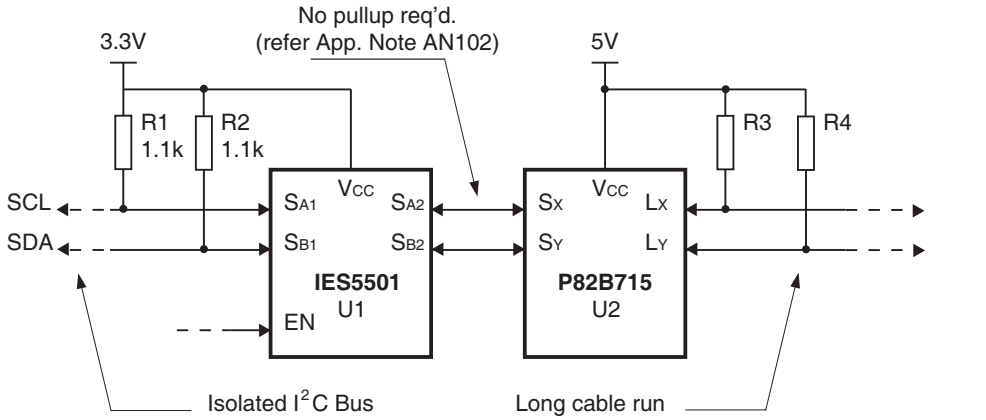

Fig.12 IES5501 isolating the standard I²C bus from a P82B715 used as a line driver

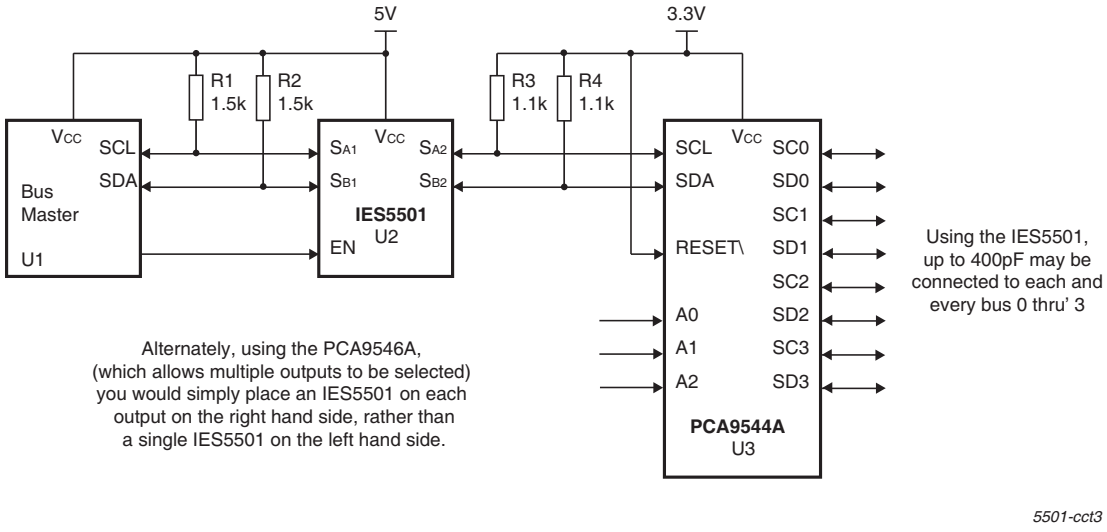

Fig.13 IES5501 multiplexer isolation application

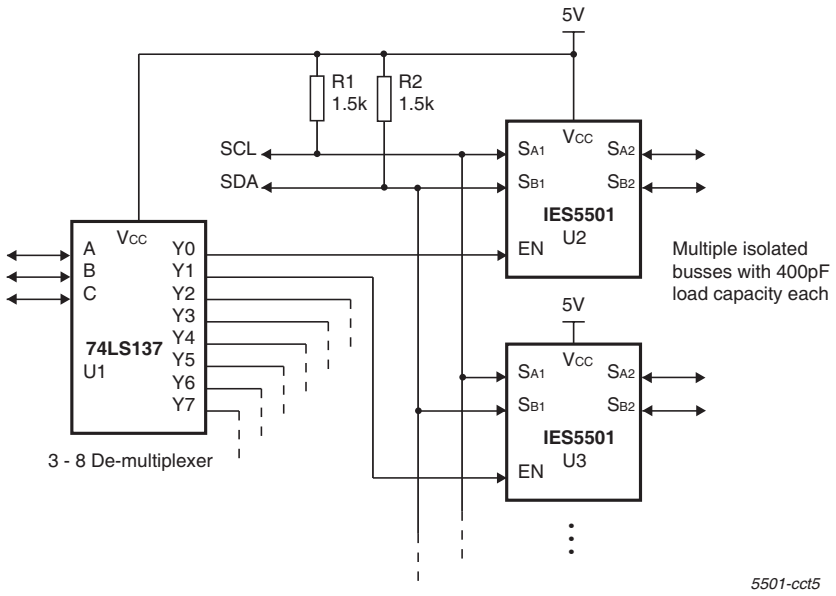

Fig.14 IES5501 bus multiplexer application driven from a simple logic device

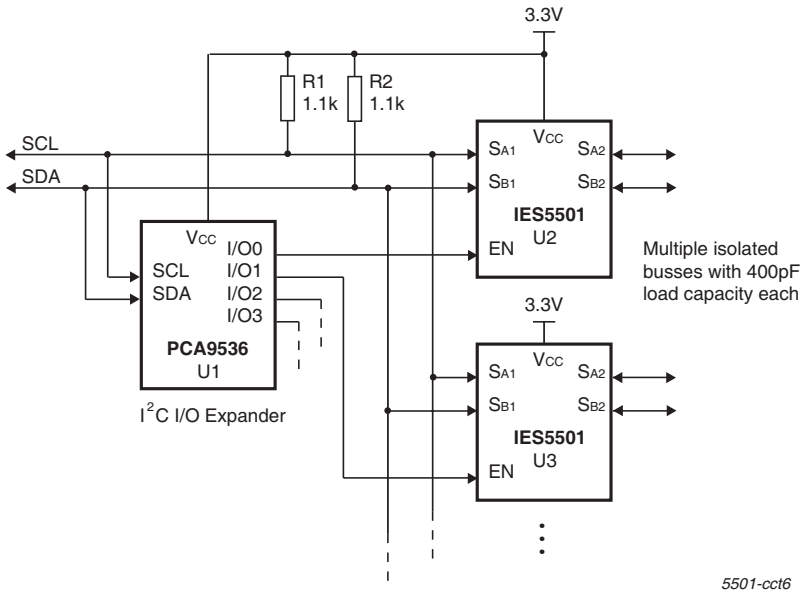

Fig.15 IES5501 bus multiplexer application driven from an I2C I/O Expander

10 ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	NAME	DESCRIPTION	VERSION	ROHS
IES5501T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1	Yes
IES5501D	MSOP-8L	micro small outline package; 8 leads; body width 3.0 mm	SOT505-1	Yes

Other package options are available - contact Hendon Semiconductors for details. For more information on packages, please refer to the document “Integrated Circuit Packaging and Soldering Information” on the Hendon Semiconductors web site.

11 ESD CAUTION

Electrostatic Discharge (ESD) sensitive device. ESD can cause permanent damage or degradation in the performance of this device. This device contains ESD protection structures aimed at minimising the impact of ESD. However, it is the users responsibility to ensure that proper ESD precautions are observed during the handling, placement and operation of this device.

12 DOCUMENT HISTORY

REVISION	DATE	DESCRIPTION
1.0	20070112	Philips to NXP; AN102 in Fig; Capacitor recommendation; Enable timing
1.1	20070528	Update email address
1.2	20071023	Pin Capacitance; Voffset; Company Name Change
1.3	20080513	Update backplane example to AdvancedTCA
1.4	20080613	Remove erroneous negative on EN pin current in Section 8

13 DEFINITIONS

Data sheet status	
Engineering sample information	This contains draft information describing an engineering sample provided to demonstrate possible function and feasibility. Engineering samples have no guarantee that they will perform as described in all details.
Objective specification	This data sheet contains target or goal specifications for product development. Engineering samples have no guarantee that they will function as described in all details.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later. Products to this data may not yet have been fully tested, and their performance fully documented.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

14 COMPANY INFORMATION

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