S1D13748 Mobile Graphics Engine

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The S1D13748 is a low cost, low power Mobile Graphics Engine providing multiple LCD support for embedded and mobile products requiring up to WVGA resolution. Supporting up to three display layers, the S1D13748 provides the Host processor with flexibility in handling multiple image sources. It's ability to receive high speed Host writes, combined with it's support for a wide variety of LCD panels, makes the S1D13748 an excellent choice for a multitude of LCD applications.

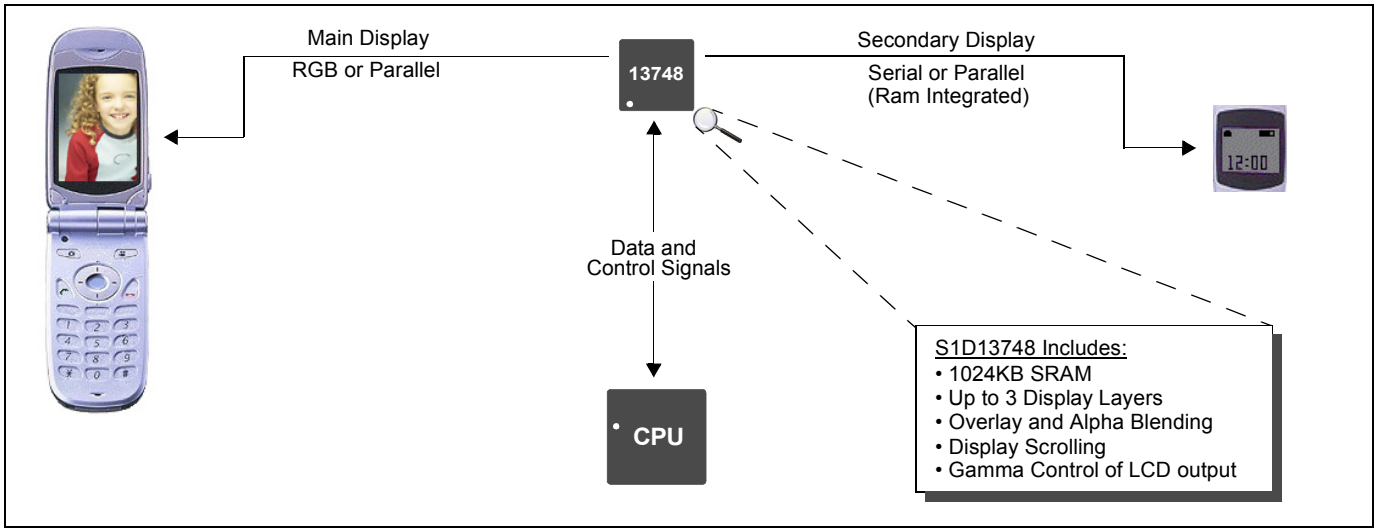
The S1D13748 includes a pixel doubling feature which allows easy migration to larger panel sizes using existing image data. The feature set includes independent resizing of PIP window image data using the bi-cubic scaler, scrolling control for each layer, and LCD output manipulation such as gamma control and optional dithering. This allows the Host processor to provide image data, but off-loads the image processing requirement from the Host. The S1D13748 also incorporates LCD Bypass Mode which allows the Host to exercise direct control over parallel or serial RAM-based panels.

The S1D13748 contains 1024K bytes of embedded SRAM which is used to store image data for up to three layers for LCD1 and image data for LCD2. This feature set provides a low cost, low power single chip solution to meet the demands of embedded markets requiring up to WVGA resolution, such as Mobile Communications devices.

FEATURES

- Embedded 1024K byte SRAM
- Low Operating Voltage
- 16-bit Indirect Host Interface
  - High Speed Host Writes
  - Rectangular, Rotated, and Mirror Host Write Modes
  - Input Formats: YUV 4:2:2, 4:2:0 and RGB 5:6:5
- Supports up to 2 LCD panels (LCD2 must be RAM integrated)
- Support for RGB, Serial, and Parallel I/F panels
- LCD Bypass Mode
- Support for up to 3 display layers with overlay and alpha blending
  - Main Layer image can be doubled in size
  - PIP1 Layer can be resized from 8x to 1/8x
  - PIP2 Layer can be resized from 8x to 1/8x
- Independent scrolling control for each layer
- Look-up Table for gamma control of LCD output
- Optional dithering of LCD output
- Internal PLL or Digital Clock Input
- Software Initiated Power Save Mode
- PFBGA 121-pin or QFP20 144-pin packages

SYSTEM BLOCK DIAGRAM



■ DESCRIPTION

Memory

- 1024K bytes of embedded SRAM

CPU Interface

- 16-bit Indirect Host Interface
  - Supports High Speed Host Writes
  - Integrated Host interface Write Controller supports:
    - Rectangular Write Mode
    - Rotated Write Mode
    - Mirror Write Mode
- LCD Bypass Mode allows direct control of serial and parallel LCD panels by the Host CPU

Panel Support

- 9/12/16/18/24-bit RGB interface panels
- 8/16/18/24-bit Parallel interface panels (RAM Integrated)
- 8/16-bit Serial interface panels (RAM Integrated)
- Supports up to 2 LCD panels (LCDs cannot be refreshed simultaneously)
  - LCD1: RGB, LCD2: Serial w/ RAM
  - LCD1: Parallel w/ RAM, LCD2: Serial w/RAM
  - LCD1: Parallel w/RAM, LCD2: Parallel w/RAM
  - LCD1: RGB, LCD2: Parallel w/RAM

Input Formats

- Host can input image data as:
  - YUV 4:2:2
  - YUV 4:2:0
  - RGB 5:6:5

Display Features

- Supports up to 3 layers with Overlay and Alpha Blending functions:
  - Main Layer features:
    - Image can be stored as RGB 5:6:5
    - Pixel Doubling which doubles the size of the display image (independent horizontal/vertical)
  - PIP1 Layer features:
    - Image can be stored as RGB 5:6:5 or YUV 4:2:2
    - Bi-Cubic Scaler can resize image from 8x - 1/8x
    - Edge Enhancement support
  - PIP2 Layer features:
    - Image can be stored as RGB 5:6:5 or YUV 4:2:2
    - Bi-Cubic Scaler can resize image from 8x - 1/8x
    - Panorama function allows variable vertical scaling
    - Edge Enhancement support
    - LUT (Look-Up Table) for independent gamma control of PIP2 window
- Independent Display Scrolling for each Layer (Main, PIP1, PIP2)
- LUT (Look-Up Table) for gamma control of the LCD output
- Optional dithering for the LCD output

Miscellaneous

- Internal PLL or digital clock input (CLKI)
- Software initiated power save mode
- General Purpose IO pins
- $CORE_{VDD}$ 1.5 volts and IO_{VDD} 1.80, 2.80, or 3.30 volts
- Packages:
  - PFBGA 121-pin (10 x 10 x 1.2mm) (0.8mm pitch)
  - QFP20 144-pin (20 x 20 x 1.4mm) (0.5mm pitch)

CONTACT YOUR SALES REPRESENTATIVE FOR THESE COMPREHENSIVE DESIGN TOOLS

- S1D13748 Technical Documentation
- CPU Independent Software Utilities
- S1D13748 Evaluation Boards
- Royalty Free source level driver code

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