# TS1103

## A 1µA, 200µV$_{OS}$ Bidirectional Precision Current-Sense Amplifier

## FEATURES

- ♦ Ultra-Low Supply Current: 1µA
- ♦ Wide Input Common Mode Range: +2V to +27V
- ♦ Low Input Offset Voltage: 200µV (max)
- ♦ Low Gain Error: 0.6% (max)
- ♦ Voltage Output
- ♦ Four Gain Options Available:
  - TS1103-25: Gain = 25V/V
  - TS1103-50: Gain = 50V/V
  - TS1103-100: Gain = 100V/V
  - TS1103-200: Gain = 200V/V
- ♦ 6-Lead SOT23 Packaging

## APPLICATIONS

Notebook Computers
Power Management Systems
Portable/Battery-Powered Systems
Smart Chargers
Smart Phones

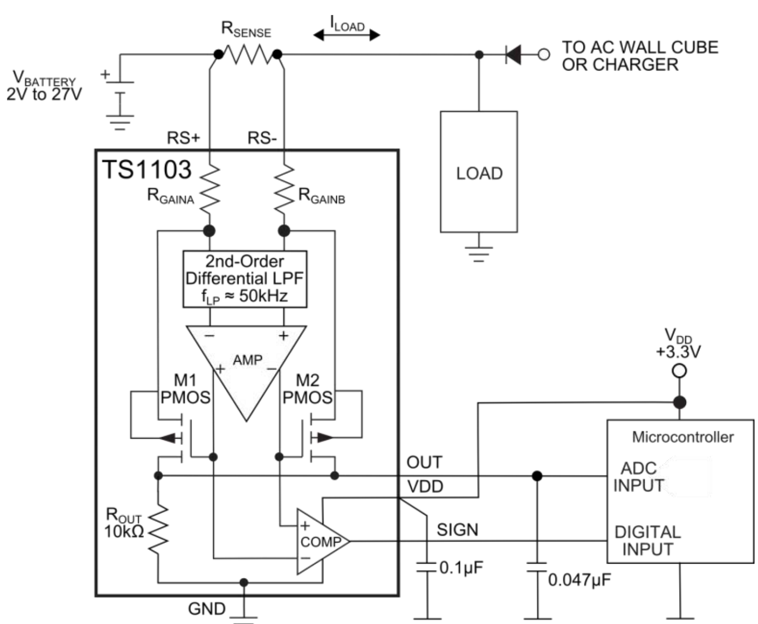
## DESCRIPTION

The TS1103 is the latest addition to the TS1101 family of bidirectional current-sense amplifiers. Consuming a very low 1µA supply current, the TS1103 high-side current-sense amplifiers combine a 200-µV (max) V$_{OS}$ and a 0.6% (max) gain error for cost-sensitive applications. For all high-side bidirectional current-sensing applications, the TS1103s are self-powered and feature a wide input common-mode voltage range from 2V to 27V. A SIGN comparator digital output is also provided that indicates the direction of current flow depending on the external connections to the TS1103's RS+ and RS- input terminals.

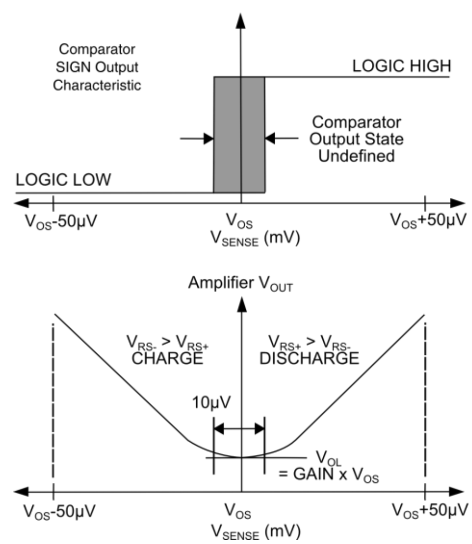
The SOT23 package makes the TS1103 an ideal choice for pcb-area-critical, supply-current-conscious, high-accuracy current-sense applications in all battery-powered and portable instruments.

All TS1103s are specified for operation over the -40°C to +105°C extended temperature range.

## TYPICAL APPLICATION CIRCUIT




**SIGN Comparator's Symmetric I$_{LOAD}$ Crossover**




| PART | GAIN OPTION |
|---|---|
| TS1103-25 | 25 V/V |
| TS1103-50 | 50 V/V |
| TS1103-100 | 100 V/V |
| TS1103-200 | 200 V/V |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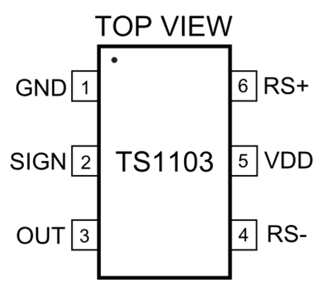
## ABSOLUTE MAXIMUM RATINGS

RS+, RS- to GND ............................................-0.3V to +27V
$V_{DD}$, OUT, SIGN to GND ....................................-0.3V to +6
RS+ to RS- ...................................................................±28V
Short-Circuit Duration: OUT to GND ................... Continuous
Continuous Input Current (Any Pin) ........................... ±20mA
Continuous Power Dissipation ($T_A$ = +70°C)
6-Lead SOT23 (Derate at 4.5mW/°C above +70°C)
.............................................................................. 360mW

Operating Temperature Range .................... -40°C to +105°C
Junction Temperature ............................................... +150°C
Storage Temperature Range ....................... -65°C to +150°C
Lead Temperature (Soldering, 10s) ........................... +300°C
Soldering Temperature (Reflow) ............................ +260°C

Electrical and thermal stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to any absolute maximum rating conditions for extended periods may affect device reliability and lifetime.

## PACKAGE/ORDERING INFORMATION




SOT23-6
G6 Package

| ORDER NUMBER | PART MARKING | CARRIER | QUANTITY |
|---|---|---|---|
| TS1103-25EG6 | TADW | Tape & Reel | ----- |
| TS1103-25EG6T | | Tape & Reel | 3000 |
| TS1103-50EG6 | TADX | Tape & Reel | ----- |
| TS1103-50EG6T | | Tape & Reel | 3000 |
| TS1103-100EG6 | TADY | Tape & Reel | ----- |
| TS1103-100EG6T | | Tape & Reel | 3000 |
| TS1103-200EG6 | TADZ | Tape & Reel | ----- |
| TS1103-200EG6T | | Tape & Reel | 3000 |

**Lead-free Program:** Silicon Labs supplies only lead-free packaging.

Consult Silicon Labs for products specified with wider operating temperature ranges.

# ELECTRICAL CHARACTERISTICS

$V_{RS+}$ = 3.6V; $V_{SENSE}$ = ($V_{RS+}$ - $V_{RS-}$) = 0V; $C_{OUT}$ = 47nF; $V_{DD}$ = 1.8V; $T_A$ = -40°C to +105°C, unless otherwise noted. Typical values are at $T_A$ = +25°C. See Note 1.

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Supply Current (Note 2) | $I_{CC}$ | $T_A$ = +25°C | | 0.68 | 0.85 | μA |
| | | | | | 1.0 | |
| | | $V_{RS+}$ = 25V, $T_A$ = +25°C | | | 1.0 | |
| | | $V_{RS+}$ = 25V | | | 1.2 | |
| Common-Mode Input Range | $V_{CM}$ | Guaranteed by CMRR | 2 | | 27 | V |
| **CURRENT SENSE AMPLIFIER PARAMETERS** | | | | | | |
| Common-Mode Rejection Ratio | CMRR | 2V < $V_{RS+}$ < 27V | 120 | 150 | | dB |
| Input Offset Voltage (Note 3) | $V_{OS}$ | $T_A$ = +25°C | | ±30 | ±200 | μV |
| | | | | | ±300 | |
| $V_{OS}$ Hysteresis (Note 4) | $V_{HYS}$ | $T_A$ = +25°C | | 10 | | μV |
| Gain | G | TS1103-25 | | 25 | | V/V |
| | | TS1103-50 | | 50 | | |
| | | TS1103-100 | | 100 | | |
| | | TS1103-200 | | 200 | | |
| Gain Error (Note 5) | GE | $T_A$ = +25°C | | ±0.2 | ±0.6 | % |
| | | | | | ±1.0 | |
| Gain Match (Note 5) | GM | $T_A$ = +25°C | | ±0.2 | ±0.6 | % |
| | | | | | ±1 | |
| Output Resistance (Note 6) | $R_{OUT}$ | TS1103-25/50/100 | 7.0 | 10 | 13.2 | kΩ |
| | | TS1103-200 | 14.0 | 20 | 26.4 | |
| OUT Low Voltage | $V_{AOL}$ | Gain = 25 | | | 5 | mV |
| | | Gain = 50 | | | 10 | |
| | | Gain = 100 | | | 20 | |
| | | Gain = 200 | | | 40 | |
| OUT High Voltage (Note 7) | $V_{AOH}$ | $V_{OH}$ = $V_{RS-}$ - $V_{OUT}$ | | 0.05 | 0.2 | V |
| Output Settling Time | $t_S$ | TS1103-25/50/100, 1% final value, $V_{OUT}$ = 3V | | 2.2 | | ms |
| | | TS1103-200, 1% final value, $V_{OUT}$ = 3V | | 4.3 | | |
| **SIGN COMPARATOR PARAMETERS** | | | | | | |
| VDD Supply Voltage Range | $V_{DD}$ | | 1.25 | | 5.5 | V |
| VDD Supply Current | $I_{DD}$ | | | 0.02 | 0.2 | μA |
| Output Low Voltage | $V_{COL}$ | $V_{DD}$ = 1.25V, $I_{SINK}$ = 5μA | | | 0.2 | V |
| | | $V_{DD}$ = 1.8V, $I_{SINK}$ = 35μA | | | | |
| Output High Voltage | $V_{COH}$ | $V_{DD}$ = 1.25V, $I_{SOURCE}$ = 5μA | $V_{DD}$ – 0.2 | | | V |
| | | $V_{DD}$ = 1.8V, $I_{SOURCE}$ = 35μA | | | | |
| Propagation Delay | $t_{PD}$ | $V_{SENSE}$ = ±1mV | | 3 | | ms |
| | | $V_{SENSE}$ = ±10mV | | 0.4 | | |

**Note 1:** All devices are 100% production tested at $T_A$ = +25°C. All temperature limits are guaranteed by product characterization.
**Note 2:** Extrapolated to $V_{OUT}$ = 0. $I_{CC}$ is the total current into the RS+ and the RS- pins.
**Note 3:** Input offset voltage $V_{OS}$ is extrapolated from a $V_{OUT+}$ measurement with $V_{SENSE}$ set to +1mV and a $V_{OUT-}$ measurement with $V_{SENSE}$ set to -1mV; vis-a-viz,

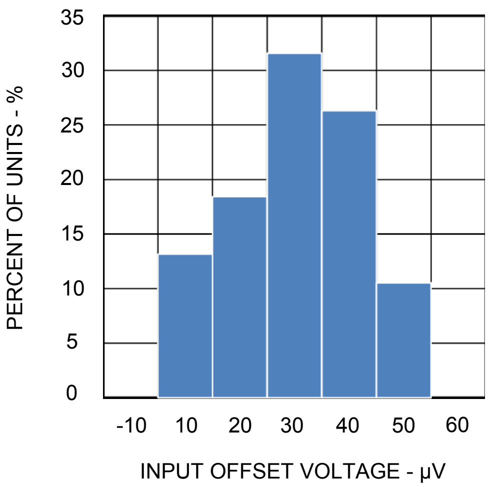
$$\text{Average } V_{OS} = \frac{(V_{OUT-}) - (V_{OUT+})}{2 \times \text{GAIN}}$$

**Note 4:** Amplitude of $V_{SENSE}$ lower or higher than $V_{OS}$ required to cause the comparator to switch output states.
**Note 5:** Gain error applies to current flow in either direction and is calculated by applying two values for $V_{SENSE}$ and then calculating the error of the actual slope vs. the ideal transfer characteristic:
For GAIN = 25, the applied $V_{SENSE}$ is 20mV and 120mV.
For GAIN = 50, the applied $V_{SENSE}$ is 10mV and 60mV.
For GAIN = 100, the applied $V_{SENSE}$ is 5mV and 30mV.
For GAIN = 200, the applied $V_{SENSE}$ is 2.5mV and 15mV.
**Note 6:** The device is stable for any capacitive load at $V_{OUT}$.
**Note 7:** $V_{OH}$ is the voltage from $V_{RS-}$ to $V_{OUT}$ with $V_{SENSE}$ = 3.6V/GAIN.

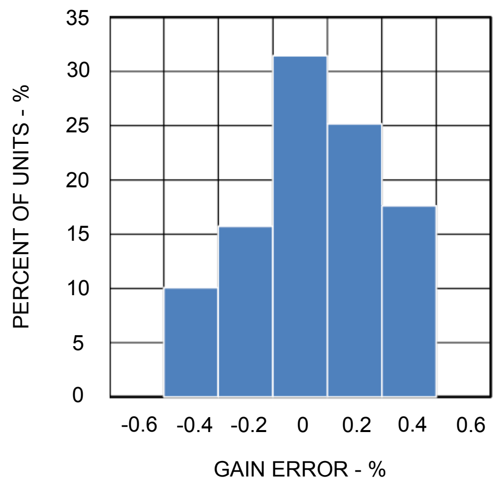
## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{RS+} = V_{RS-} = 3.6V$; $T_A = +25°C$, unless otherwise noted.

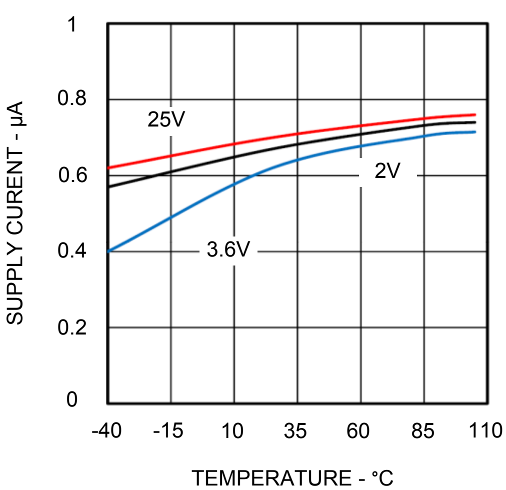
**Input Offset Voltage Histogram**



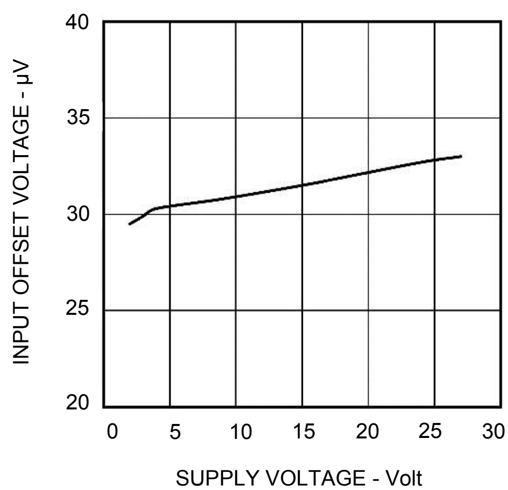

**Gain Error Histogram**



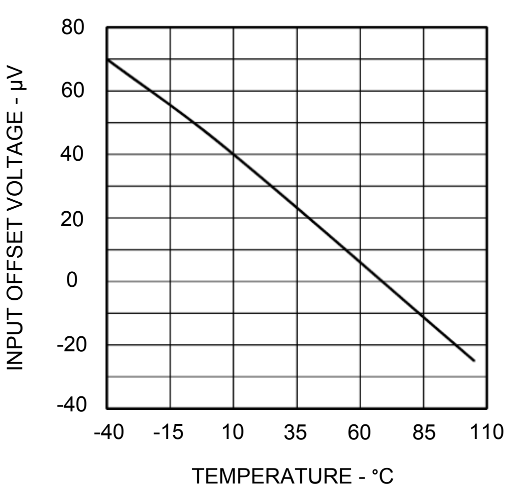

**Supply Current vs Temperature**



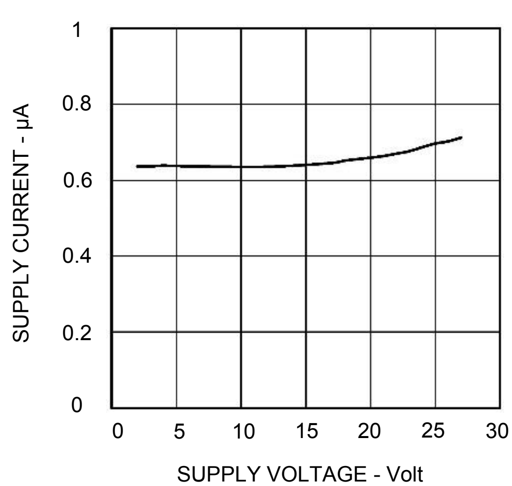

**Input Offset Voltage vs Common-Mode Voltage**




**Input Offset Voltage vs Temperature**



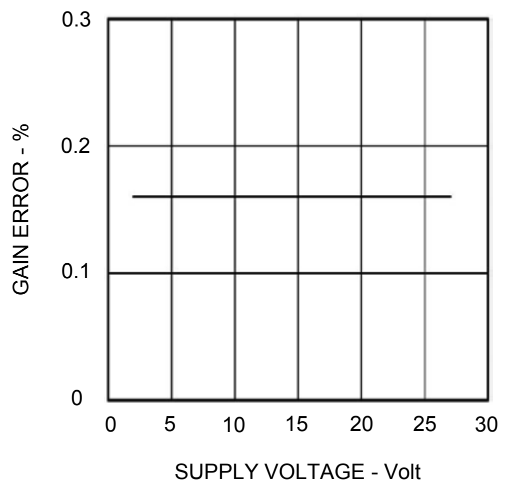

**Supply Current vs Common-Mode Voltage**



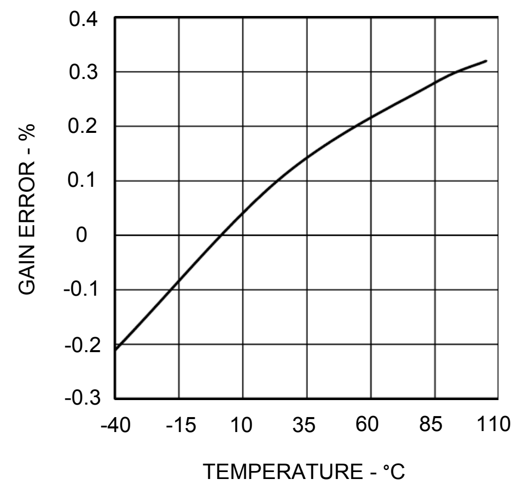
# TYPICAL PERFORMANCE CHARACTERISTICS

$V_{RS+} = V_{RS-} = 3.6V$; $T_A = +25°C$, unless otherwise noted.

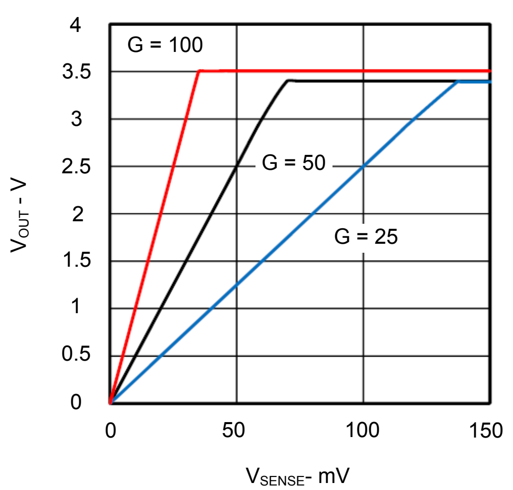
**Gain Error vs Common-Mode Voltage**



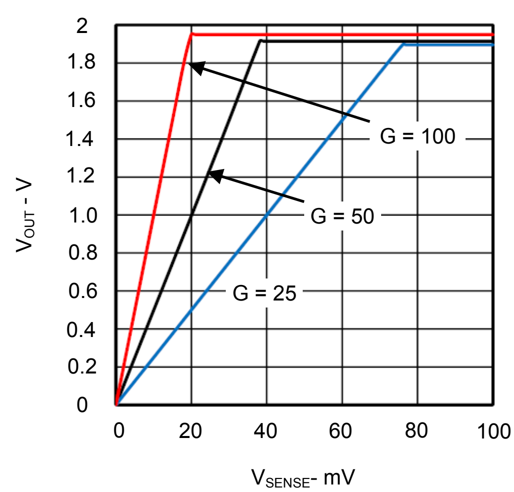

**Gain Error vs. Temperature**



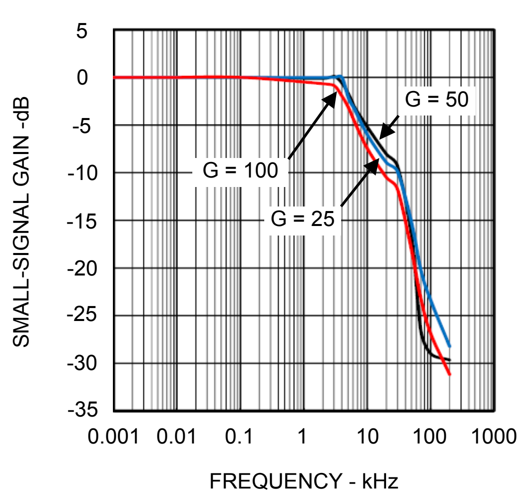

**$V_{OUT}$ vs $V_{SENSE}$ @ Supply = 3.6V**



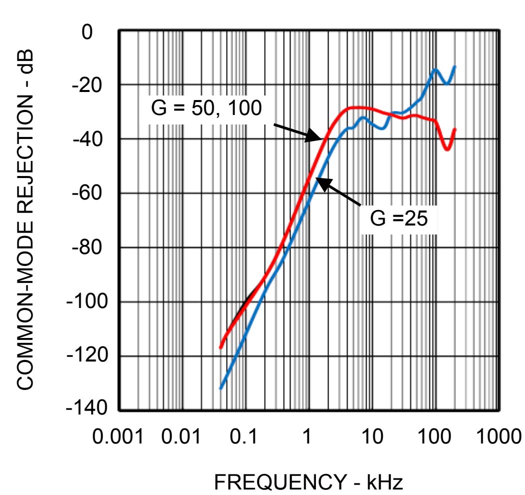

**$V_{OUT}$ vs $V_{SENSE}$ @ Supply = 2V**




**Small-Signal Gain vs Frequency**



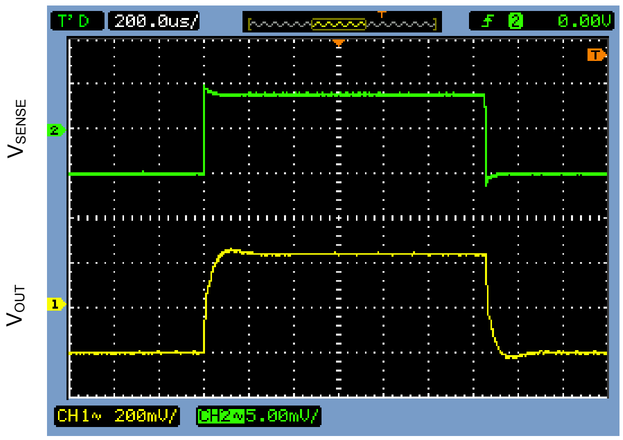

**Common-Mode Rejection vs Frequency**



## TYPICAL PERFORMANCE CHARACTERISTICS

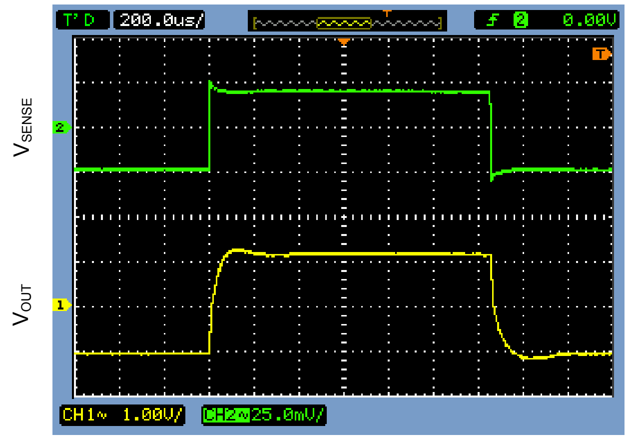
$V_{RS+} = V_{RS-} = 3.6V$; $C_{OUT} = 0pF$; $T_A = +25°C$, unless otherwise noted.

**Small-Signal Pulse Response, Gain = 50**



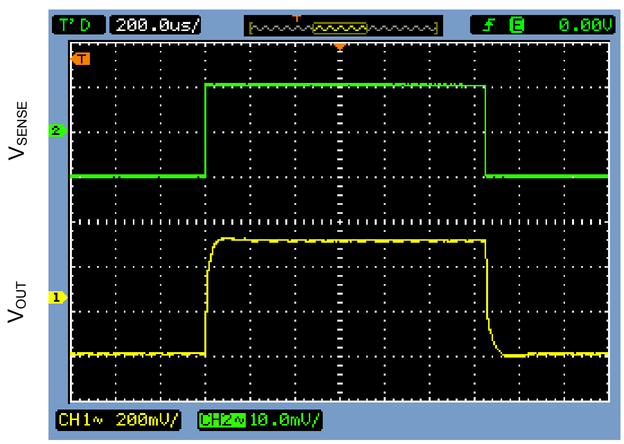

200µs/DIV

**Large-Signal Pulse Response, Gain = 50**



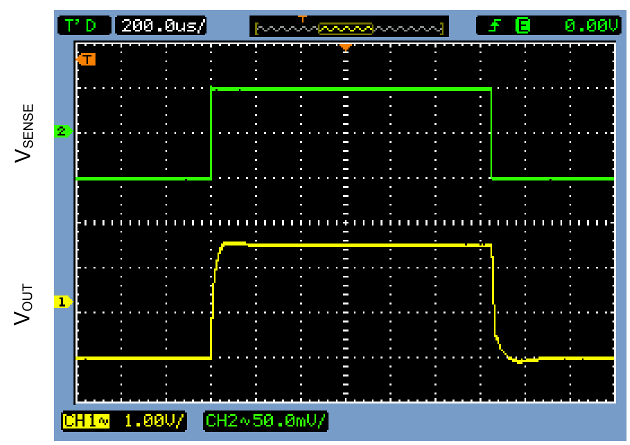

200µs/DIV

**Small-Signal Pulse Response, Gain = 25**



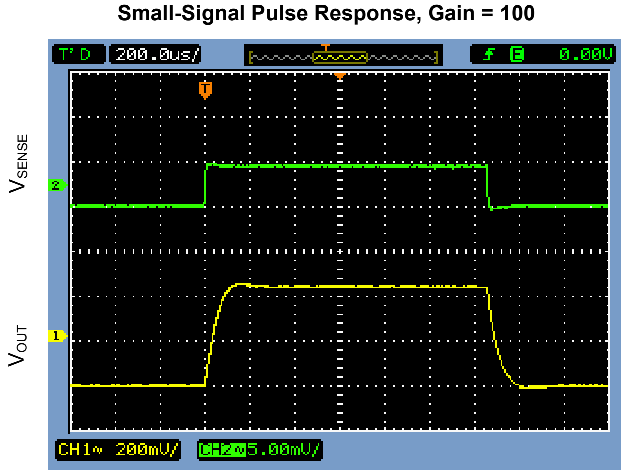

200µs/DIV

**Large-Signal Pulse Response, Gain = 25**



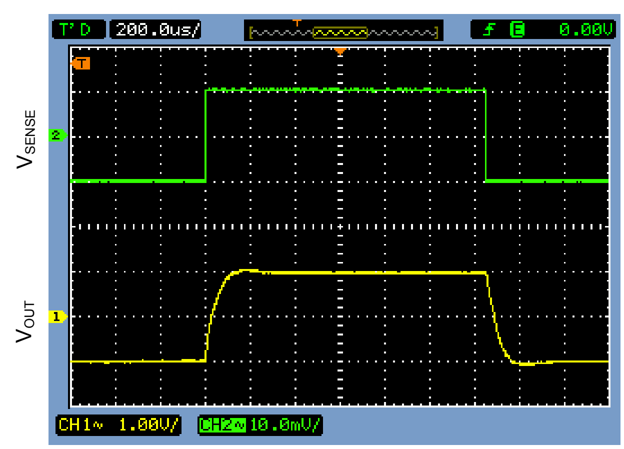

200µs/DIV

**Small-Signal Pulse Response, Gain = 100**




200µs/DIV

**Large-Signal Pulse Response, Gain = 100**

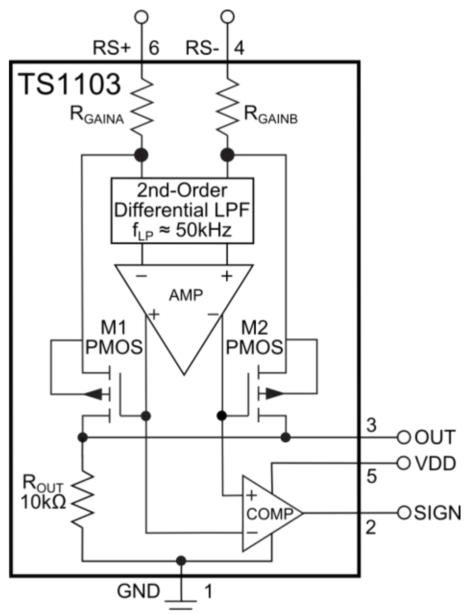



200µs/DIV

## PIN FUNCTIONS

| PIN | LABEL | FUNCTION |
|---|---|---|
| 1 | GND | Ground. Connect this pin to analog ground. |
| 2 | SIGN | Comparator Output, push-pull; SIGN is HIGH for ($V_{RS+} > V_{RS-}$) and LOW for ($V_{RS-} > V_{RS+}$). |
| 3 | OUT | Output Voltage. $V_{OUT}$ is proportional to $V_{SENSE} = (V_{RS+} - V_{RS-})$ or $(V_{RS-} - V_{RS+})$. |
| 4 | RS- | External Sense Resistor Load-Side Connection |
| 5 | VDD | SIGN Comparator External Power Supply Pin; Connect this pin to system's logic VDD supply. |
| 6 | RS+ | External Sense Resistor Power-Side Connection |

## BLOCK DIAGRAM




## DESCRIPTION OF OPERATION

The internal configuration of the TS1103 – a bidirectional high-side, current-sense amplifier – is a variation of the TS1100 uni-directional current-sense amplifier. In the design of the TS1103, the input amplifier was reconfigured for fully differential input/output operation and a second low-threshold p-channel FET (M2) was added where the drain terminal of M2 is also connected to ROUT. Therefore, the behavior of the TS1103 for when $V_{RS-} > V_{RS+}$ is identical for when $V_{RS+} > V_{RS-}$.

Referring to the typical application circuit on Page 1, the inputs of the TS1103's differential input/output amplifier are connected across an external RSENSE resistor that is used to measure current. At the non-inverting input of the TS1103 (the RS- terminal), the applied voltage is $I_{LOAD}$ x RSENSE. Since the RS- terminal is the non-inverting input of the internal op amp, op amp feedback action forces the inverting input of the internal op amp to the same potential ($I_{LOAD}$ x RSENSE). Therefore, the voltage drop across RSENSE ($V_{SENSE} = V_{RS+} - V_{RS-}$) and the voltage drop across RGAINA (at the RS+ terminal) are equal. Necessary for gain ratio match, both RGAINA and RGAINB are the same value.

Since p-channel M1's source is connected to the inverting input of the internal op amp and since the voltage drop across RGAINA is the same as the external $V_{SENSE}$, op amp feedback action drives the gate of M1 such that M1's drain-source current is equal to:

$$I_{DS(M1)} = \frac{V_{SENSE}}{RGAINA}$$

or

$$I_{DS(M1)} = \frac{I_{LOAD} \times R_{SENSE}}{RGAINA}$$

Since M1's drain terminal is connected to ROUT, the output voltage of the TS1103 at the OUT terminal is, therefore;

$$V_{OUT} = I_{LOAD} \times R_{SENSE} \times \frac{R_{OUT}}{RGAINA}$$

When the voltage at the RS- terminal is greater than the voltage at the RS+ terminal, the external VSENSE voltage drop is impressed upon RGAINB. The voltage drop across RGAINB is then converted into a current by M2 that then produces an output voltage across ROUT. In this design, when M1 is conducting current ($V_{RS+} > V_{RS-}$), the TS1103's internal amplifier holds M2 OFF. When M2 is conducting current ($V_{RS-} > V_{RS+}$), the internal amplifier holds M1 OFF. In either case, the disabled FET does not contribute to the resultant output voltage.

The current-sense amplifier's gain accuracy is therefore the ratio match of ROUT to RGAIN[A/B]. For each of the four gain options available, Table 1 lists the values for ROUT and RGAIN[A/B]. The TS1103's output stage is protected against input overdrive by use of an output current-limiting circuit of 3mA (typical) and a 7V internal clamp protection circuit.

**Table 1: Internal Gain Setting Resistors (Typical Values)**

| GAIN (V/V) | RGAIN[A/B] (Ω) | ROUT (Ω) | Part Number |
|---|---|---|---|
| 25 | 400 | 10k | TS1103-25 |
| 50 | 200 | 10k | TS1103-50 |
| 100 | 100 | 10k | TS1103-100 |
| 200 | 100 | 20k | TS1103-200 |

### The SIGN Comparator Output

As shown in the TS1103's block diagram, the design of the TS1103 incorporated one additional feature – an analog comparator the inputs of which monitor the internal amplifier's differential output voltage. While the voltage at the TS1103's OUT terminal indicates the magnitude of the load current, the TS1103's SIGN output indicates the load current's direction. The SIGN output is a logic high when M1 is conducting current ($V_{RS+} > V_{RS-}$). Alternatively, the SIGN output is a logic low when M2 is conducting current ($V_{RS+} < V_{RS-}$). The SIGN comparator's transfer characteristic is illustrated in Figure 1. Unlike other current-sense amplifiers that implement a OUT/SIGN arrangement, the TS1103 exhibits no "dead zone" at $I_{LOAD}$ switchover.

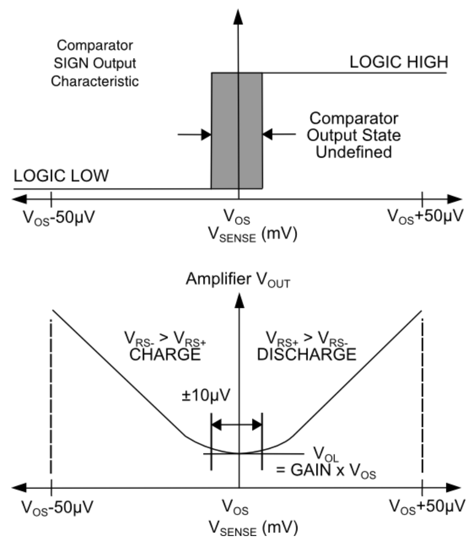



**Figure 1:** TS1103's SIGN Comparator Transfer Characteristic.

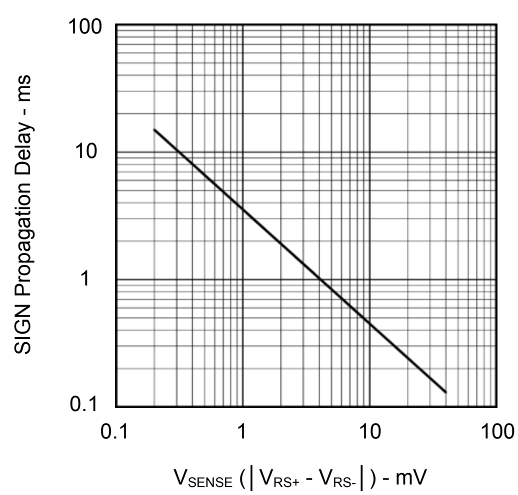



**Figure 2:** SIGN Comparator Propagation Delay vs $V_{SENSE}$.

The other attribute of the SIGN comparator's behavior is its propagation delay as a function of applied $V_{SENSE}$ [($V_{RS+}$ - $V_{RS-}$) or ($V_{RS-}$ - $V_{RS+}$)]. As shown in Figure 2, the SIGN comparator's propagation delay behavior is symmetric regardless of current-flow direction and is inversely proportional to $V_{SENSE}$.

# APPLICATIONS INFORMATION

**Choosing the Sense Resistor**

Selecting the optimal value for the external RSENSE is based on the following criteria and for each commentary follows:

1) RSENSE Voltage Loss
2) $V_{OUT}$ Swing vs. Applied Input Voltage at $V_{RS+}$ and Desired $V_{SENSE}$
3) Total $I_{LOAD}$ Accuracy
4) Circuit Efficiency and Power Dissipation
5) RSENSE Kelvin Connections

**1) RSENSE Voltage Loss**

For lowest IR power dissipation in RSENSE, the smallest usable resistor value for RSENSE should be selected.

**2) $V_{OUT}$ Swing vs. Applied Input Voltage at $V_{RS+}$ and Desired $V_{SENSE}$**

As there is no separate power supply pin for the TS1103, the circuit draws its power from the voltage at its RS+ and RS- terminals. Therefore, the signal voltage at the OUT terminal is bounded by the minimum voltage applied at the RS+ terminal.

Therefore,

$$V_{OUT(max)} = V_{RS+(min)} - V_{SENSE(max)} - V_{OH(max)}$$

and

$$R_{SENSE} < \frac{V_{OUT}\,(\max)}{GAIN \times I_{LOAD}(\max)}$$

where the full-scale $V_{SENSE}$ should be less than $V_{OUT(MAX)}$/GAIN at the application's minimum RS+ terminal voltage. For best performance with a 3.6V power supply, RSENSE should be chosen to generate a $V_{SENSE}$ of: a) 120mV (for the 25V/V GAIN option), b) 60mV (for the 50V/V GAIN option), c) 30mV (for the 100V/V GAIN option), or d) 15mV (for the 200V/V GAIN option) at the full-scale $I_{LOAD}$ current in each application. For the case where the minimum power supply voltage is higher than 3.6V, each of the four full-scale $V_{SENSE}$s above can be increased.

**3) Total Load Current Accuracy**

In the TS1103's linear region where $V_{OUT} < V_{OUT(max)}$, there are two specifications related to the circuit's accuracy: a) the TS1103's input offset voltage ($V_{OS(max)}$ = 200µV) and b) its gain error (GE(max) = 0.6%). An expression for the TS1103's total error is given by:

$$V_{OUT} = [GAIN \times (1 \pm GE) \times V_{SENSE}] \pm (GAIN \times V_{OS})$$

A large value for RSENSE permits the use of smaller load currents to be measured more accurately because the effects of offset voltages are less significant when compared to larger VSENSE voltages. Due care though should be exercised as previously mentioned with large values of RSENSE.

**4) Circuit Efficiency and Power Dissipation**

IR losses in RSENSE can be large especially at high load currents. It is important to select the smallest, usable RSENSE value to minimize power dissipation and to keep the physical size of RSENSE small. If the external RSENSE is allowed to dissipate significant power, then its inherent temperature coefficient may alter its design center value, thereby reducing load current measurement accuracy. Precisely because the TS1103's input stage was designed to exhibit a very low input offset voltage, small RSENSE values can be used to reduce power dissipation and minimize local hot spots on the pcb.

**5) RSENSE Kelvin Connections**

For optimal $V_{SENSE}$ accuracy in the presence of large load currents, parasitic pcb track resistance should be minimized. Kelvin-sense pcb connections between RSENSE and the TS1103's RS+ and RS- terminals are strongly recommended. The drawing in Figure 3 illustrates the connections between the current-sense amplifier and the current-sense resistor. The pcb layout should be balanced and symmetrical to minimize wiring-induced errors. In addition, the pcb layout for RSENSE should include good thermal management techniques for optimal RSENSE power dissipation.

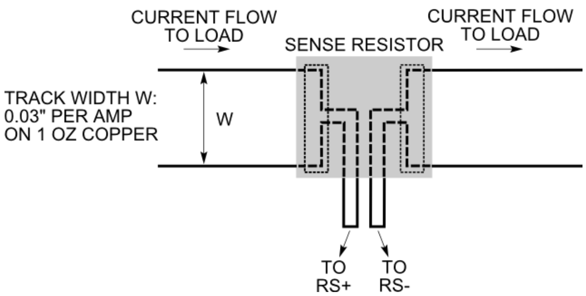



**Figure 3**: Making PCB Connections to RSENSE.

### 6) RSENSE Composition

Current-shunt resistors are available in metal film, metal strip, and wire-wound constructions. Wire-wound current-shunt resistors are constructed with wire spirally wound onto a core. As a result, these types of current shunt resistors exhibit the largest self inductance. In applications where the load current contains high-frequency transients, metal film or metal strip current sense resistors are recommended.

### Internal Noise Filter

In power management and motor control applications, current-sense amplifiers are required to measure load currents accurately in the presence of both externally-generated differential and common-mode noise. An example of differential-mode noise that can appear at the inputs of a current-sense amplifier is high-frequency ripple. High-frequency ripple – whether injected into the circuit inductively or capacitively - can produce a differential-mode voltage drop across the external current-shunt resistor (RSENSE). An example of externally-generated, common-mode noise is the high-frequency output ripple of a switching regulator that can result in common-mode noise injection into both inputs of a current-sense amplifier.

Even though the load current signal bandwidth is DC, the input stage of any current-sense amplifier can rectify unwanted, out-of-band noise that can result in an apparent error voltage at its output. This rectification of noise signals occurs because all amplifier input stages are constructed with transistors that can behave as high-frequency signal detectors in the same way pn-junction diodes were used as RF envelope detectors in early radio designs. Against common-mode injected noise, the amplifier's internal common-mode rejection is usually sufficient.

To counter the effects of externally-injected noise, it has always been good engineering practice to add external low-pass filters in series with the inputs of a current-sense amplifier. In the design of discrete current-sense amplifiers, resistors used in the external low-pass filters were incorporated into the circuit's overall design so errors because of any input-bias current-generated offset voltage errors and gain errors were compensated.

With the advent of monolithic current-sense amplifiers, like the TS1103, the addition of external low-pass filters in series with the current-sense amplifier's inputs only introduces additional offset voltage and gain errors. To minimize or eliminate altogether the need for external low-pass filters and to maintain low input offset voltage and gain errors, the TS1103 incorporates a 50-kHz (typ), 2$^{nd}$-order differential low-pass filter as shown in the TS1103's Block Diagram.

### Output Filter Capacitor

If the TS1103 is part of a signal acquisition system where its OUT terminal is connected to the input of an ADC with an internal, switched-capacitor track-and-hold circuit, the internal track-and-hold's sampling capacitor can cause voltage droop at $V_{OUT}$. A 22nF to 100nF good-quality ceramic capacitor from the OUT terminal to GND forms a low-pass filter with the TS1103's $R_{OUT}$ and should be used to minimize voltage droop (holding $V_{OUT}$ constant during the sample interval. Using a capacitor on the OUT terminal will also reduce the TS1103's small-signal bandwidth as well as band-limiting amplifier noise.

### PC Board Layout and Power-Supply Bypassing

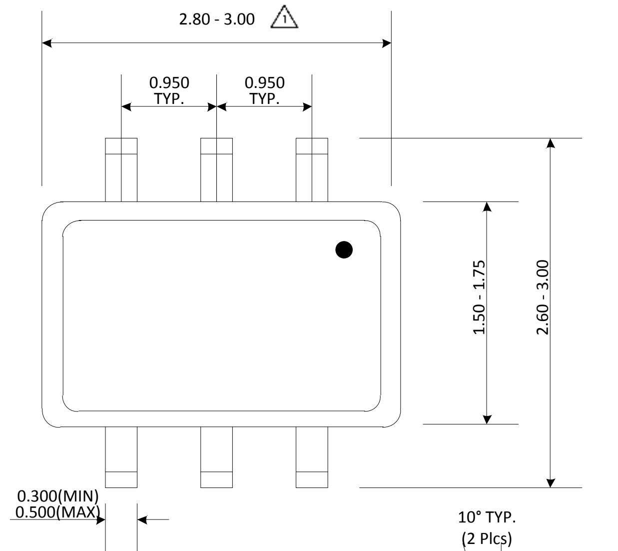
For optimal circuit performance, the TS1103 should be in very close proximity to the external current-sense resistor and the pcb tracks from RSENSE to the RS+ and the RS- input terminals of the TS1103 should be short and symmetric. Also recommended are a ground plane and surface mount resistors and capacitors.

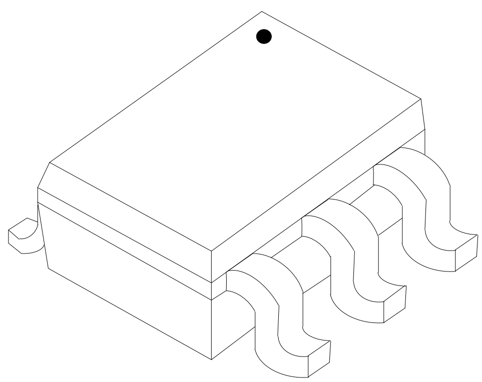
# PACKAGE OUTLINE DRAWING

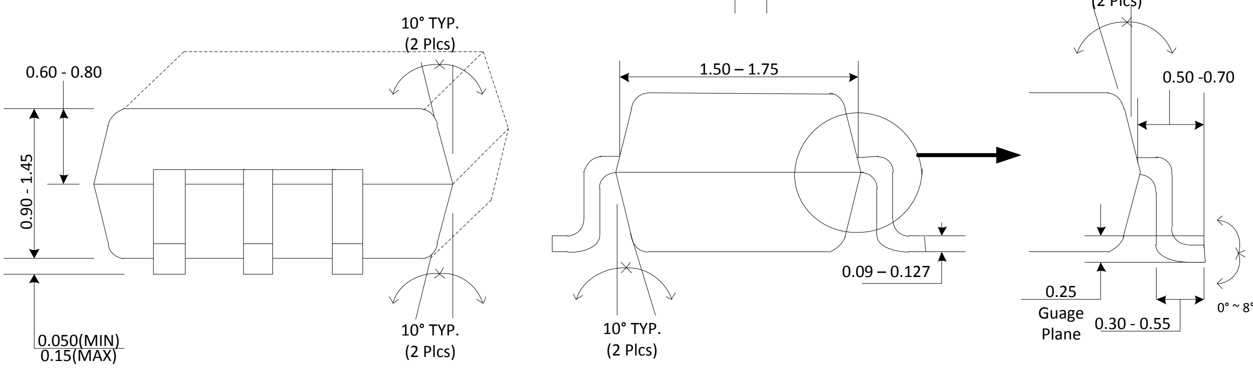
## 6-Pin SOT23 Package Outline Drawing

(N.B., Drawings are not to scale)

Note:
△1 Dimension are exclusive of mold flash and gate burr.
**2.** Dimension are exclusive of solder plating.
**3.** The foot length measuring is based on the gauge plane method.
**4.** Package is surface to be matte finish VDI 11~13.
**5.** Dimensions and tolerances are as per ANSI Y14.5M, 1982.
**6.** This part is compliant with EIAJ specification SC74A and JEDEC MO-178 AB spec.
**7.** Die is facing up for mold, Die is facing down for trim/form, ie. reverse trim/form.
**8.** All dimensions are in mm.



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