FAIRCHILD SEMICONDUCTOR®

June 2011

SG6741
Highly Integrated Green-Mode PWM Controller

Features

- High-Voltage Startup
- Low Operating Current: 4mA
- Linearly Decreasing PWM Frequency to 22kHz
- Frequency Hopping to Reduce EMI Emission
- Peak-Current-Mode Control
- Cycle-by-Cycle Current Limiting
- Leading-Edge Blanking
- Synchronized Slope Compensation
- Gate Output Maximum Voltage Clamp: 18V
- V_{DD} Over-Voltage Protection (Auto Restart)
- V_{DD} Under-Voltage Lockout (UVLO)
- Internal Open-Loop Protection
- Constant Power Limit (Full AC Input Range)

Applications

General-purpose switch-mode power supplies and flyback power converters, including:

- Power Adapters
- Open-Frame SMPS

Description

The highly integrated SG6741 PWM controller provides several features to enhance the performance of flyback converters.

The highly integrated SG6741 series of PWM controllers provides several features to enhance the performance of flyback converters.

To minimize standby power consumption, a proprietary green-mode function provides off-time modulation to linearly decrease the switching frequency at light-load conditions. To avoid acoustic-noise problems, the minimum PWM frequency is set above 22KHz. This green-mode function enables the power supply to meet international power conservation requirements. With the internal high-voltage startup circuitry, the power loss due to bleeding resistors is also eliminated. To further reduce power consumption, SG6741 is manufactured using the BiCMOS process, which allows an operating current of only 4mA.

SG6741 integrates a frequency-hopping function that helps reduce EMI emission of a power supply with minimum line filters. Its built-in synchronized slope compensation achieves stable peak-current-mode control. The proprietary internal line compensation ensures constant output power limit over a wide range of AC input voltages, from $90V_{AC}$ to $264V_{AC}$.

SG6741 provides many protection functions. In addition to cycle-by-cycle current limiting, the internal open-loop protection circuit ensures safety when an open-loop or output short-circuit failure occurs. PWM output is disabled until V_{DD} drops below the UVLO lower limit; then the controller starts again. As long as V_{DD} exceeds about 26V, the internal OVP circuit is triggered.

SG6741 is available in an 8-pin SOP package.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
SG6741SZ	-40 to +105°C	8-Lead Small Outline Package (SOP)	Tape & Reel
SG6741SY	-40 to +105°C	8-Lead Small Outline Package (SOP)	Tape & Reel

Application Diagram

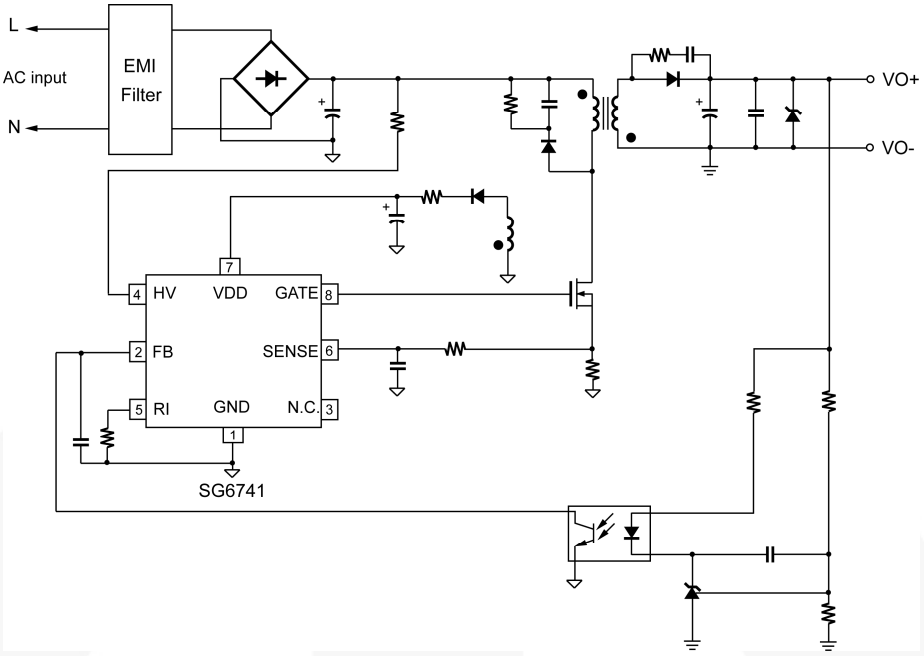

Figure 1. Typical Application

Internal Block Diagram

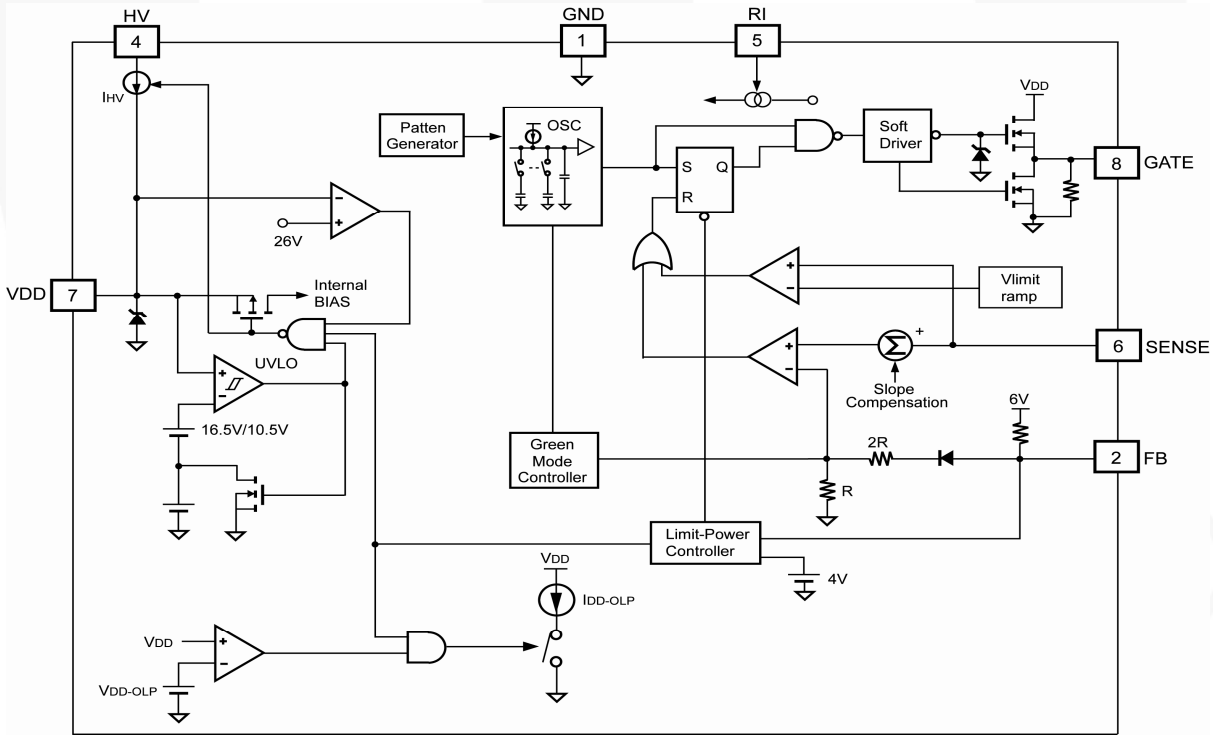

Figure 2. Functional Block Diagram

Marking Information

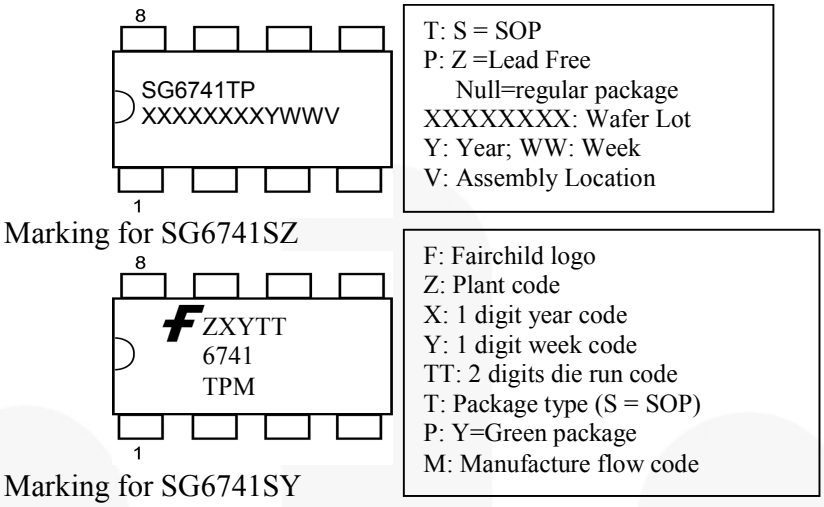

Figure 3. Top Mark

Pin Configuration

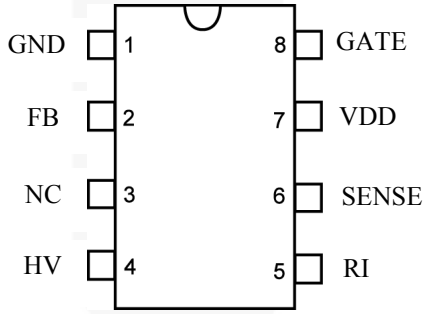

Figure 4. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	GND	Ground.
2	FB	The signal from the external compensation circuit is fed into this pin. The PWM duty cycle is determined in response to the signal on this pin and the current-sense signal on the SENSE pin.
3	NC	No connection.
4	HV	For startup, this pin is pulled high to the line input or bulk capacitor via resistors.
5	RI	A resistor connected from the RI pin to GND pin provides the SG6741 with a constant current source. This determines the center PWM frequency. Increasing the resistance reduces PWM frequency. Using a 26KΩ resistor (R_I) results in a 65kHz center PWM frequency.
6	SENSE	Current sense. The sensed voltage is used for peak-current-mode control and cycle-by-cycle current limiting.
7	VDD	Power supply. The internal protection circuit disables PWM output as long as V_{DD} exceeds the OVP trigger point.
8	GATE	The totem-pole output driver. Soft driving waveform is implemented for improved EMI.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. All voltage values, except differential voltages, are given with respect to the ground pin.

Symbol	Parameter		Min.	Max.	Unit
V_{VDD}	DC Supply Voltage[1, 2]			30	V
V_{FB}	FB Pin Input Voltage		-0.3	7.0	V
V_{SENSE}	SENSE Pin Input Voltage		-0.3	7.0	V
V_{RI}	RI Pin Input Voltage		-0.3	7.0	V
V_{HV}	HV Pin Input Voltage			500	V
P_D	Power Dissipation ($T_A < 50°C$)			400	mW
Θ_{JA}	Thermal Resistance (Junction-to-Air)			141	°C/W
T_J	Operating Junction Temperature		-40	+125	°C
T_{STG}	Storage Temperature Range		-55	+150	°C
T_L	Lead Temperature (Wave Soldering or IR, 10 Seconds)			+260	°C
ESD	Electrostatic Discharge Capability, Human Body Model, JESD22-A114	All Pins Except HV Pin		4	kV
	Electrostatic Discharge Capability, Machine Model, JESD22-A115	All Pins Except HV Pin		200	V

Notes:
1. All voltage values, except differential voltages, are given with respect to the network ground terminal.
2. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device.

Electrical Characteristics

V_{DD}=15V, T_A=25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD} Section						
V_{OP}	Continuously Operating Voltage				22	V
V_{DD-ON}	Start Threshold Voltage		15.5	16.5	17.5	V
V_{DD-OFF}	Minimum Operating Voltage		9.5	10.5	11.5	V
I_{DD-ST}	Startup Current	V_{DD-ON} – 0.16V			30	µA
I_{DD-OP}	Operating Supply Current	V_{DD}=15V, GATE Open		4	5	mA
I_{DD-OLP}	Internal Sink Current	V_{DD-OLP} +0.1V	50	70	90	µA
V_{TH-OLP}	I_{DD-OLP} off Voltage		6.5	7.5	8.0	V
V_{DD-OVP}	V_{DD} Over-Voltage Protection		25	26	27	V
$t_{D-VDDOVP}$	V_{DD} Over-Voltage Protection Debounce Time		100	180	260	µs
HV Section						
I_{HV}	Supply Current from HV Pin	V_{AC}=90V (V_{DC}=120V), V_{DD}=10µF		2.0		mA
I_{HV-LC}	Leakage Current After Startup	HV=500V, V_{DD}=V_{DD-OFF}+1V		1	20	µA
Oscillator Section						
f_{OSC}	Frequency in Nominal Mode	Center Frequency	62	65	68	KHz
		Hopping Range	±3.7	±4.2	±4.7	
t_{HOP}	Hopping Period			4.4		ms
f_{OSC-G}	Green-Mode Frequency		16	18	21	KHz
f_{DV}	Frequency Variation vs. V_{DD} Deviation	V_{DD}=11V to 22V			5	%
f_{DT}	Frequency Variation vs. Temperature Deviation	T_A=-40 to 105°C			5	%

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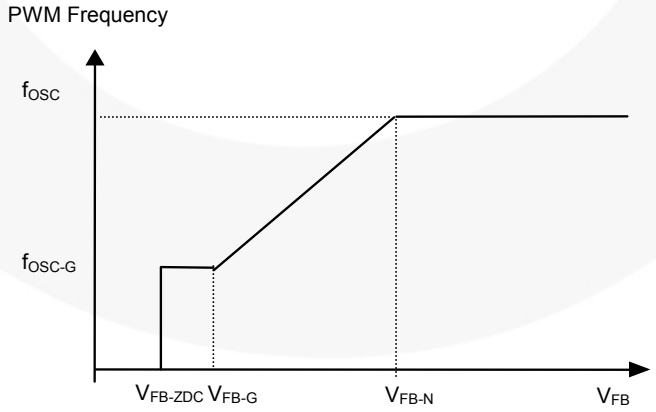

Figure 5. V_{FB} vs. PWM Frequency

Electrical Characteristics (Continued)

V_{DD}=15V, T_A=25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Feedback Input Section						
A_V	Input Voltage to Current-Sense Attenuation		1/3.75	1/3.20	1/2.75	V/V
Z_{FB}	Input Impedance		4		7	kΩ
$V_{FB-OPEN}$	Output High Voltage	FB Pin Open	5.5			V
V_{FB-OLP}	FB Open-Loop Trigger Level		3.7	4.0	4.3	V
t_{D-OLP}	Delay Time of FB Pin Open-Loop Protection	R_I=26kΩ	50	56	62	ms
V_{FB-N}	Green-Mode Entry FB Voltage		1.9	2.1	2.3	V
V_{FB-G}	Green-Mode Ending FB Voltage			V_{FB-N}-0.5		V
V_{FB-ZDC}	Zero Duty-Cycle Input Voltage		V_{FB-G} - 0.25	V_{FB-G} - 0.20	V_{FB-G} - 0.10	V
Current-Sense Section						
Z_{SENSE}	Input Impedance			12		KΩ
V_{STHFL}	Current Limit Flatten Threshold Voltage		0.87	0.90	0.93	V
V_{STHVA}	Current Limit Valley Threshold Voltage	V_{STHFL}–V_{STHVA}	0.30	0.34	0.38	V
t_{PD}	Delay to Output			100	200	ns
t_{LEB}	Leading-Edge Blanking Time		275	350	425	ns
V_{S-SCP}	Threshold Voltage for SENSE Short-Circuit Protection			0.15		V
t_{D-SSCP}	Delay Time for SENSE Short-Circuit Protection	V_{SENSE}<0.15V, R_I=26kΩ		180		µs
GATE Section						
DCY_{MAX}	Maximum Duty Cycle		70	75	80	%
V_{GATE-L}	Gate Low Voltage	V_{DD}=15V, I_O=50mA			1.5	V
V_{GATE-H}	Gate High Voltage	V_{DD}=12.5V, I_O=50mA	8			V
t_r	Gate Rising Time	V_{DD}=15V, C_L=1nF	150	250	350	ns
t_f	Gate Falling Time	V_{DD}=15V, C_L=1nF	30	50	90	ns
$I_{GATE-SOURCE}$	Gate Source Current	V_{DD}=15V, GATE=6V	250			mA
$V_{GATE-CLAMP}$	Gate Output Clamping Voltage	V_{DD}=22V			18	V

Notes:

3. When activated, the output is disabled and the latch is turned off.
4. The threshold temperature for enabling the output again and resetting the latch after OTP has been activated.

Typical Performance Characteristics