

MAGICSTRAP[®] with I²C Interface Preliminary Data Sheet

LXMS2HACNF-165

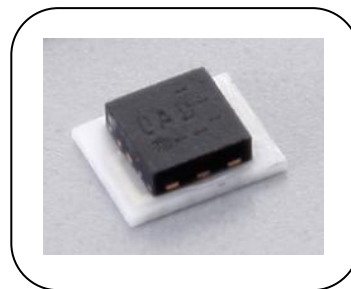


1. General description

Murata MAGICSTRAP[®] is an innovative RFID module with I²C interface as well as various RF features. It incorporates an industry standard IC.

[Features]

- Compliant to EPC global Class1 Gen2
- Ultra small package (2.5 x 2.0 x 1.0mm max)
- Supports both US (902MHz-928MHz) and EU (865-868MHz) frequency range with single design
- I²C interface to read/write from its build in memory
- Fully compatible with conventional SMT process and reflow process
- 100% green material for RoHS compliance
- Internal 3.3kbit user memory



2. Block diagram and construction

2-1. Block diagram

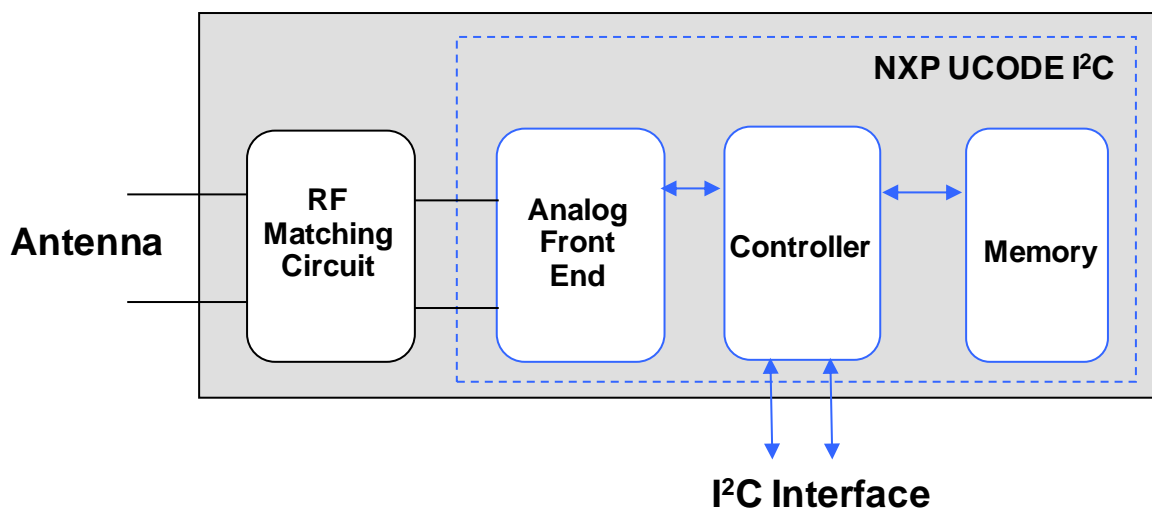


Fig1-1. Block diagram

2-2. Construction

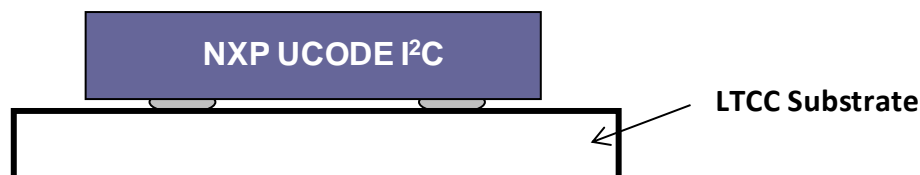


Fig1-2. Construction

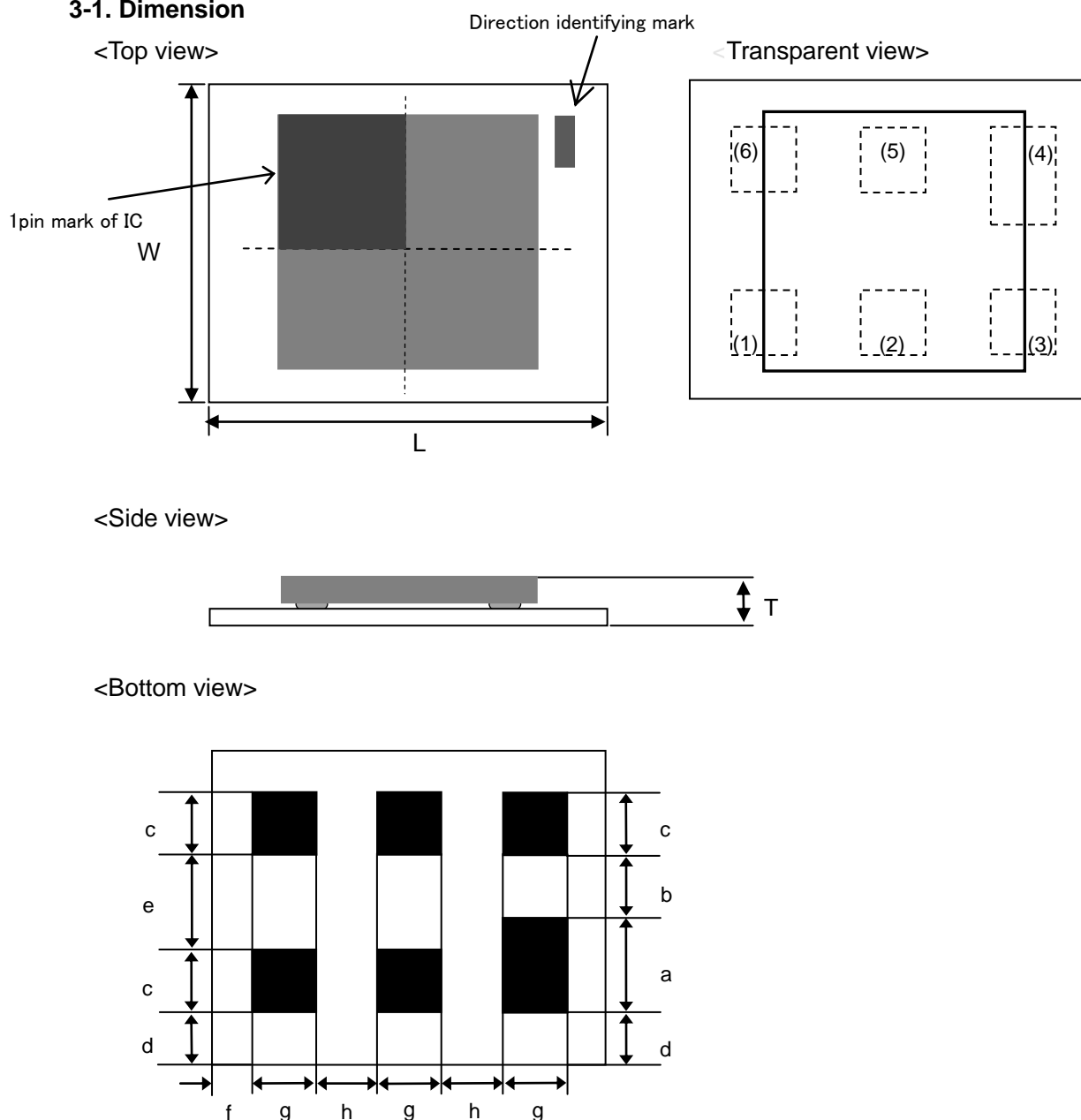
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3. Mechanical information

3-1. Dimension



Mark	Dimensions
L	2.5 ± 0.2
W	2.0 ± 0.2
T	1.0max

Mark	Dimensions
a	0.6 ± 0.1
b	0.4 ± 0.1
c	0.4 ± 0.1
d	0.3 ± 0.2

Unit : mm

Mark	Dimensions
e	0.6 ± 0.1
f	0.25 ± 0.20
g	0.4 ± 0.1
h	0.4 ± 0.1

Fig2. Dimension

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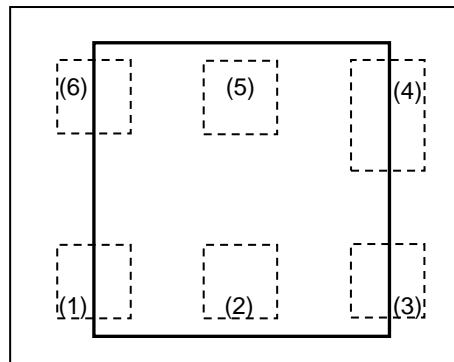


3-2. Pin assignment

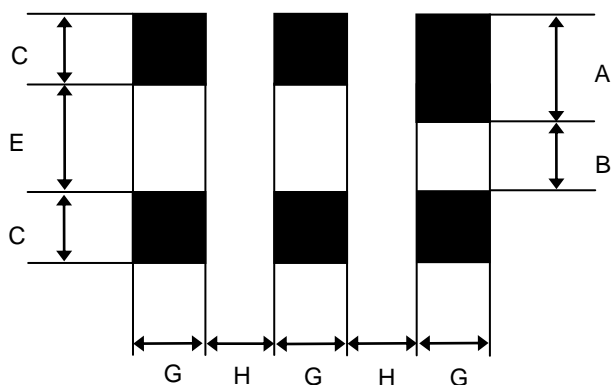
Table1. Pin assignment

No.	Terminal Name	Description
(1)	RFN1	Antenna
(2)	SCL	I2C clock
(3)	SDA	I2C data
(4)	GND	GND for I2C
(5)	VDD	Power supply for I2C (1.5V~3.7V)
(6)	RFP1	Antenna

<Top View>



3-3. Recommended land pattern



Unit : mm

Mark	Dimensions
A	0.6
B	0.4
C	0.4
E	0.6
G	0.4
H	0.4

Fig3. Recommended land pattern

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4. Electrical performance

4-1. Frequency range

865-868MHz (EU Band)

902-928 MHz (US Band)

4-2. Impedance at minimum operating power

Table2. Impedance value

(Ta=25degC, Unit : Ohm)

Impedance value	@866.5MHz	R	9
		X	-71
	@915.0MHz	R	12
		X	-65

4-3. Memory size

Part number	IC	EPC	User	TID
LXMS2HACNF-165	NXP UCODE I ² C	160bits	3328bits	96bits

4-4. Input voltage of VDD

1.8V~3.6V

5. Operating, storage temperature and moisture sensitive level

5-1. Operating temperature

-40degC ~ +85degC

5-2. Storage temperature

-40degC ~ +85degC

5-3. Moisture sensitive level

MSL1

6. RoHS compliance

This product is compliant with RoHS directive

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7. Reference antenna design on PCB

7-1. Overview of reference antenna pattern

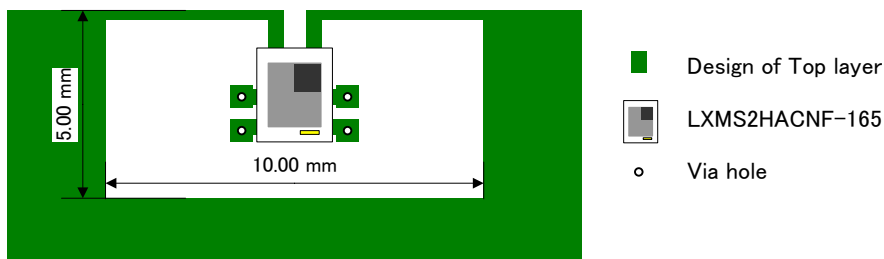


Fig4. Overview of reference antenna pattern

10mm x 5mm area is required for the reference antenna pattern where you need to avoid any unnecessary patterns except lines from this product (RFN1, RFP1, VDD, SDA, SCL, GND).

7-2. Steps to make reference antenna design on PCB

Step1) Decide the position (10mm x 5mm) and remove all the patterns from all layers.

See Appendix.A1 for 3D image of this step.

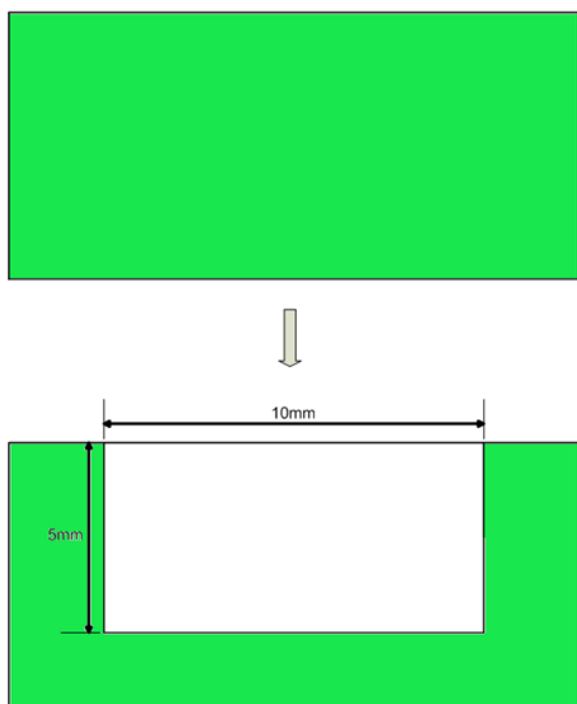


Fig5-1. Top layer image for Step1).

Step2) Copy the recommended land pattern from 3-3.

Please copy land pattern from 3-3. on Top layer and Solder_resist layer so that you can place the component on this land pattern. Center of the component is (X,Y)=(5.0, 2.7) from origin O=(0.0,0.0). See Appendix.A2 for detail design.

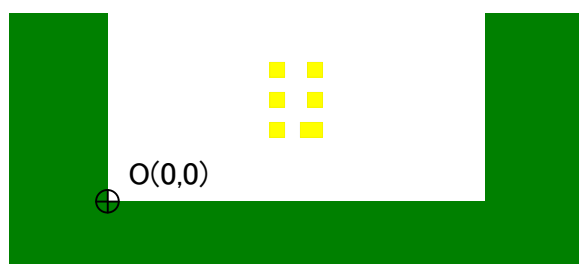


Fig5-2. Copy the recommended land pattern from 3-3

Step3) Connect antenna patterns from RFN1 and RFP1

Please draw antenna patterns from RFN1 and RFP1 pins. See Appendix.A3 for detail design.

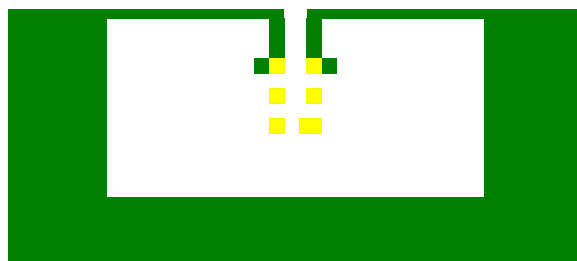


Fig5-3. Connect antenna patterns from RFN1 and RFP1

Step4) Make pads for SDA/SCL/VDD and connect from respective pins

Please make pads and via holes for SDA, SCL, VDD and GND and connect from respective pins. See Appendix.A4 for detail design.

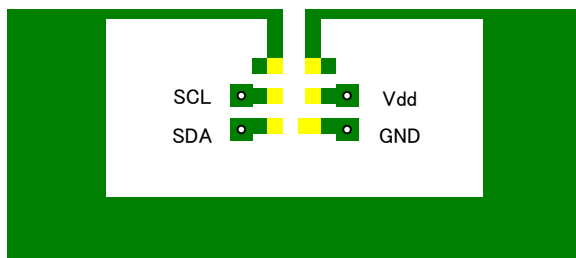


Fig5-4. Make pads for SDA, SCL, VDD and GND and connect from respective pins

Step5) Connect SDA, SCL, VDD and GND signals on Internal layer or Bottom layer

Please connect SDA, SCL, VDD and GND signals on Internal layer or Bottom layer. See Appendix.A5 for detail design.

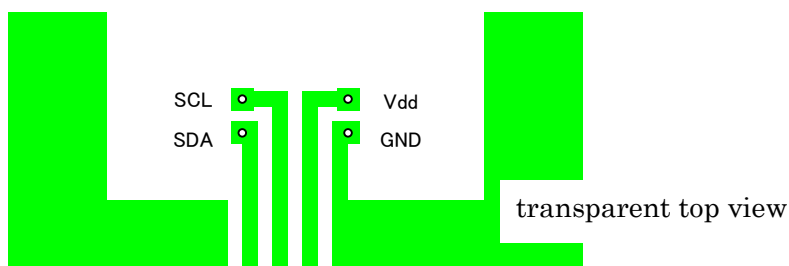


Fig5-5. Connect SDA, SCL, VDD and GND signals on Internal layer or Bottom layer.

7-3. DXF file and Gerber file

Reference antenna design for DXF format and Gerber format are also available, please request to your contact.

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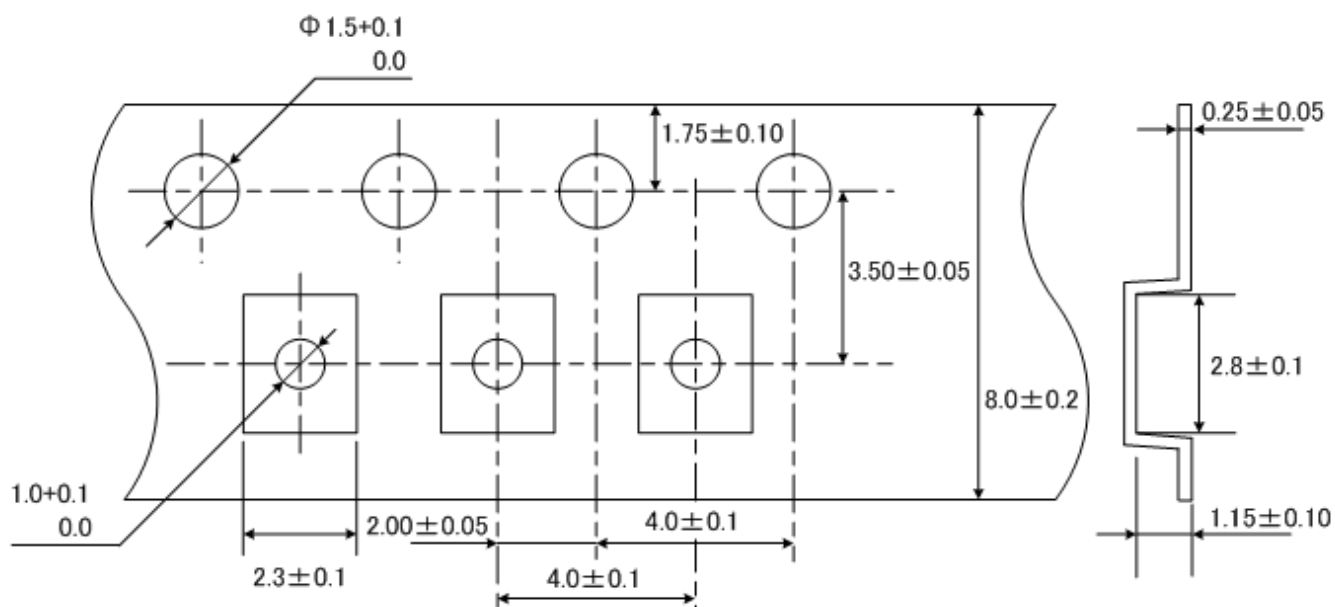
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8. Packaging

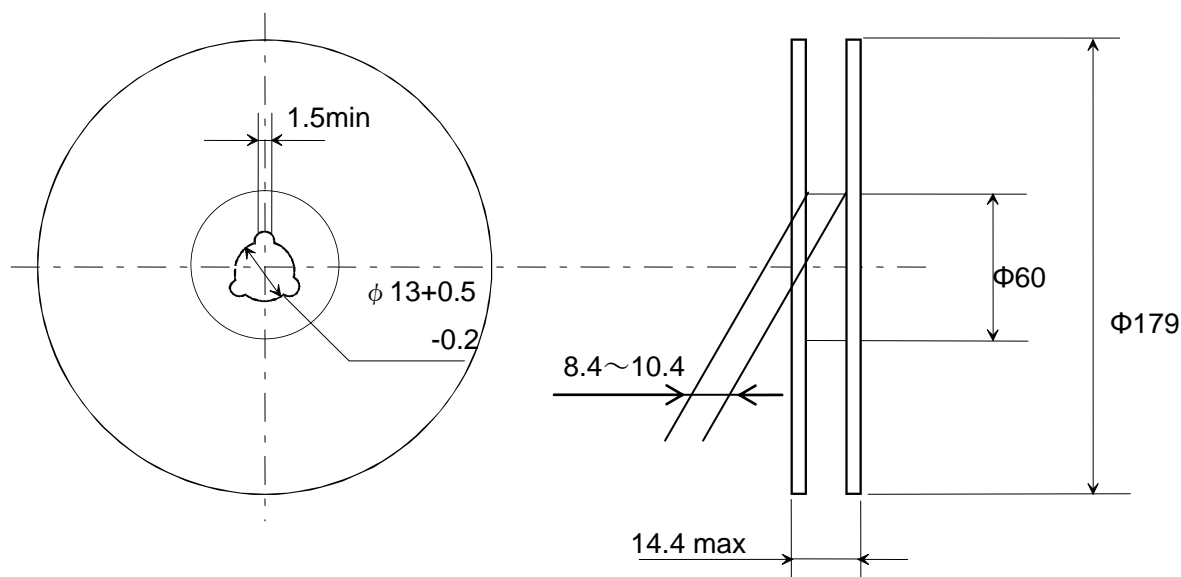
8-1. Dimensions of tape (plastic tape)

(Unit : mm)



8-2. Dimensions of reel

(Unit: mm)



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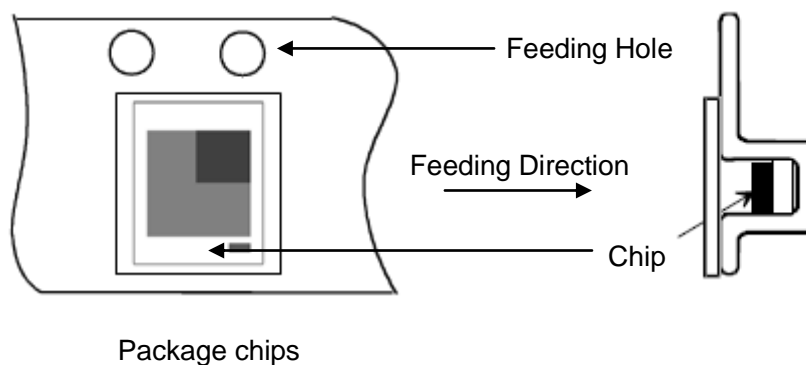
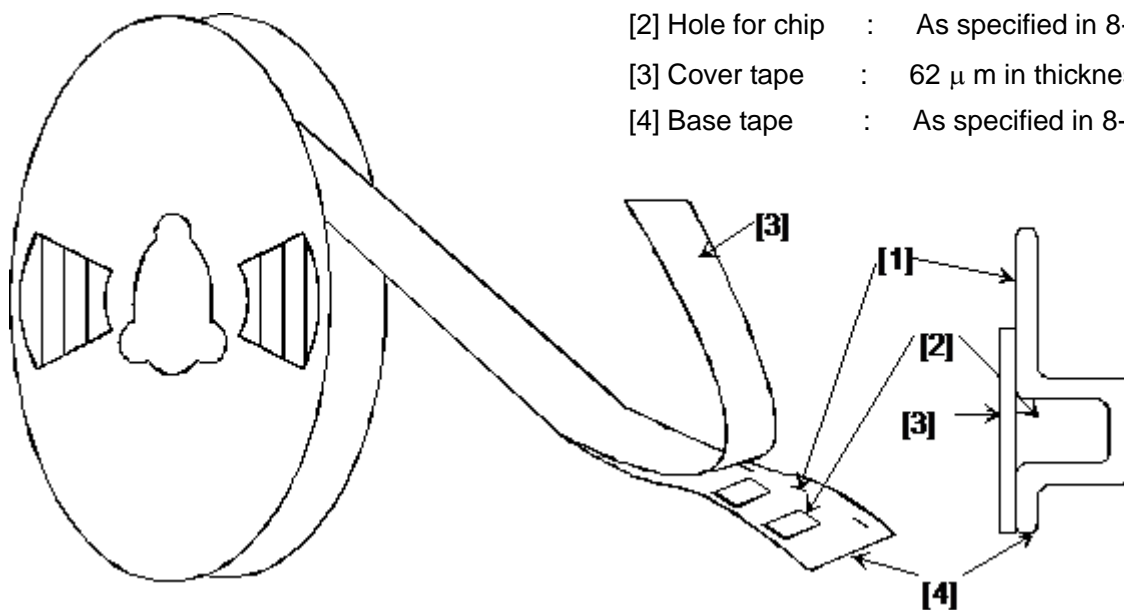
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8-3. Taping diagrams

- [1] Feeding Hole : As specified in 8-1.
- [2] Hole for chip : As specified in 8-1
- [3] Cover tape : 62 μ m in thickness
- [4] Base tape : As specified in 8-1.

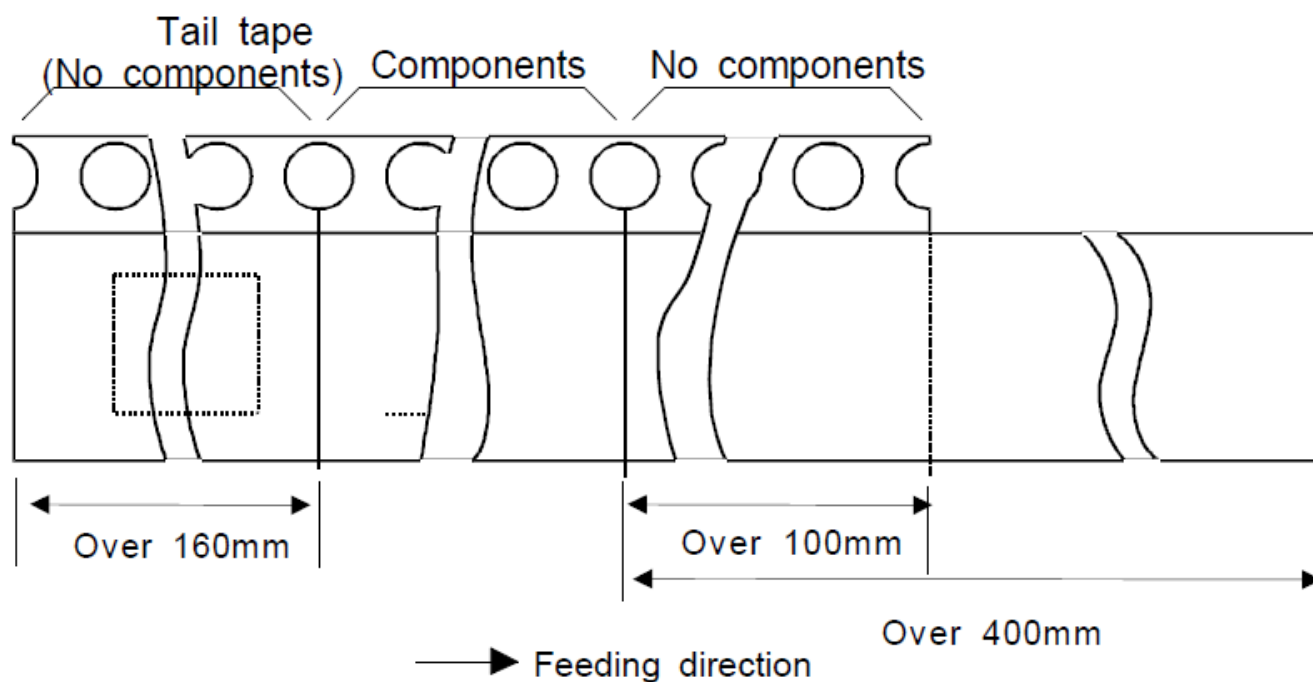


The tape for chips are wound clockwise, the feeding holes to the right side as the tape is pulled toward the user.

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8-4. Leader and tail tape



8-5. Quantity per reel

3,000pcs

8-6. Minimum order quantity

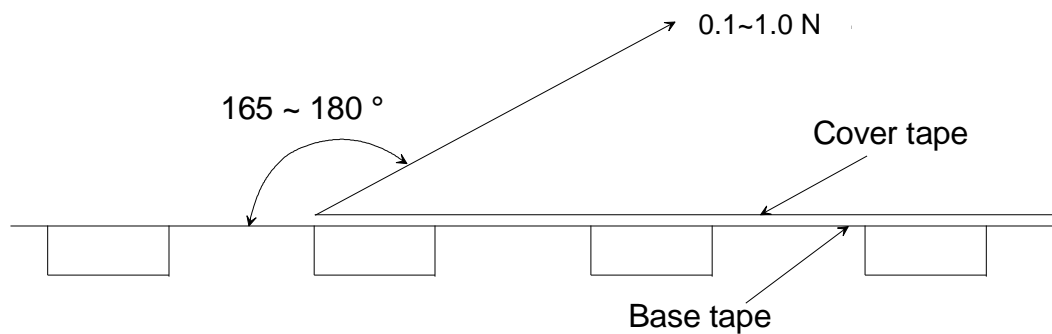
3,000pcs

8-7. Material

Base tapePlastic
ReelPlastic

8-8. Peeling force

0.1~1.0 N in the direction of peeling as shown below.



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9. Contact window / the latest data about MAGICSTRAP[®]

Email : magicstrap@ml.murata.co.jp

URL : <http://www.murata.com/products/rfid/index.html>

<Note>

This document is tentative version. The content is under development for improvement and may subject to change without notice. When we submit specification and/or approval sheet, these document should replace this technical data.

" MAGICSTRAP[®] " is the registered trademark of Murata Manufacturing. Co., Ltd. in Japan.

NOTICE

1. Storage Conditions:

To avoid damaging the solderability of the external electrodes, be sure to observe the following points.

- Store products where the ambient temperature is 5 to 30 °C and humidity min 60% RH.
(Packing materials, In particular, may be deformed at the temperature over 40 °C.).
- Store products in non corrosive gas (Cl₂, NH₃, SO₂, NO_x, etc.).
- Stored products should be used within 6 months of receipt. Solderability should be verified if this period is exceeded.

This product is applicable to MSL1 (Based on IPC/JEDEC J-STD-020)

2. Handling Conditions:

Be careful in handling or transporting products because excessive stress or mechanical shock may break products due to the nature of ceramics structure.

Handle with care if products may have cracks or damages on their terminals, the characteristics of products may change. Do not touch products with bare hands that may result in poor solderability.

3. Standard PCB Design (Land Pattern and Dimensions):

All the ground terminals should be connected to the ground patterns. Furthermore, the ground pattern should be provided between IN and OUT terminals. Please refer to the specifications for the standard land dimensions.

The recommended land pattern and dimensions is as Murata's standard. The characteristics of products may vary depending on the pattern drawing method, grounding method, land dimensions, land forming method of the NC terminals and the PCB material and thickness. Therefore, be sure to verify the characteristics in the actual set. When using non-standard lands, contact Murata beforehand.

4. Notice for Chip Placer:

When placing products on the PCB, products may be stressed and broken by uneven forces from a worn-out chucking locating claw or a suction nozzle. To prevent products from damages, be sure to follow the specifications for the maintenance of the chip placer being used. For the positioning of products on the PCB, be aware that mechanical chucking may damage products.

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5. Soldering Conditions:

Carefully perform preheating so that the temperature difference (ΔT) between the solder and products surface should be in the following range. When products are immersed in solvent after mounting, pay special attention to maintain the temperature difference within 100 °C. Soldering must be carried out by the above mentioned conditions to prevent products from damage. Contact Murata before use if concerning other soldering conditions.

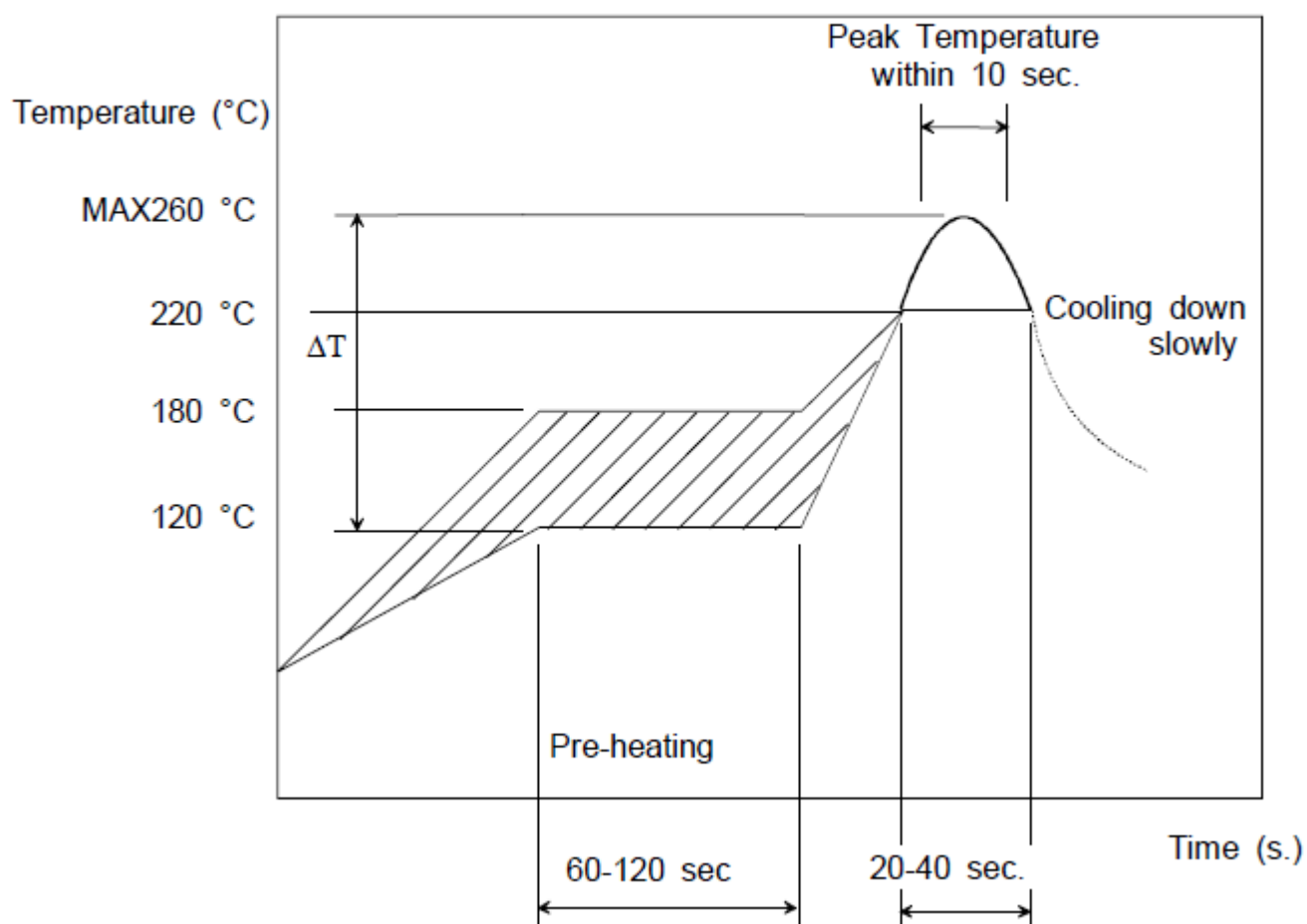
Soldering method	Temperature
Soldering iron method	• $\Delta T \leq 130$ °C
Reflow method	

- Soldering iron method conditions are indicated below.

Kind of iron Item	Ceramics heater
Soldering iron wattage	≤ 18 W
Temperature of iron-tip	≤ 350 °C
Iron contact time	within 3 s

- Diameter of iron-tip : $\phi 3.0$ mm max.
- Do not allow the iron-tip to directly touch the ceramic element.
- The soldering can be accepted just one time.

Reflow soldering standard conditions(Example)



Use rosin type flux or weakly active flux with a chlorine content of 0.2 wt % or less.

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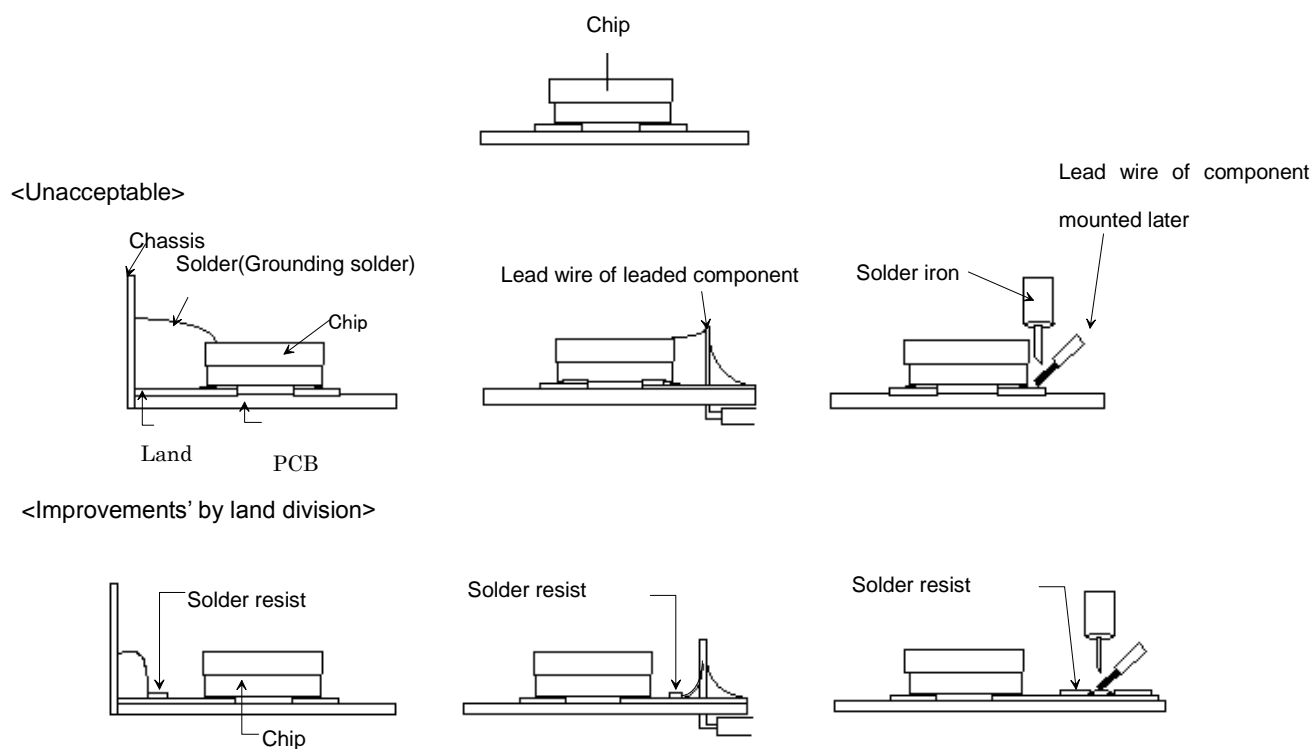
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Amount of Solder Paste:

- Ensure that solder is applied smoothly to a minimum height of 0.2 to 0.5 mm at the end surface of the external electrodes. If too much or little solder is applied, there is high possibility that the mechanical strength will be insufficient, creating the variation of characteristics.

Amount of solder paste



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6. Cleaning Conditions:

Any cleaning is not permitted.

7. Operational Environment Conditions:

Products are designed to work for electronic products under normal environmental conditions (ambient temperature, humidity and pressure). Therefore, products have no problems to be used under the similar conditions to the above-mentioned. However, if products are used under the following circumstances, it may damage products and leakage of electricity and abnormal temperature may occur.

- In an atmosphere containing corrosive gas (Cl₂, NH₃, SO_x, NO_x etc.).
- In an atmosphere containing combustible and volatile gases.
- Dusty place.
- Direct sunlight place.
- Water splashing place.
- Humid place where water condenses.
- Freezing place.

If there are possibilities for products to be used under the preceding clause, consult with Murata before actual use.

8. Input Power Capacity:

Products shall be used in the input power capacity as specified in this specification.

Inform Murata beforehand, in case that the components are used beyond such input power capacity range.

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9. Limitation of Applications:

The product is designed and manufactured for consumer application only and is not available for any application listed below which requires especially high reliability for the prevention of such defect as may directly cause damage to the third party's life, body or property.

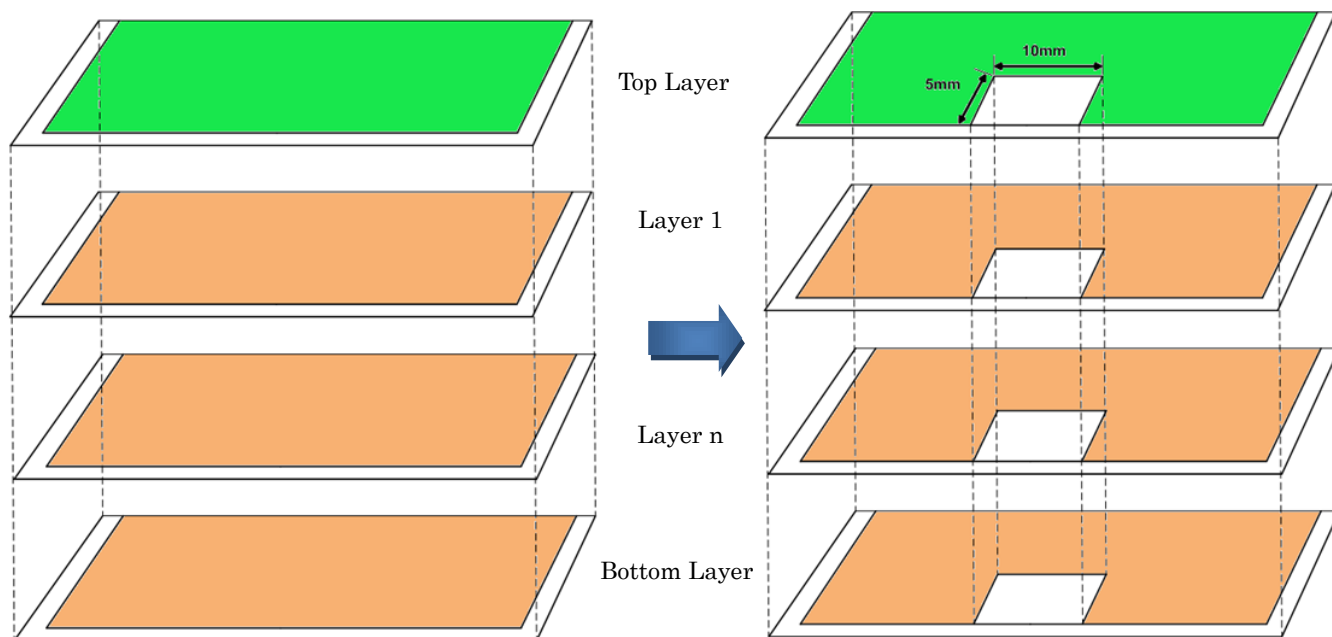
- Aircraft equipment.
- Aerospace equipment
- Undersea equipment.
- Medical equipment.
- Transportation equipment (vehicles, trains, ships, etc.).
- Traffic signal equipment.
- Disaster prevention / crime prevention equipment.
- Application of similar complexity and/ or reliability requirements to the applications listed in the above.

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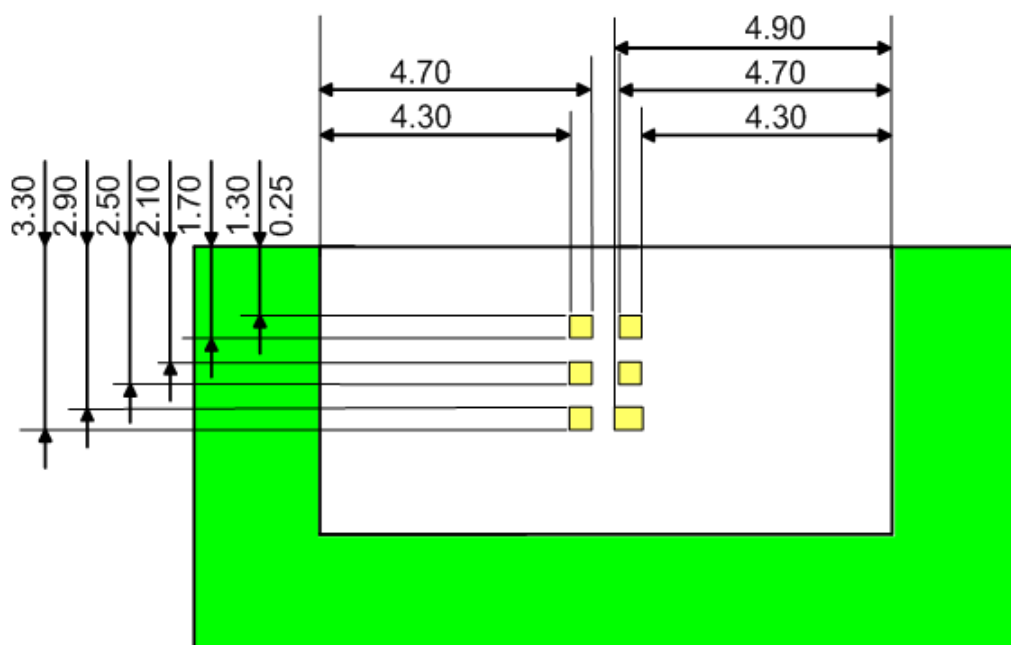
Appendix.A1



FigA-1. 3D image of Step1)

Appendix.A2

Top Layer (Top View)



FigA-2. Drawing of Step2)

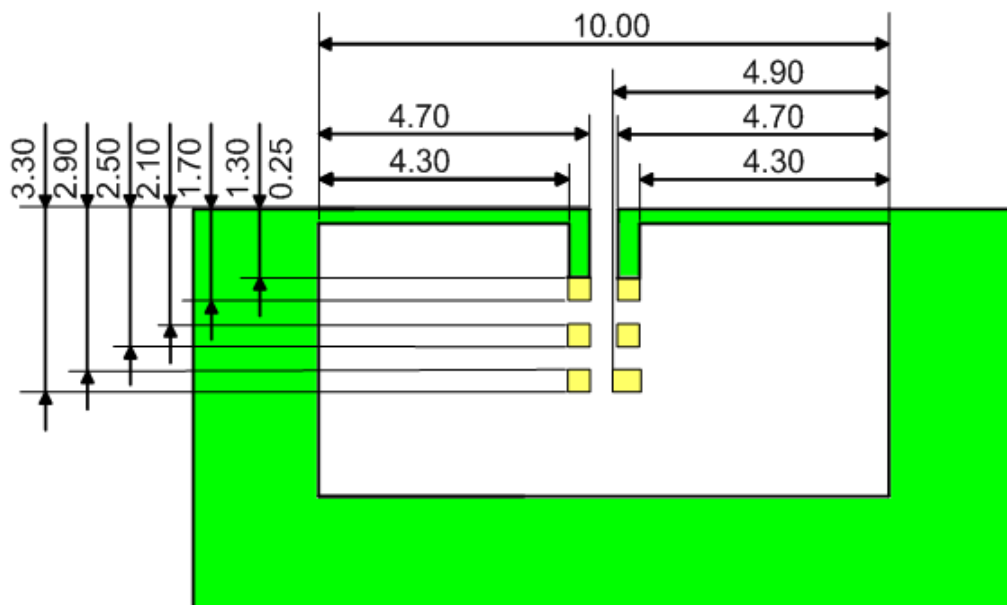
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Appendix.A3

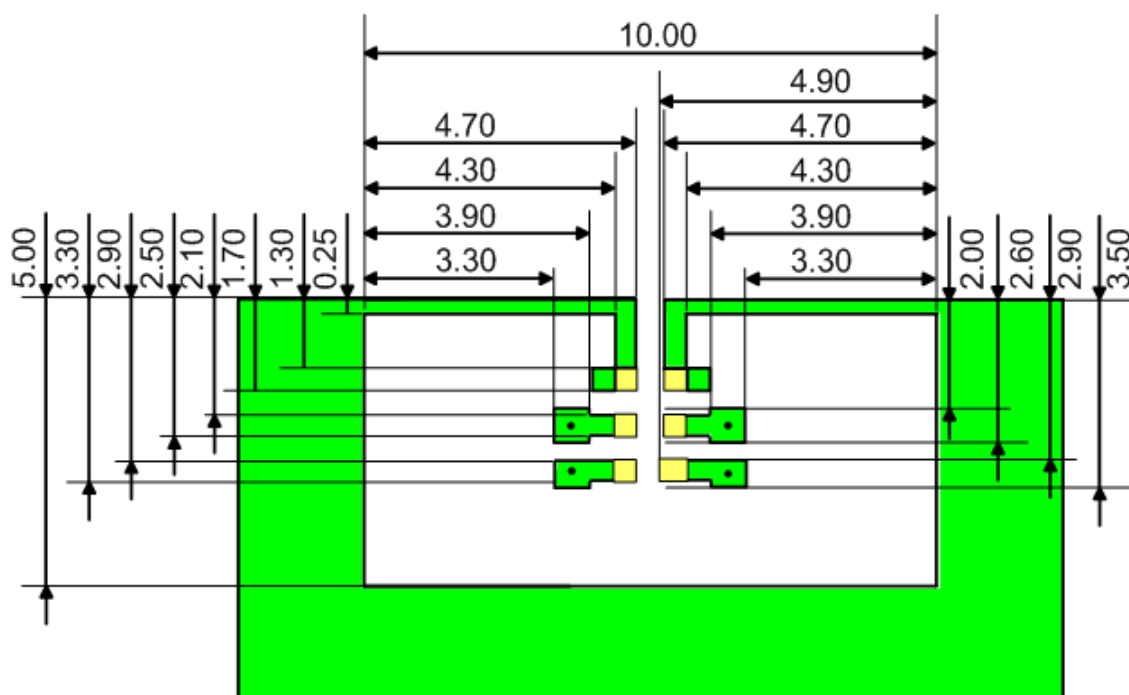
Top Layer (Top View)



FigA-3. Drawing of Step3)

Appendix.A4

Top Layer (Top View)



FigA-4. Drawing of Step4)

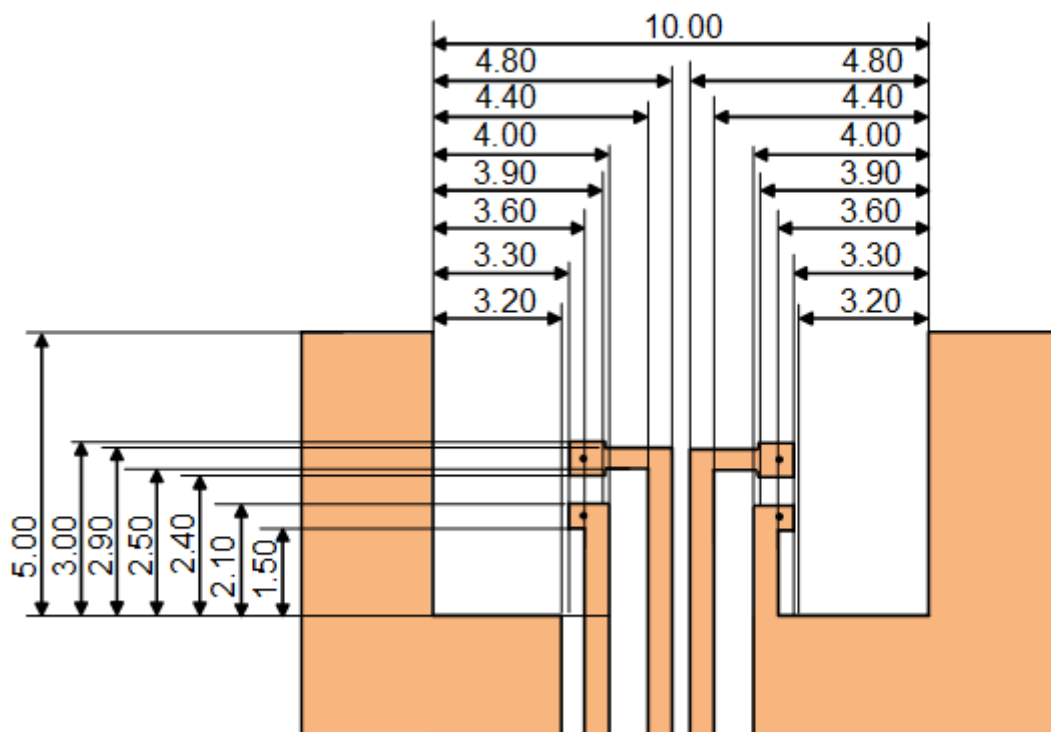
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Appendix.A5

Bottom Layer (Top View)



FigA-5. Drawing of Step5)

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Revision History

Revision Code	Date	Description
0.1	Jan.10.2014	First issue