iCE40HX-8K Breakout Board

User's Guide

November 2013
EB85_01.0

Introduction

Thank you for choosing the Lattice iCE40HX-8K Breakout Board.

This document provides technical information and instructions for using the iCE40HX-8K Breakout Board. This kit is based on the Lattice iCE40-HX8K-CT256 high performance FPGA device. Two source codes, one written in Verilog and the other in VHDL, are available to download for the iCE40HX-8K Breakout Board. Both codes are functionally the same.

The contents of this user's guide include demo operation, top-level functional descriptions of the various portions of the evaluation board, descriptions of the on-board connectors, switches, a complete set of schematics and the bill of materials for the iCE40HX-8K Evaluation Board.

Features

The iCE40HX-8K Breakout Board includes:

- **iCE40HX-8K Evaluation Board** – The iCE40HX-8K Evaluation Board features the following on board capabilities:
  - iCE40HX-8K CT256 device
  - 8 user accessible LEDs
  - SPI Flash for programming configuration
  - 40 pin 0.1" header for user connectivity
  - 0.1" holes for user connectivity
  - FTDI 2232H for USB interface
  - 12Mhz oscillator
  - Jumpers to select programming the SPI flash or iCE40HX-8K
- **Pre-loaded Demo** – The kit comes with a default design that flashes the LEDs on and off
- **USB connector Cable** – A mini B USB cable for programming the SRAM fabric of the iCE40HX-8K or the on-board SPI flash. The USB cable also powers the iCE40HX-8K evaluation board.

Figure 1 shows the top side of the iCE40HX-8K Evaluation Board indicating the specific features that are designed on the board.

Figure 1. iCE40HX-8K Evaluation Board (Top Side)

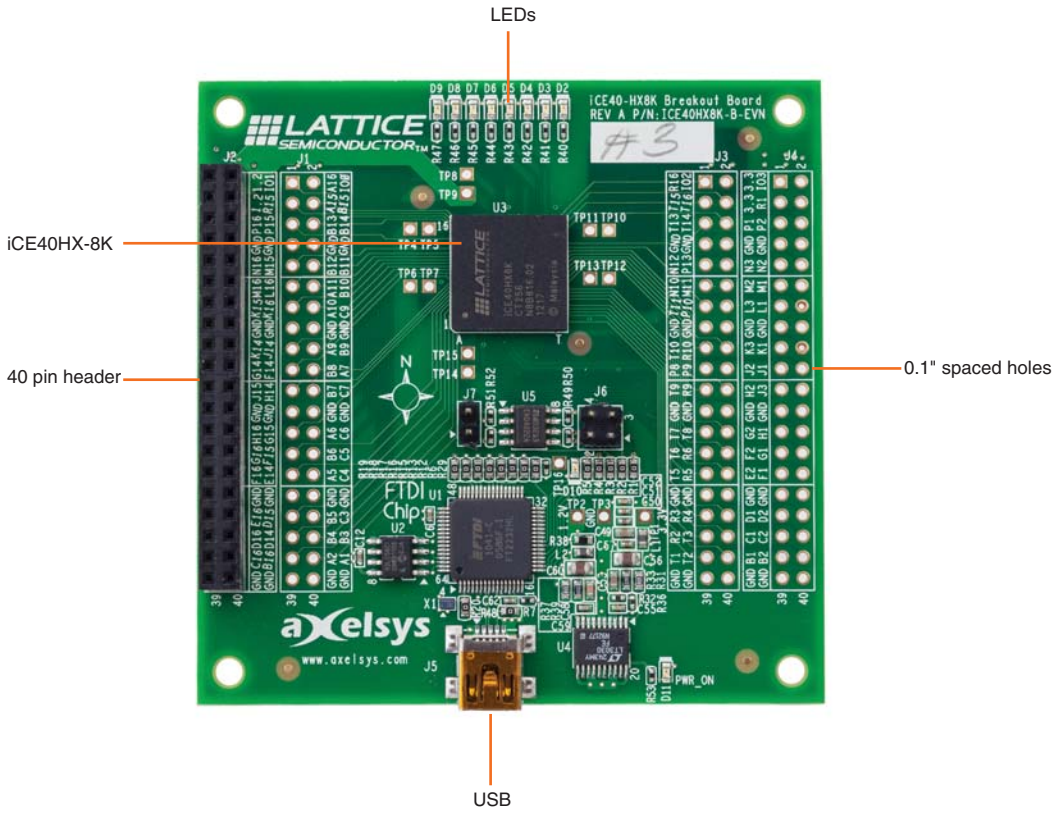
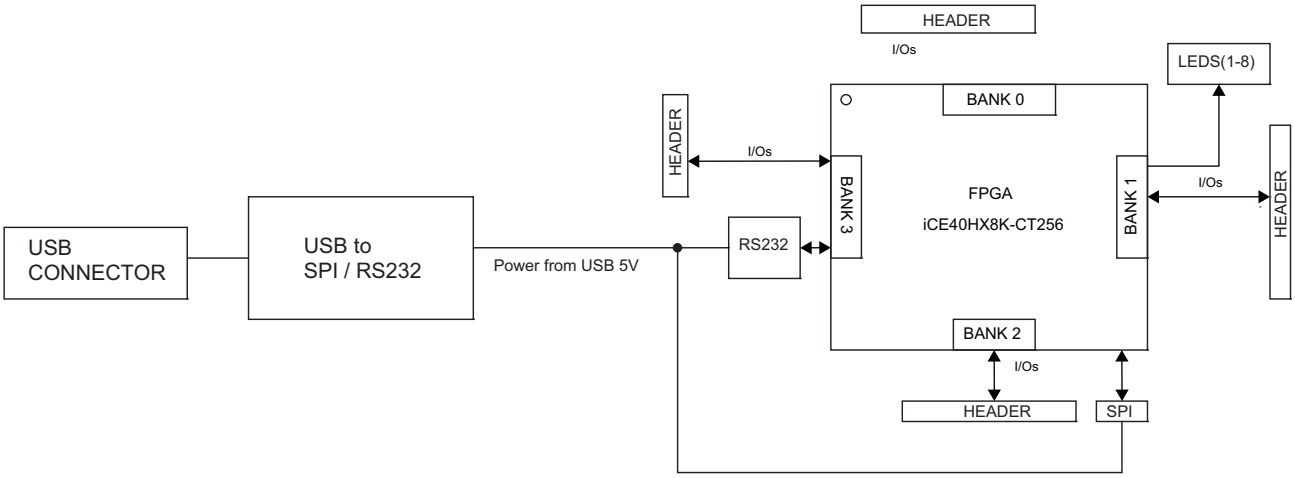


Figure 2. Block Diagram



iCE40 Device

This board features an iCE40HX-8K device with a 1.2v core supply. It is packaged in a 256 caBGA package. For a complete description of this device, see HB1011, iCE40 LP/LX/LM Family Handbook.

Software Requirements

You should install the following software before you begin developing designs for the evaluation board:

- Lattice iCEcube2 Release: 2012.09SP1.22498 or later
- Diamond Programmer: Version 2.2 or later

These software are available at the Lattice website Design Software & IP page. Make sure you log in to the Lattice website, otherwise these software downloads will not be visible.

Demonstration Design

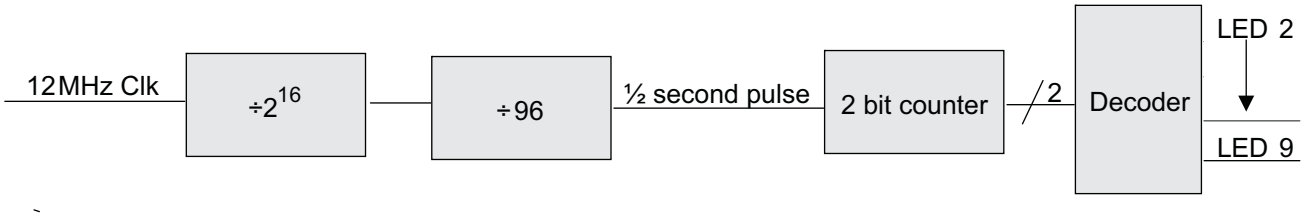
The demonstration design iCE40HX8KLED.zip file contains the following files:

- LED_VHDL.vhd (VHDL code)
- LED_Verilog.v (Verilog code)
- LED.pcf (pin constraint file)
- LED_VHDL_bitmap.hex (Bit stream file for programming FPGA.)
- LED_Verilog_bitmap.hex (Bit stream file for programming FPGA.)

Two source codes are provided, one written in VHDL and the other in Verilog. Both of these codes function identically. This provides you with an option to use either one of the code when programming the Breakout Board. When the FPGA is programmed with one of these codes, the red LEDs (D2 thru D9) will flash on for ½ second and off for ½ second.

Figure 3 shows the block diagram of the Verilog or VHDL code.

Figure 3. Block Diagram of the Verilog or VHDL Code



The source code has two counters that are used to divide the 12MHz clock by 216 and 96 generating a approximately ½ second pulse. This pulse along with the decoder will turn the LEDs (D2 thru D9) on for ½ second and off for ½ second. The decoder can be modified to have any type of LED sequence by changing either the VHDL or Verilog code.

When the board is plugged into a USB port, a +5 volt power is applied to the board that will light a green LED (D11). After the FPGA has been programmed, a green LED (D10) will light. This LED is connected to the CDONE line of the FPGA.

Board Power

The iCE40HX-8K evaluation board is powered with the USB cable. LED location D11 indicates that the board is powered up. All I/Os are driven at 3.3v.

Board I/Os

The I/Os that feed the holes and the 0.1” connector are driven at 3.3v levels. Location J2 is the populated 2 x 20 row connector. Locations J1, J3 and J4 have hole locations that the users can connect to for their specific I/O requirements.

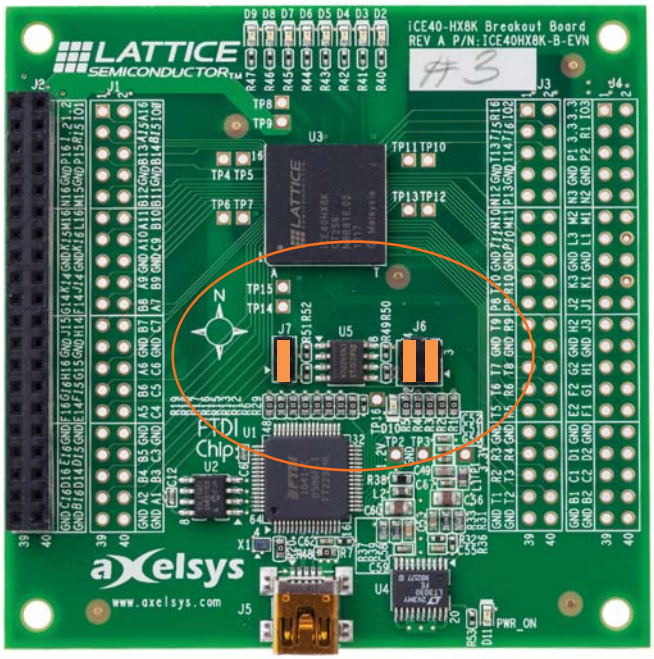
Programming Options

Two jumpers, J6 and J7 can be set for two types of FPGA Configurations:

- SPI Flash Mode, for programming the serial flash memory.
- SPI Peripheral Mode, for configuring the volatile CRAM in the FPGA.

In SPI Flash Mode the SPI signals, from the FTDI USB interface chip, programs the serial flash memory. After the memory is programmed the FPGA reads from the memory and configures its self. The advantage of programming the serial flash is that the FPGA will be re-configured after power-up. Jumpers must be in locations J7:1-2, J6:2-4, and J6:1-3. See Figure 4

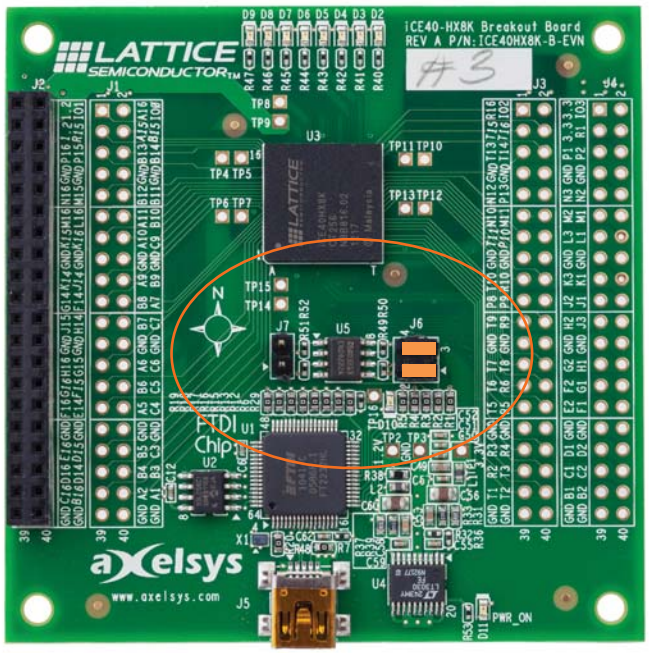
Figure 4. SPI Flash Programming



In SPI Peripheral Mode the SPI signals loads the program file into the CRAM (configuration ram) of the FPGA directly. In this mode the FPGA will lose its configuration when power is removed and must be re-configured. Jump-

ers must be in locations J6:1-2 and J6:3-4. Jumper J7 is not installed. See Figure 5

Figure 5. CRAM Programming



LED in location D10 is connected to the CDONE pin of the iCE40HX-8K. This can be monitored to determine that the iCE40HX-8K is programmed correctly.

Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
ICE40HX-8K Breakout Board	ICE40HX8K-B-EVN	

Technical Support Assistance

e-mail: techsupport@latticesemi.com

Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
November 2013	01.0	Initial release.

Appendix A. Schematic Diagrams

Figure 6. Block Diagram

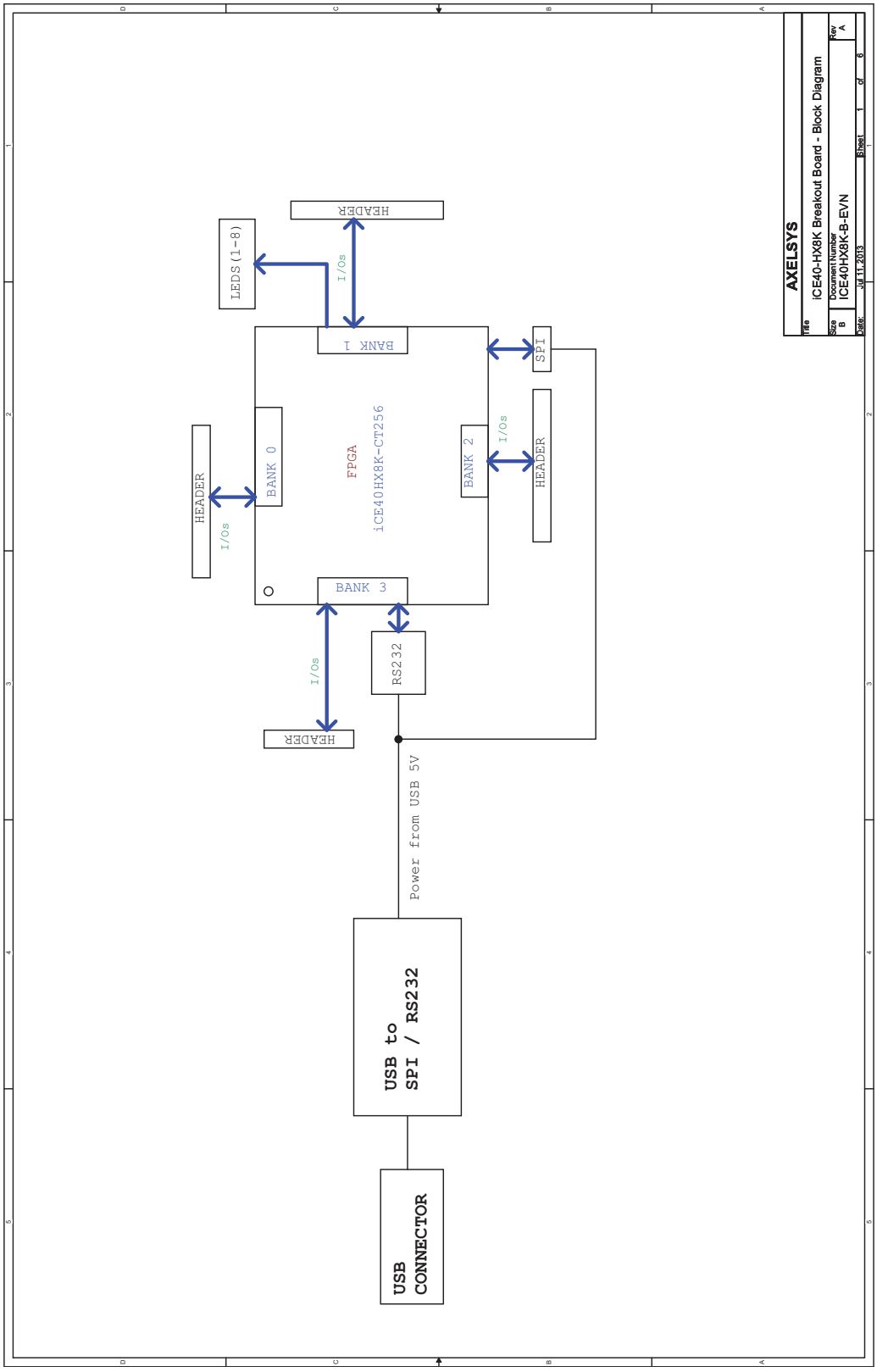


Figure 7. USB to SPI/RS232

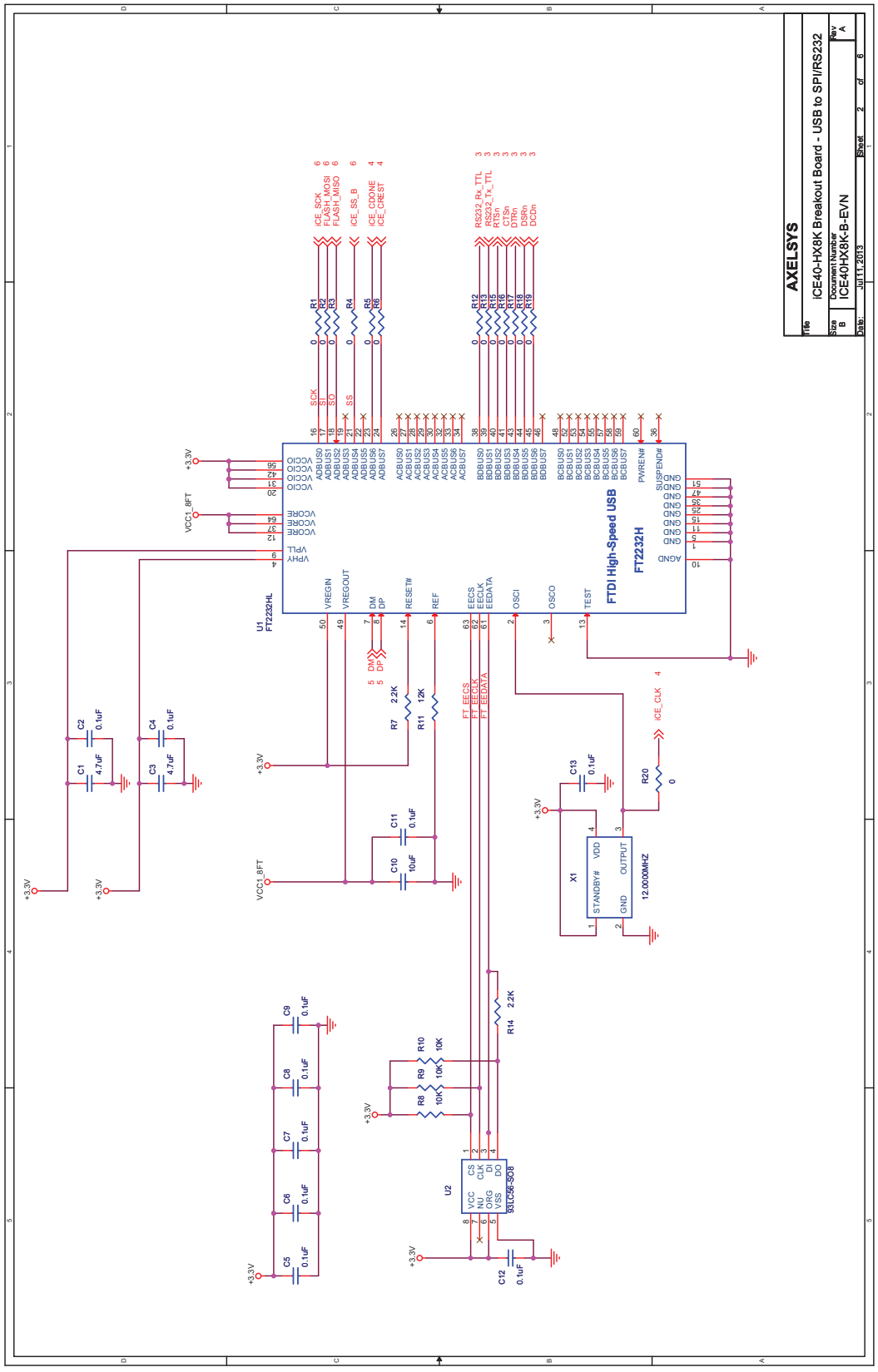


Figure 8. FPGA

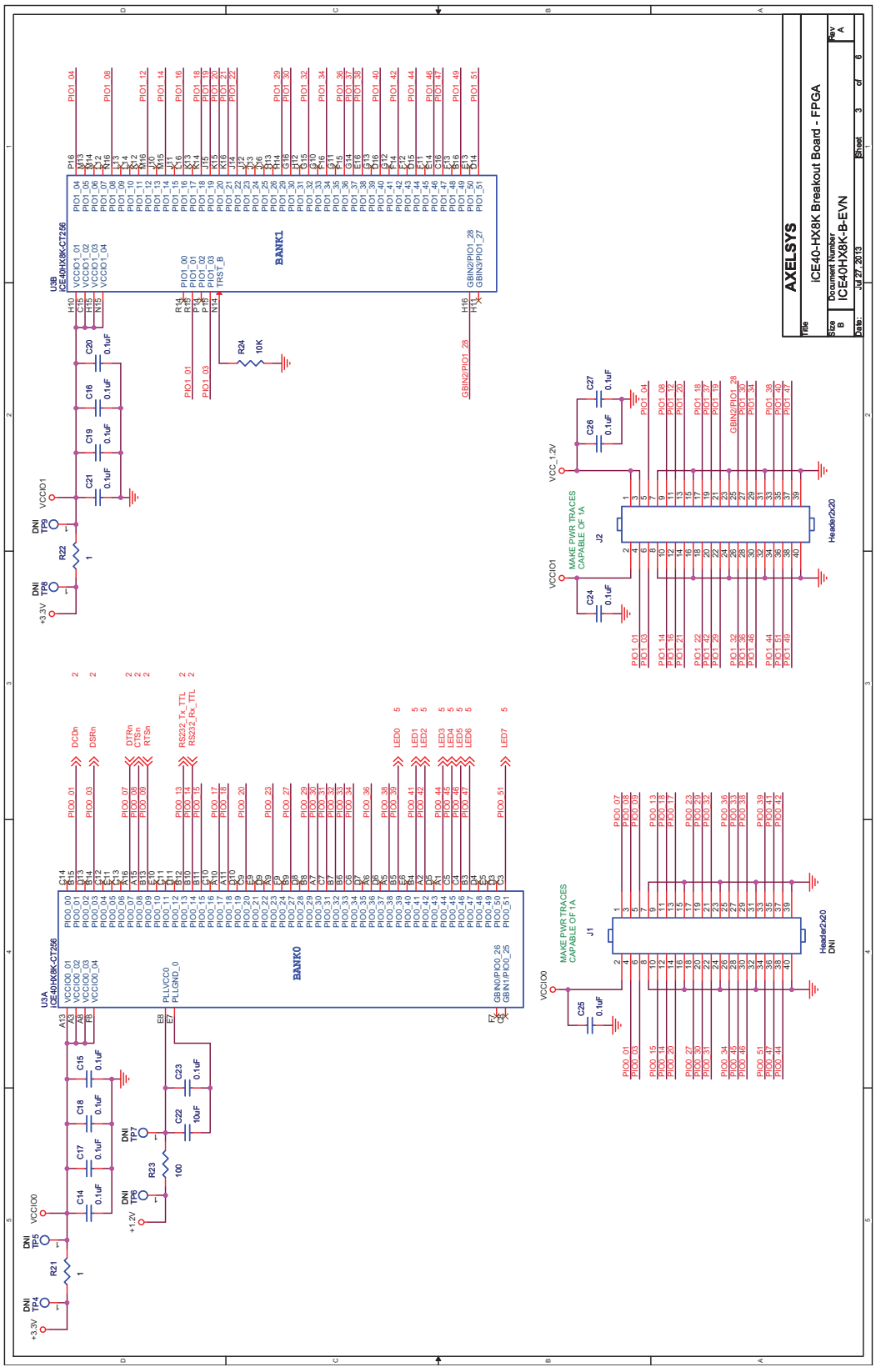


Figure 9. FPGA

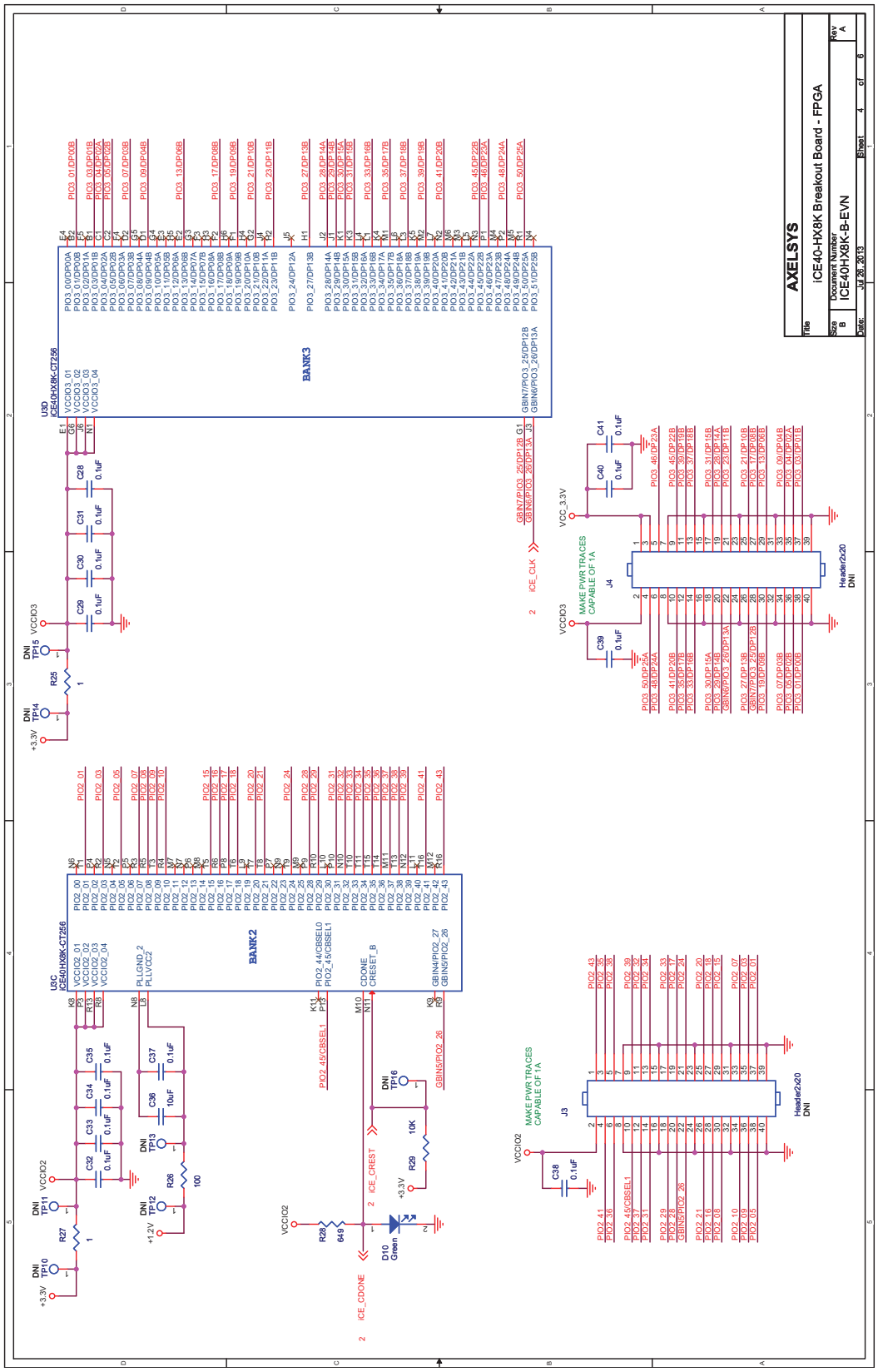


Figure 10. Power and LEDs

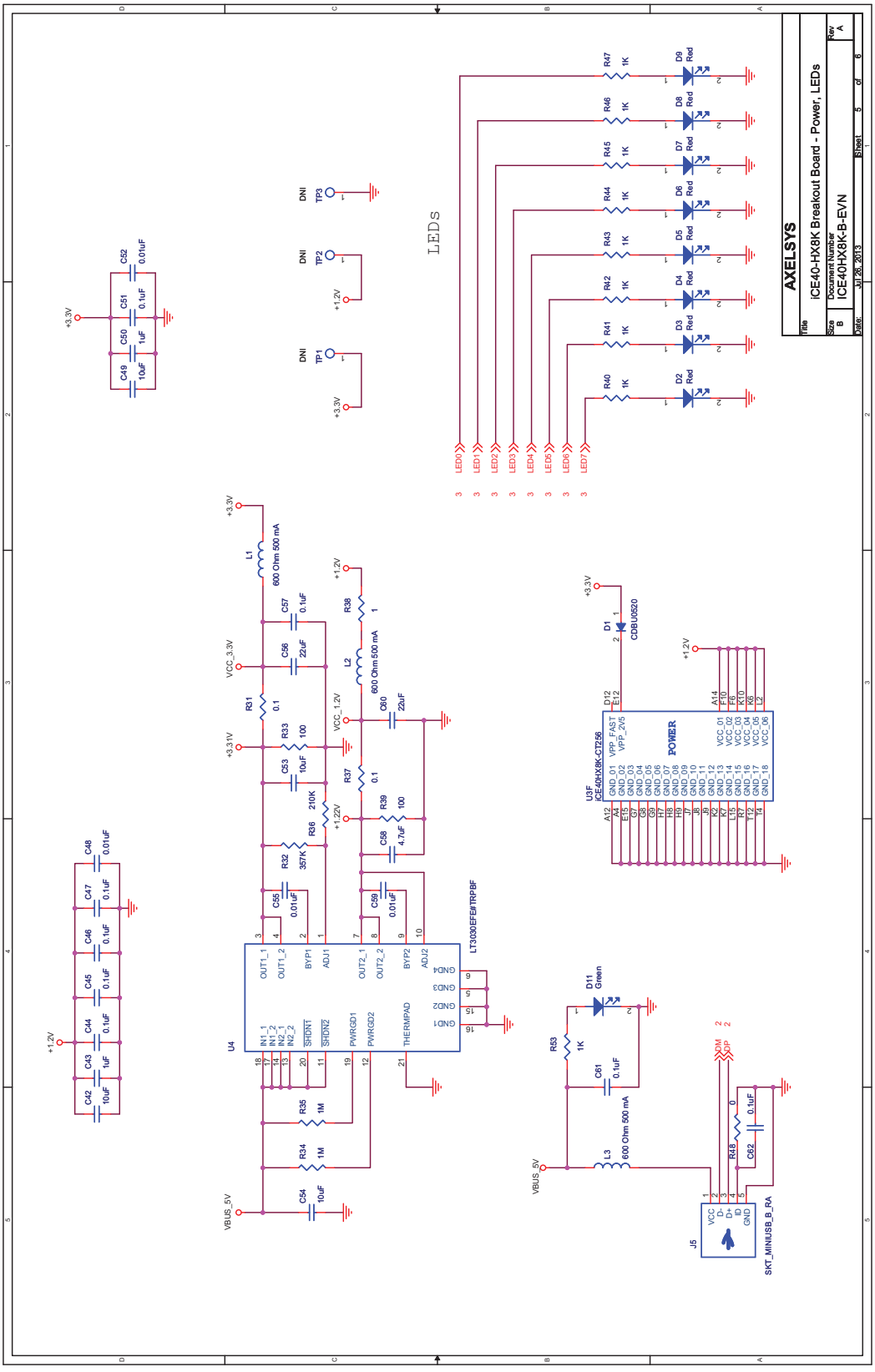


Figure 11. SPI