The Analog Mixed Signal Company

Data Sheet

Rev. 1.00 / October 2011

ZSSC3138

Sensor Signal Conditioner for Ceramic Sensor Applications

ZSSC3138

Sensor Signal Conditioner for Ceramic Sensor Applications

Brief Description

The ZSSC3138 is a member of the ZSSC313x product family of CMOS integrated circuits designed for automotive/ industrial sensor applications. All family members are well suited for highly-accurate amplification and sensor-specific correction of resistive bridge sensor signals. An internal 16-bit RISC microcontroller running a correction algorithm compensates sensor offset, sensitivity, temperature drift, and non-linearity of the connected sensor element. The required calibration coefficients are stored by the One-Pass calibration procedure on chip (EEPROM).

The ZSSC3138 offers a maximum analog gain of 420 and two offset compensation features. These fit perfectly to the requirements of ceramic thick-film-based sensor elements as well as strain gauges. The high amplification in combination with the offset compensation offers the capability to set up ceramic thick-film-based sensor applications without laser trimming, which leads to better long-term stability.

Features

- Adjustable to nearly all resistive bridge sensor types, analog gain of 420, maximum overall gain of 1680
- Enhanced sample rate: 7.8 kHz maximum
- High ADC resolution 15/16 bit
- Safety functionality sensor connection
- Internal temperature compensation
- Digital compensation of sensor offset, sensitivity, temperature drift, and non-linearity
- Output options: ratiometric analog voltage output (5 - 95% maximum, 12.4 bit resolution) or ZACwire™ (digital One-Wire Interface (OWI))
- Sensor biasing by voltage
- High voltage protection up to 33 V
- Supply current: 5.5mA maximum
- Reverse polarity and short circuit protection
- Wide operation temperature range between -40 to +150°C
- Traceability by user-defined EEPROM entries

Benefits

- Family approach offers the best fitting IC-selection to build up cost optimized applications
- No external trimming components required
- Low number of external components needed
- PC-controlled configuration and One-Pass/ end-of-line calibration via I²C™ or ZACwire™ interface: simple, cost efficient, quick, and precise
- High accuracy (0.25% FSO* @ -25 to +85°C; 0.5% FSO @ -40 to +125°C)
- Optimized for automotive/industrial environments due to robust protection circuitries, excellent electromagnetic compatibility and AEC-Q100 qualification

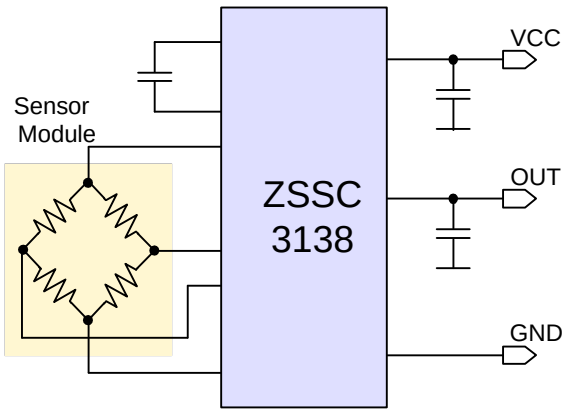
Available Support

- Evaluation Kits
- Application Notes
- Mass Calibration System

Physical Characteristics

- Supply voltage 4.5 to 5.5 V
- Operation temperature: -40°C to +125°C (-40°C to +150°C extended temperature range depending on product version)
- Available in RoSH-compliant JEDEC-SSOP14 package or delivery as die

ZSSC3138 Minimum Application Requirements



* FSO= Full Scale Output

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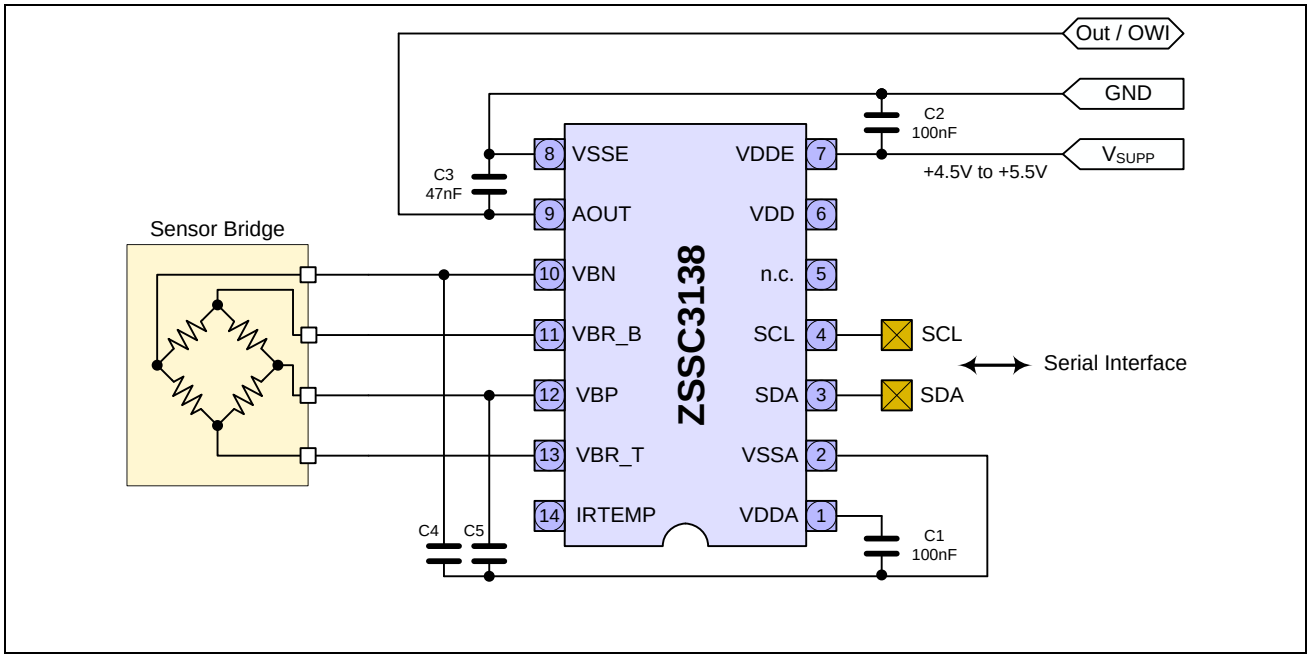
ZSSC3138 Application Example



Ordering Information *(See data sheet section 8 for complete delivery options.)*

Product Sales Code	Description	Package
ZSSC3138AA2T	ZSSC3138 SSOP14 – temperature range -40 to +125°C	Tube
ZSSC3138AA2R	ZSSC3138 SSOP14 – temperature range -40 to +125°C	Reel
ZSSC3138AE2T	ZSSC3138 SSOP14 – temperature range -40 to +150°C	Tube
ZSSC3138AE2R	ZSSC3138 SSOP14 – temperature range -40 to +150°C	Reel
ZSSC313xKITV1.0	ZSSC313x Evaluation Kit, version 1.0, including Evaluation Board, IC samples, USB cable, DVD with software and documentation	Kit
ZSSC313x Mass Calibration System V1.1	Modular Mass Calibration System (MSC) for ZSSC313x including MCS boards, cable, connectors, software DVD with documentation	Kit

Sales and Further Information

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1 Electrical Characteristics

1.1. Absolute Maximum Ratings

Parameters apply in operation temperature range and without time limitations.

Table 1.1 Absolute Maximum Ratings

No.	Parameter	Symbol	Conditions	Min	Max	Unit
1.1.1	Supply voltage [1]	$VDDE_{AMR}$	To VSSE, refer to section 3 for application circuits	-33	33	VDC
1.1.2	Potential at AOUT pin [1]	V_{OUT}	Referenced to VSSE	-33	33	VDC
1.1.3	Analog supply voltage [1]	$VDDA_{AMR}$	Referenced to VSSA, VDDE - VDDA < 0.35 V	-0.3	6.5	VDC
1.1.4	Voltage at all analog and digital IO pins	V_{A_IO} V_{D_IO}	Referenced to VSSA	-0.3	VDDA + 0.3	VDC
1.1.5	Storage temperature	T_{STG}		-55	150	°C

1) Refer to the *ZSSC313x High Voltage Protection Description* for specification and detailed conditions.

1.2. Operating Conditions

All voltages are referenced to VSSA.

Table 1.2 Operating Conditions

No.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.2.1	Ambient temperature [1] [2]	T_{AMB_TQE}	Temperature range (TQE)	-40		150	°C
		T_{AMB_TQA}	Temperature range (TQA)	-40		125	°C
		T_{AMB_TQI}	Temperature range (TQI)	-25		85	°C
1.2.2	Supply voltage	VDDE		4.5	5.0	5.5	VDC
1.2.3	Bridge resistance [3], [4]	R_{BR}		2		25	kΩ

1) See the temperature profile description in the *ZSSC313x Dice Package Document* for operation in temperature range > 125°C.
2) Maximum operation temperature range depends on product version (refer to section 8).
3) No measurement in mass production, parameter is guaranteed by design and/or quality observation.
4) Symmetric behavior and identical electrical properties (especially the low pass characteristic) of both sensor inputs of the ZSSC3138 are required. Unsymmetrical conditions of the sensor and/or external components connected to the sensor input pins of ZSSC3138 can generate a failure in signal operation.

1.3. Electrical Parameters

All parameter values are valid under the operating conditions specified in section 1.2 (special definitions excluded). All voltages referenced to VSSA.

Note: See important notes at the end of Table 1.3.

Table 1.3 Electrical Parameters

No.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.3.1. Supply Current and System Operation Conditions							
1.3.1.1	Supply current	I_S	Without bridge and load current, $f_{CLK} \leq 3$ MHz			5.5	mA
1.3.1.2	Clock frequency [1)]	f_{CLK}	Adjustment guaranteed for whole temperature range (T_{AMB_TQA})	2	3	4	MHz
1.3.2. Analog Front-End (AFE) Characteristics							
1.3.2.1	Input span	V_{IN_SP}	Analog gain: 105 to 2.8	8		275	mV/V
			Analog gain: 420 to 2.8	1		275	mV/V
1.3.2.2	Analog offset compensation range		Depends on gain adjust; refer to section 2.3.2	-300		300	% V_{IN_SP}
1.3.2.3	Parasitic differential input offset current [1)]	I_{IN_OFF}	Temperature range T_{AMB_TQE}	-10		10	nA
			Temperature range T_{AMB_TQI}	-2		2	nA
1.3.2.4	Common mode input range	V_{IN_CM}	Depends on gain adjust; XZC off, refer to section 2.3.1	0.29 * VDDA		0.65 * VDDA	V
1.3.3. Temperature Measurement (Refer to section 2.4.)							
1.3.3.1	Internal temperature diode sensitivity	ST_{TSI}	Raw values, without conditioning	700		2700	ppm FS / K

No.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.3.4. A/D Conversion							
1.3.4.1	A/D resolution [1]	r_{ADC}		13		16	Bit
1.3.4.2	DNL [1]	DNL_{ADC}	r_{ADC}=13bit, f_{CLK}=3MHz, best fit, complete AFE, range according to 1.3.4.5			0.95	LSB
1.3.4.3	INL TQA [1]	INL_{ADC}	r_{ADC}=13bit, f_{CLK}=3MHz, best fit, complete AFE, range according to 1.3.4.5, temperature range T_{AMB_TQA}			4	LSB
1.3.4.4	INL TQE	INL_{ADC}	r_{ADC}=13bit, f_{CLK}=3MHz, best fit, complete AFE, range according to 1.3.4.5, temperature range T_{AMB_TQE}			5	LSB
1.3.4.5	ADC input range	Range	r_{ADC}=13bit, f_{CLK}=3MHz, best fit, complete AFE, range according to 1.3.4.5	10		90	%VDDA
1.3.5. Sensor Check							
1.3.5.1	Sensor connection loss	R_{SCC_min}	Detection threshold	100			kΩ
1.3.5.2	Sensor input short	R_{SSC_short}	Short detection guaranteed	0		50	Ω
1.3.5.3	Sensor input no short	R_{SSC_pass}	Short is never detected	1000			Ω
1.3.6. DAC and Analog Output (Pin AOUT)							
1.3.6.1	D/A resolution	r_{DAC}	Analog output, 10-90%		12		Bit
1.3.6.2	Output current sink and source for VDDE=5V	$I_{SRC/SINK\_OUT}$	V_{OUT}: 5-95%, R_{LOAD} ≥ 2kΩ			2.5	mA
			V_{OUT}: 10-90%, R_{LOAD} ≥1kΩ			5	mA
1.3.6.3	Short circuit current	I_{OUT_max}	To VSSE/VDDE [2]	-25		25	mA
1.3.6.4	Addressable output signal range	V_{SR_OUT95}	@ R_{LOAD} ≥ 2kΩ	0.05		0.95	VDDE
		V_{SR_OUT90}	@ R_{LOAD} ≥ 1kΩ	0.1		0.90	VDDE
1.3.6.5	Output slew rate [1]	SR_{OUT}	C_{LOAD} < 50nF	0.1			V/µs
1.3.6.6	Output resistance in diagnostic mode	R_{OUT_DIA}	Diagnostic range: <4|96>%, R_{LOAD} ≥ 2kΩ <8|92>%, R_{LOAD} ≥ 1kΩ			82	Ω
1.3.6.7	Load capacitance [1]	C_{LOAD}	C3 + CL (refer to section 3)			150	nF
1.3.6.8	DNL	DNL_{OUT}		-1.5		1.5	LSB

No.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.3.6.9	INL TQA [1)]	INL_{OUT}	Best fit, r_{DAC}=12bit, temperature range T_{AMB_TQA}	-5		5	LSB
1.3.6.10	INL TQE	INL_{OUT}	Best fit, r_{DAC}=12bit, temperature range T_{AMB_TQE}	-8		8	LSB
1.3.6.11	Output leakage current @ 150°C	I_{LEAK_OUT}	In case of power or ground loss	-25		25	µA
1.3.7. System Response							
1.3.7.1	Startup time [3), 1)]	t_{STA}	To 1st output f_{CLK}=3MHz, r_{ADC}=14bit (no ROM check)			35	ms
			2nd ord. ADC			5	ms
1.3.7.2	Response time (100% jump) [1)]	t_{RESP}	f_{CLK}=4MHz, r_{ADC}=13bit Refer to Table 2.3		5780		µs
			2nd ord. ADC		340		µs
1.3.7.3	Bandwidth [1)]		Comparable to analog sensor signal conditioners			200	Hz
			2nd ord. ADC			7.8	kHz
1.3.7.4	Analog output noise peak-to-peak [1)]	$V_{NOISE,PP}$	Shorted inputs bandwidth ≤ 10kHz			10	mV
1.3.7.5	Analog output noise RMS [1)]	$V_{NOISE,RMS}$	Shorted inputs bandwidth ≤ 10kHz			3	mV
1.3.7.6	Ratiometricity error	RE_{OUT_5}	Maximum error of VDDE=5V to 4.5/5.5V			1000	ppm
1.3.7.7	Overall failure [4)], (Deviation from ideal line including INL, gain, offset and temperature errors) (No sensor-caused effects. Digital readout shown in parenthesis)	F_{ALL} TQI	f_{CLK}≤3MHz, r_{ADC}=13bit, temperature range T_{AMB_TQI}		0.25 (0.1)		% FS
		F_{ALL} TQA	f_{CLK}≤3MHz, r_{ADC}=13bit, temperature range T_{AMB_TQA}		0.5 (0.25)		% FS
		F_{ALL} TQE	f_{CLK}≤3MHz, r_{ADC}=13bit, temperature range T_{AMB_TQE}		1.0 (0.5)		% FS

1) No measurement in mass production, parameter is guaranteed by design and/or quality observation.
2) Minimum output voltage to VDDE or maximum output voltage to VSSE.
3) Depends on resolution and configuration. Start routine begins approximately 0.8ms after power on.
4) If XZC is active, additional overall failure of 25ppm/K for XZC=31 maximum. Failure decreases linearly for XZC<31.

1.4. Interface Characteristics and EEPROM

No.	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.4.1. I²C™ Interface (Refer to the *ZSSC313x Functional Description* for timing details)							
1.4.1.1	Input-high level	$V_{I^2C\_IN\_H}$		0.8			VDDA
1.4.1.2	Input-low level [1)]	$V_{I^2C\_IN\_L}$				0.2	VDDA
1.4.1.3	Output-low level [1)]	$V_{I^2C\_OUT\_L}$	Open drain, I_{OL}<2mA			0.15	VDDA
1.4.1.4	SDA load capacitance [1)]	C_{SDA}				400	pF
1.4.1.5	SCL clock frequency [1)]	f_{SCL}				400	kHz
1.4.1.6	Internal pull-up resistor [1)]	R_{I^2C}		25		100	kΩ
1.4.2. ZACwire™ One-Wire Interface (OWI)							
1.4.2.1	Input-low level [1)]	$V_{OWI\_IN\_L}$				0.2	VDDA
1.4.2.2	Input-high level [1)]	$V_{OWI\_IN\_H}$		0.75			VDDA
1.4.2.3	Output-low level [1)]	$V_{OWI\_OUT\_L}$	Open drain, I_{OL}<2mA			0.15* VDDA	VDDA
1.4.2.4	Start window [1)]		Typ: @ f_{CLK}=3MHz	96	175	455	ms
1.4.3. EEPROM							
1.4.3.1	Ambient temperature EEPROM programming [1)]	T_{AMB_EEP}		-40		150	°C
1.4.3.2	Write cycles [1)]	n_{WRI_EEP}	@write <= 85°C			100k	
			@write up to 150°C			100	
1.4.3.3	Read cycles [1), 2)]	n_{READ_EEP}	<=175°C			$8 * 10^8$	
1.4.3.4	Data retention [1) 3)]	t_{RET_EEP}	1300h @ 175°C (=100000h @ 55°C + 27000h @ 125°C + 3000h @ 150°C)			15	a
1.4.3.5	Programming time [1)]	t_{WRI_EEP}	Per written word, f_{CLK}=3MHz		12		ms

1) No measurement in mass production, parameter is guaranteed by design and/or quality observation.

2) Valid for the dice. Note that the additional package and temperature version causes restrictions.

3) Over lifetime and valid for the dice, use the calculation sheet *ZMDI Temperature Profile Calculation Sheet* for temperature stress calculation, note that additional package and temperature version caused restrictions.

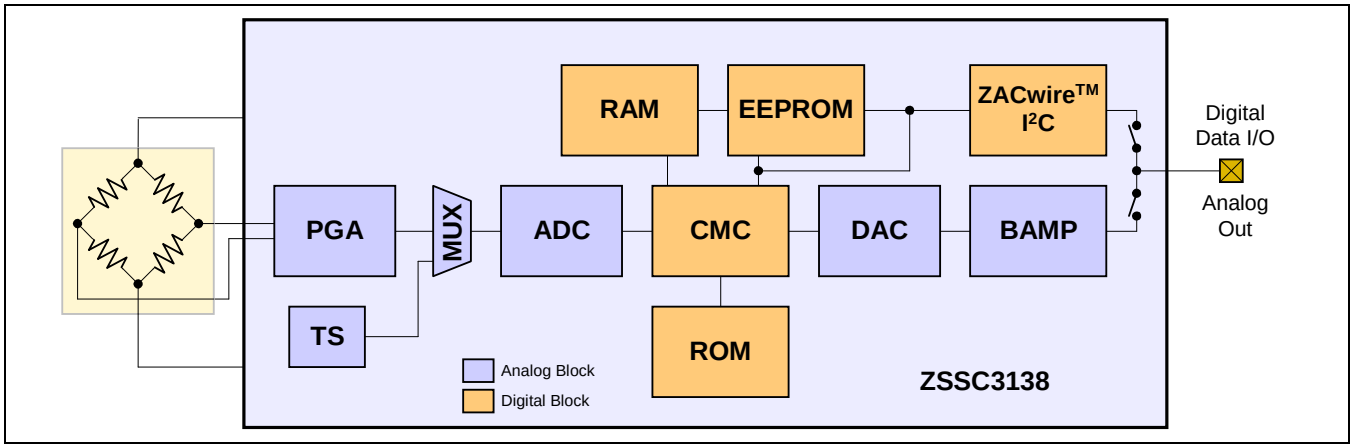
2 Circuit Description

2.1. Signal Flow

The ZSSC3138's signal path is partly analog and partly digital. The analog part is realized differentially – this means the differential bridge sensor signal is internally handled via two signal lines that are rejected symmetrically around an internal common mode potential (analog ground = VDDA/2).

As a result of the differential design, it is possible to amplify positive and negative input signals that are within the common mode range of the signal input.

Figure 2.1 Block Diagram of the ZSSC3138



PGA	Programmable Gain Amplifier
MUX	Multiplexer
ADC	Analog-to-Digital Converter
CMC	Calibration Microcontroller
DAC	Digital-to-Analog Converter
BAMP	Buffer Amplifier – output buffer OPAMP
EEPROM	Non-volatile Memory for Calibration Parameters and Configuration
TS	On-chip Temperature Sensor (pn-junction)
ROM	Memory for Correction Formula and Algorithm
RAM	Volatile Memory for Calibration Parameters and Configuration

The differential signal from the bridge sensor is pre-amplified by the programmable gain amplifier (PGA). The multiplexer (MUX) transmits the signals from either the bridge sensor, the external diode, or the separate temperature sensor to the analog-to-digital converter (ADC) in a specific sequence (alternatively, instead of the temperature diode, the internal pn-junction (TS) can be used). Subsequently, the ADC converts these signals into digital values.

The digital signal correction takes place in the calibration microcontroller (CMC). It is based on a correction formula located in the ROM and on sensor-specific coefficients stored in the EEPROM during calibration. Depending on the programmed output configuration, the corrected sensor signal is output as an analog value or in a digital format (I²C™ or ZACwire™). The configuration data and the correction parameters can be programmed into the EEPROM via the digital interfaces.

2.2. Application Modes

For each application, a configuration set must be established (generally prior to calibration) by programming the on-chip EEPROM for the following modes:

- Sensor channel
  - Input range: The gain adjustment of the AFE with respect to the maximum sensor signal span and the zero point of the ADC must be chosen.
  - Extended analog offset compensation (XZC): If required, this compensates large sensor offsets; e.g., if the sensor offset voltage is near to or larger than the sensor span.
  - Resolution/response time: The A/D converter must be configured for resolution. The ADC order (first or second order) must also be configured. These settings influence the sampling rate and the signal integration time, and thus, the noise immunity.
- Temperature
  - Temperature measurement

2.3. Analog Front-End (AFE)

The analog front-end (AFE) consists of the programmable gain amplifier (PGA), the multiplexer (MUX), and the analog-to-digital converter (ADC).

2.3.1. Programmable Gain Amplifier (PGA)

Table 2.1 shows the adjustable gains, the sensor signal spans, and the valid common mode range.

Table 2.1 Adjustable Gains, Resulting Sensor Signal Spans and Common Mode Ranges

No.	Overall Gain a_{IN}	Max. Span V_{IN_SP} [mV/V] [1]	Gain Amp1	Gain Amp2	Gain Amp3	Input Common Mode Range V_{IN_CM} as % of VDDA [2]	
						XZC = Off	XZC = On
1	420	1.8	30	7	2	29 to 65	45 to 55
2	280	2.7	30	4.66	2	29 to 65	45 to 55
3	210	3.6	15	7	2	29 to 65	45 to 55
4	140	5.4	15	4.66	2	29 to 65	45 to 55
5	105	7.1	7.5	7	2	29 to 65	45 to 55
6	70	10.7	7.5	4.66	2	29 to 65	45 to 55
7	52.5	14.3	3.75	7	2	29 to 65	45 to 55
8	35	21.4	3.75	4.66	2	29 to 65	45 to 55
9	26.3	28.5	3.75	3.5	2	29 to 65	45 to 55
10	14	53.75	1	7	2	29 to 65	45 to 55
11	9.3	80	1	4.66	2	29 to 65	45 to 55
12	7	107	1	3.5	2	29 to 65	45 to 55
13	2.8	267	1	1.4	2	32 to 57	Not applicable

2.3.2. Offset Compensation

The ZSSC3138 processes a digital sensor offset correction during the digital signal correction/conditioning by the calibration microcontroller (CMC).

The ZSSC3138 supports an analog compensation (XZC) for large offset values up to a maximum of approximately 300% of span, depending on the gain adjustment (Table 2.2). It is needed for compensation of large offset values, which would overdrive the analog signal path by uncompensated gaining. For analog sensor offset pre-compensation, a compensation voltage is added in the analog pre-gaining signal path (coarse offset removal). The analog offset compensation in the AFE can be adjusted by 6 EEPROM bits.

[1] Recommended maximum internal signal range is 75% of supply voltage.
Span is calculated by the following formula: Span = 75% / gain.

[2] Bridge in voltage mode, containing maximum input signal with XZC = +300% Offset, 14-bit accuracy. Refer to the *ZSSC313x Functional Description* for usable input signal/common mode range at bridge in current mode.

Table 2.2 Analog Zero Point Shift Ranges (XZC)

PGA Gain a_{IN}	Max. Span V_{IN_SP} [mV/V]	Offset Shift / XZC Step [% V_{IN_SP}]	Maximum Offset Shift [mV/V]	Maximum Shift (XZC = ±31) [% V_{IN_SP}]
420	1.8	12.5 %	7.8	388%
280	2.7	7.6 %	7.1	237%
210	3.6	12.5 %	15.5	388%
140	5.4	7.6 %	14.2	237%
105	7.1	12.5 %	31	388%
70	10.7	7.6 %	28	237%
52.5	14.3	12.5 %	32	388%
35	21.4	7.6 %	57	237%
26.3	28.5	5.2 %	52	161%
14	53.75	12.5 %	194	388%
9.3	80	7.6 %	189	237%
7	107	5.2 %	161	161%
2.8	267	0.83 %	72	26%

2.3.3. Measurement Cycle

Depending on EEPROM settings, the multiplexer selects the following inputs in a certain sequence.

- Temperature sensor signal
- Internal offset of the input channel (V_{OFF})
- Pre-amplified bridge sensor signal

The complete measurement cycle is controlled by the CMC. The cycle diagram in Figure 2.2 shows its basic structure. Note that the “CMV” check is not available for the ZSSC3138.

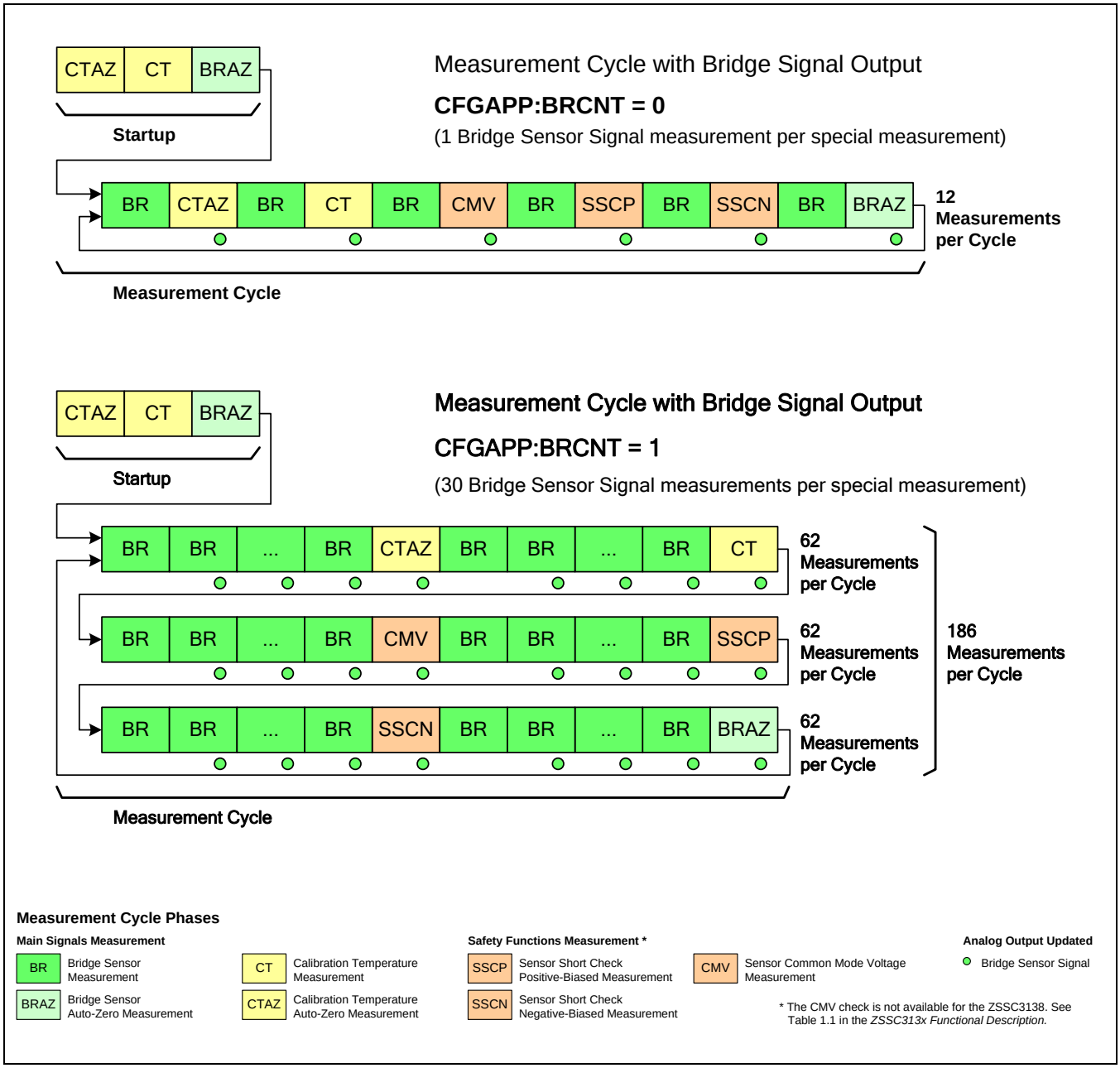
The EEPROM adjustable parameter is

- Bridge signal measurement count n = <1, 30>

After power-on, the start routine is called, and it performs all required measurements once.

Note: The tasks “CMV,” “SSC/SCC+” and “SSC/SCC-” are always performed in every measurement cycle, independent from EEPROM configuration.

Figure 2.2 Measurement Cycle



2.3.4. Analog-to-Digital Converter

The ADC is an integrating A/D converter using full-differential switched-capacitor technique.

- Programmable ADC resolutions are r_{ADC}=<13, 14>bit. The ZSSC3138 supports <15, 16>bit resolution with segmentation.

The A/D conversion is inherently monotone and insensitive to short and long term instability of the clock frequency. The conversion cycle time t_{CYC_1} depends on the desired resolution and can be roughly calculated by equation 1):

$$t_{CYC\_1} = \frac{2^r}{\left(\frac{f_{CLK}}{2}\right)} \qquad 1)$$

Where

r	Adjusted resolution in bits
f_{CLK}	Clock frequency (see specification 1.3.1)

The ZSSC3138 supports a second-order ADC mode with the advantage of a much shorter conversion cycle time but with the drawback of a lower noise immunity caused by the shorter signal integration period. The conversion cycle time in this mode t_{CYC_2} is roughly calculated by equation 2):

$$t_{CYC\_2} = \frac{2^{(r+3)/2}}{\left(\frac{f_{CLK}}{2}\right)} \qquad 2)$$

The calculation formulas give an overview about conversion time for one A/D conversion. Refer to the *ZSSC313x Bandwidth Calculation Sheet* for a detailed calculation of sampling time and bandwidth.

The result of the A/D conversion is a relative counter result corresponding to the following equation:

$$Z_{ADC} = 2^r * \left(\frac{V_{ADC\_DIFF}}{V_{ADC\_REF}} - RS_{ADC} \right) \qquad 3)$$

Where

Z_{ADC}	Number of counts (result of the conversion)
r	Adjusted resolution in bit
$V_{ADC\_DIFF/REF}$	Differential input/reference voltage of ADC
RS_{ADC}	Inherent ADC Range Shift (RS_{ADC} = $^1/_{16}$, $^1/_8$, $^1/_4$, $^1/_2$, controlled by the EEPROM content)

With the RS_{ADC} value, a sensor input signal can be shifted in the optimal input range of the ADC.

Table 2.3 Analog Output Resolution versus Sample Rate

	ADC Adjustment	Approximated Output Resolution [1]		Sample Rate f_{CON} [2]		Averaged Bandwidth	
Order O_{ADC}	r_{ADC} [Bit]	Digital [Bit]	Analog [Bit]	f_{CLK}=3MHz [Hz]	f_{CLK}=4MHz [Hz]	f_{CLK}=3MHz [Hz]	f_{CLK}=4MHz [Hz]
1	13	13	12	345	460	130	172
	14	14	12	178	237	67	89
	15	14	12	90	120	34	45
	16	14	12	45	61	17	23
2	13	13	12	5859	7813	2203	2937
	14	14	12	3906	5208	1469	1958
	15	14	12	2930	3906	1101	1468
	16	14	12	1953	2604	734	979

ADC reference voltage V_{ADC_REF} is defined by the potential between pins VBR_T and VBR_B (or between pins VDDA and VSSA, if CFGAPP:BREF=1). The theoretical ADC input range RNG_{ADC_DIFF} is equivalent to the ADC reference voltage. In practice, the ADC input range must be used at maximum from 10% to 90% of RNG_{ADC_DIFF}, which is a necessary condition for ensuring the specified accuracy, stability and non-linearity parameters of the AFE. This condition is also valid for the whole temperature range and all applicable sensor tolerances. The ZSSC3138 has no internal failsafe function that can verify compliance with this requirement.

2.4. Temperature Measurement

The ZSSC3138 supports acquiring temperature data needed for calibration of the sensor signal using an internal pn-junction temperature sensor.

Refer to the *ZSSC313x Functional Description* for a detailed explanation of temperature sensor adaptation and adjustment.

2.5. System Control and Conditioning Calculation

The system control supports the following tasks/features:

- Controlling the measurement cycle regarding to the EEPROM-stored configuration data
- Calculating the 16bit correction for each measurement signal using the EEPROM stored calibration coefficients and ROM-based algorithms (signal conditioning)
- Managing the startup sequence and start signal conditioning
- Processing communication requests received by the digital interface
- Performing failsafe tasks for the functions of ZSSC3138 and message detected errors with diagnostic states

Refer to the *ZSSC313x Functional Description* for a detailed description.

[1] ADC resolution should be one bit higher than applied output resolution if the AFE gain is adjusted so that the input range is used more than 50%. Otherwise ADC resolution should be more than one bit higher than applied output resolution.

[2] The sampling rate (A/D conversion time) is only a part of the whole cycle; refer to *ZSSC313x Bandwidth Calculation Sheet* for detailed information.

2.5.1. Operation Modes

The internal state machine represents three main states:

- Normal Operation Mode (NOM) – for continuous processing of signal conditioning
- Command Mode (CM) – for calibration and access to all internal registers
- Diagnostic Mode (DM) – for failure messaging

2.5.2. Startup Phase[1]

The startup phase consists of following parts:

1. Internal supply voltage settling phase (potential VDDA-VSSA) including reset of the circuitry by the power-on reset block (POR). Refer to the *ZSSC313x High Voltage Protection Description* for power-on/off thresholds.
   Time (beginning with VDDA-VSSA=0V): 500µs to 2000µs, AOUT: tri-state
2. System start, EEPROM read out and signature check (and ROM check, if CFGAPP:CHKROM=1).
   Time: ~200µs (~9000µs with ROM check – 28180clocks), AOUT: LOW (DM)
3. Processing the start routine for signal conditioning (all measurements and conditioning calculations).
   Time: 5x A/D conversion time, AOUT: behavior depending on configured OWI mode (refer to section 2.6):
   - OWIANA and OWIDIS => AOUT: LOW (DM)
   - OWIWIN and OWIENA => AOUT: tri-state

The analog output AOUT is activated at the end of the startup phase depending on the selected output and communication modes (refer to section 2.6). If an error is detected, Diagnostic Mode (DM) is activated and the diagnostic output signal is driven at the output.

After the startup phase, the continuous running measurement and calibration cycle is started. Refer to the *ZSSC313x Bandwidth Calculation Sheet* for detailed information about the output update rate.

2.5.3. Conditioning Calculation

The digitalized value for the bridge signal (acquired raw data) is processed with the correction formula to remove offset and temperature dependency and to compensate non-linearity up to 3rd order. The result of the correction calculation is a non-negative 15-bit value for the bridge signal (S) in the range [0; 1). This value S is clipped with programmed limitation coefficients and continuously written to the output register of the digital serial interface and the output DAC.

Note: The conditioning includes up to third-order non-linearity sensor input correction. The available adjustment ranges depend on the specific calibration parameters; for a detailed description, refer to the *ZSSC313x Functional Description*. For rough approximation purposes, offset compensation and linear correction can be considered to be limited only by the loss of resolution they cause; the second order correction is possible up to about 30% of the full scale difference from a straight line, third order up to about 20% (ADC resolution = 13-bit). The calibration principle applied is able to reduce present non-linearity errors of the sensor up to 90%. The temperature calibration includes first and second order correction and should be fairly sufficient in all relevant cases. ADC resolution also influences calibration possibilities – 1 bit more resolution reduces the calibration range by approximately 50%. Calculation input data width is at maximum 14-bit. The 15 and 16 bit ADC resolution modes of the ZSSC3138 use only a 14-bit segment of the ADC range.

[1] All timing values are roughly estimated and correlate with the internal clock frequency. Timing values are estimated for f_{CLK}=3MHz.

2.6. Analog Output AOUT

The analog output is used for outputting the analog signal conditioning result and for end-of-line communication via the ZACwire™ interface (one wire communication interface - OWI). The ZSSC3138 supports four different modes of the analog output in combination with OWI behavior:

- OWIENA: Analog output is deactivated, OWI communication is enabled.
- OWIDIS: Analog output will be activated after ~2ms power-on time; OWI communication is disabled.
- OWIWIN: Analog output will be activated after time window if OWI communication is not initiated; OWI communication can be enabled in a time window of ~500ms maximum; transmission of the START_CM command must be completed during the time window.
- OWIANA: Analog output will be activated after ~2ms power-on time if OWI communication is not initiated; OWI communication can be enabled in a time window of ~500ms maximum; transmission of the START_CM command must be completed during the time window; to communicate, the driven potential at AOUT must be overwritten by the external communication master (AOUT drive capability is current limited).

The analog output potential is driven by a unity gain output buffer, those input signal is generated by a 12.4-bit resistor string DAC. The output buffer (BAMP), a rail-to-rail OPAMP, is offset compensated and current limited, so a short circuit of analog output to ground or the power supply does not damage the ZSSC3138.

2.7. Serial Digital Interface

The ZSSC3138 includes a serial digital interface (SIF), which is used for communication with the circuit to perform calibration of the sensor module. The serial interface is able to communicate with two communication protocols: I²C™ and ZACwire™ (a one-wire communication interface referred to as OWI). The OWI can be used to perform an end-of-line calibration via the analog output pin AOUT of the completely assembled sensor module.

Refer to the *ZSSC313x Functional Description* for a detailed description of the serial interfaces and communication protocols.

2.8. Failsafe Features, Watchdog and Error Detection

The ZSSC3138 detects various possible errors. A detected error is indicated by changing the internal status to Diagnostic Mode (DM). In this case, the analog output is set to LOW (minimum possible output value = lower diagnostic range – LDR) and the output registers of the digital serial interface are set to the correlated error code.

A watchdog oversees the continuous operation of the CMC and the running measurement loop. The operation of the internal clock oscillator is verified continuously by oscillator failure detection.

EEPROM and RAM content are checked when accessed. Control registers are parity protected.

A check of the sensor bridge for broken wires is performed continuously by two comparators watching the input voltage of each input (sensor connection check, SCC). The sensor input is also continuously checked for a short (sensor short check, SSC). The connection of the external temperature sensor can be watched by the temperature sensor check.

Refer to the *ZSSC313x Functional Description* for a detailed description of safety features and methods of error messaging.

2.9. High Voltage, Reverse Polarity and Short Circuit Protection

The ZSSC3138 is designed for 5V power supply operation.

The ZSSC3138 and the connected sensor are protected from overvoltage and reverse polarity damage by an internal supply voltage limiter. The analog output AOUT can be connected (short circuit, overvoltage and reverse) with all potentials in the protection range under all potential conditions at the pins VDDE and VSSE.

All external components (see application circuit in section 3) are required to guarantee this operation. The protection is not time-limited. Refer to the *ZSSC313x High Voltage Protection Description* for a detailed description of protection cases and conditions.

3 Application Circuit Examples

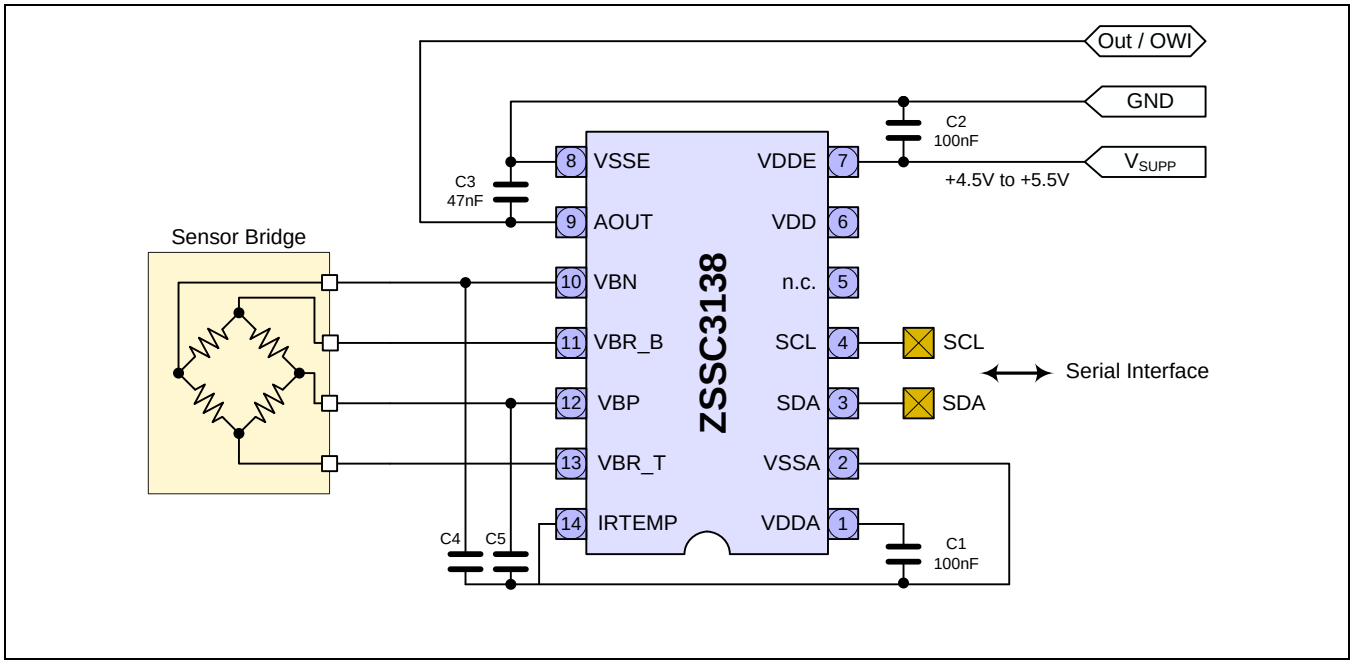
The application circuits contain external components that are needed for overvoltage, reverse polarity, and short circuit protection.

Note: Also check the *ZSSC313x Application Notes* for application examples and board layout.

Table 3.1 Application Circuit Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Notes
C1	C	100		470	nF	
C2	C	100			nF	
C3 [1, 2]	C	4	47	160	nF	The value of C3 is the sum of the load capacitor and the cable capacitance.
C4, C5 [2]	C	0		10	nF	Recommended to increase EMC immunity. The value of C4, C5 is the sum of the load capacitor and the cable capacitance.

Figure 3.1 Application with On-Chip Diode Temperature Sensor



1 The value of C3 is the sum of the load capacitor and cable capacity.
2 Higher values for C3, C4 and C5 increase EMC immunity.

4 Pin Configuration, Latch-up and ESD Protection

4.1. Pin Configuration and Latch-up Conditions

Table 4.1 Pin Configuration and Latch-up Conditions

Pin	Name	Description	Notes	Usage/ Connection [1]	Latch-up Related Application Circuit Restrictions and/or Remarks
1	VDDA	Positive analog supply voltage	Analog IO	Required/-	
2	VSSA	Negative analog supply voltage	Analog IO	Required/-	
3	SDA	I²C™ data IO	Digital IO, pull-up	-/VDDA	Trigger current/voltage to VDDA/VSSA: +/-100mA or 8/-4V
4	SCL	I²C™ clock	Digital IN, pull-up	-/VDDA	
5	n.c.	No connection			
6	VDD	Positive digital supply voltage	Analog IO	Required or open/-	Only a capacitor to VSSA is allowed; otherwise no application access
7	VDDE	Positive external supply voltage	Supply	Required/-	Trigger current/voltage: -100mA/33V
8	VSSE	Negative external supply voltage	Ground	Required/-	
9	AOUT	Analog output and One Wire IF IO	IO	Required/-	Trigger current/voltage: -100mA/33V
10	VBN	Negative input sensor bridge	Analog IN	Required/-	
11	VBR_B	Bridge bottom potential	Analog IO	Required/VSSA	Depending on application circuit, short to VDDA/VSSA possible
12	VBP	Positive input sensor bridge	Analog IN	Required/-	
13	VBR_T	Bridge top potential	Analog IO	Required/VDDA	Depending on application circuit, short to VDDA/VSSA possible
14	IRTEMP	Temperature sensor	Analog IO	Required/ VSSA	Note: External sensor to VBR_T is not supported by the ZSSC3138.

4.2. ESD Protection

All pins have an ESD protection of >2000V. The pins VDDE, VSSE and AOUT have an additional ESD protection of >4000V.

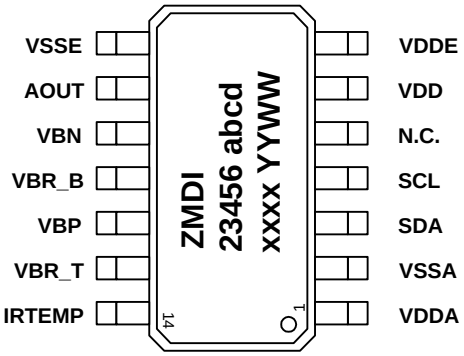
ESD protection referenced to the Human Body Model is tested with devices in SSOP14 packages during product qualification. The ESD test follows the Human Body Model with 1.5kOhm/100pF based on MIL 883, Method 3015.7.

[1] Usage: If “Required” is specified, an electrical connection is necessary – refer to the application circuits.
Connection: To be connected to this potential if not used or no application/configuration related constraints are given.

5 Package

The standard package of the ZSSC3138 is an RoHS-compliant SSOP14 “green” package (5.3mm body width) with a lead pitch of 0.65 mm.

Figure 5.1 ZSSC3138 SSOP14 Pin Diagram



6 Quality and Reliability

The ZSSC3138 is qualified according to the AEC-Q100 standard, operating temperature grade 0.

A fit rate <5fit (T=55°C, S=60%) is guaranteed.

A typical fit rate of the C7D technology, which is used for the ZSSC3138, is 2.5fit.

7 Customization

For high-volume applications that require an upgraded or downgraded functionality compared to the ZSSC3138, ZMDI can customize the circuit design by adding or removing certain functional blocks.

For customization, ZMDI has a considerable library of sensor-dedicated circuitry blocks, which enables ZMDI to provide a custom solution quickly.

Please contact ZMDI for further information.

8 Ordering Information

Product Sales Code	Description	Package
ZSSC3138AA2T	ZSSC3138 SSOP14 – temperature range -40 to +125°C	Tube
ZSSC3138AA2R	ZSSC3138 SSOP14 – temperature range -40 to +125°C	Reel
ZSSC3138AA1B	ZSSC3138 die – temperature range -40 to +125°CC	Tested dice on unsawn wafer
ZSSC3138AA1C	ZSSC3138 die – temperature range -40 to +125°CC	Tested dice on frame
ZSSC3138AA1D	ZSSC3138 die – temperature range -40 to +125°CC	Tested dice in waffle pack
ZSSC3138AE2T	ZSSC3138 SSOP14 – temperature range -40 to +150°C	Tube
ZSSC3138AE2R	ZSSC3138 SSOP14 – temperature range -40 to +150°C	Reel
ZSSC3138AE1B	ZSSC3138 die – temperature range -40 to +150°C	Tested dice on unsawn wafer
ZSSC3138AE1C	ZSSC3138 die – temperature range -40 to +150°C	Tested dice on frame
ZSSC3138AE1D	ZSSC3138 die – temperature range -40 to +150°C	Tested dice in waffle pack
ZSSC313xKITV1.0	ZSSC313x Evaluation Kit, revision 1.0, including Evaluation Board, IC samples, USB cable, DVD with software and documentation	Kit
ZSSC313x Mass Calibration System V1.1	Modular Mass Calibration System (MSC) for ZSSC313x including MCS boards, cable, connectors, software DVD with documentation	Kit

9 Additional Documents

Document	File Name
ZSSC3138 Feature Sheet	*ZSSC3138_FeatureSheet_Rev_*.PDF*
ZSSC313x Functional Description	*ZSSC313x_FunctionalDescription_Rev_*.PDF*
ZSSC313x High Voltage Protection Description	*ZSSC313x_HV_PROT_Rev_*.PDF*
ZSSC313x Dice Package	*ZSSC313x_DicePackagePin_Rev_*.PDF*
ZSSC313x Bandwidth Calculation Sheet	*ZSSC313x_Bandwidth_Calculation_Rev*.xls*
ZMDI Temperature Profile Calculation Sheet	*ZMDI_Temperature_Profile_Rev_*.xls*
ZSSC313x Application Kit Description	*ZSSC313x_APPLKIT_Rev_*.pdf*
ZSSC313x Application Notes	*ZSSC313x_AN*.pdf*

Visit ZMDI's website www.zmdi.com or contact your nearest sales office for the latest version of these documents.

10 Glossary

Term	Description
ADC	Analog-to-Digital Converter
AEC	Automotive Electronics Council
AFE	Analog Front-end
AOUT	Analog Output
BAMP	Buffer Amplifier
BR	Bridge Sensor Signal (used in commands)
CM	Command Mode
CMC	Calibration Microcontroller
CMV	Common Mode Voltage
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital-to-Analog Converter
DM	Diagnostic Mode
EEPROM	Electrically Erasable Programmable Read-Only Memory
ESD	Electrostatic Device
LDR	Lower Diagnostic Range
MUX	Multiplexer
NOM	Normal Operation Mode
OWI	One-Wire Interface
PGA	Programmable Gain Amplifier
POR	Power-on Reset
RAM	Random-Access Memory
RISC	Reduced Instruction Set Computer
ROM	Read-Only Memory
S	Bridge Signal
SCC	Sensor Connection Check
SIF	Serial Interface
SSC	Sensor Signal Conditioner or Sensor Short Check depending on context.
SSC+ (SSCP)	Positive-biased Sensor Short Check
SSC- (SSCN)	Negative-biased Sensor Short Check
T	Temperature Sensor Signal
TS	Temperature Sensor
XZC	eXtended Zero Compensation

11 Document Revision History

Revision	Date	Description
1.00	October 18, 2011	First released revision.

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