

## 6 - 18 GHz High Power Amplifier



Chip Dimensions 5.739 mm x 4.318 mm x 0.1016 mm

#### **Product Description**

The TriQuint TGA9092-SCC is a dual channel, threestage wide band HPA MMIC designed using TriQuint's proven 0.25  $\mu$ m Power pHEMT process to support a variety of high performance applications including military EW programs, VSAT, and other applications requiring wideband high power performance.

Each amplifier channel consists of one 1200  $\mu$ m input device driving a 2400  $\mu$ m intermediate stage which drives a 4800 um output stage.

The TGA9092-SCC provides a nominal 34 dBm of output power at 2dB gain compression across the 6-18 GHz range per channel . Power combined, nominal output power of 36.5 dBm can be expected with low loss external couplers. Typical per channel small signal gain is 24 dB. Typical single-ended Input/Output RL is 6-8 dB across the band.

The TGA9092-SCC is 100% DC and RF tested onwafer to ensure performance compliance. The device is available in chip form.

# TGA9092-SCC

## **Key Features and Performance**

- Dual Channel Power Amplifier
- 0.25um pHEMT Technology
- 6-18 GHz Frequency Range
- 2.8 W/Channel Midband Pout
- 5.6 W Pout Combined
- 24 dB Nominal Gain
- Balanced In/Out for Low VSWR
- 8V @ 1.2A per Channel Bias

## **Primary Applications**

- X-Ku band High Power
- VSAT



Typical Measured Pout (RF Probe)



Typical Measured Small Signal Gain

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#### TABLE I MAXIMUM RATINGS

Symbol	Parameter <u>5</u> /	Value	Notes
$\mathbf{V}^+$	Positive Supply Voltage	9 V	4/
V <sup>-</sup>	Negative Supply Voltage Range	-5V TO 0V	
$\mathbf{I}^+$	Positive Supply Current (Quiescent)	3.5 A	<u>4/</u>
$\mid I_{G} \mid$	Gate Supply Current	84.48 mA	
P <sub>IN</sub>	Input Continuous Wave Power	26 dBm	<u>4/</u>
P <sub>D</sub>	Power Dissipation	28.8 W	<u>3/ 4/</u>
T <sub>CH</sub>	Operating Channel Temperature	150 °C	<u>1/2</u> /
T <sub>M</sub>	Mounting Temperature (30 Seconds)	320 <sup>0</sup> C	
T <sub>STG</sub>	Storage Temperature	-65 to 150 <sup>0</sup> C	

- $\underline{1}$  These ratings apply to each individual FET.
- 2/ Junction operating temperature will directly affect the device median time to failure (T<sub>M</sub>). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.
- $\underline{3}$ / When operated at this bias condition with a base plate temperature of 70  $^{0}$ C, the median life is reduced from 1.6 E+6 to 5.4 E+4 hours.
- 4/ Combinations of supply voltage, supply current, input power, and output power shall not exceed P<sub>D</sub>.
- 5/ These ratings represent the maximum operable values for this two-channel device.



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#### TABLE II DC PROBE TEST (TA = 25 °C ± 5 °C)

Symbol	Parameter	Minimum	Maximum	Unit
Imax <sub>(Q1)</sub>	Maximum Current	400	800	mA
Gm (Q1)	Transconductance	200	600	mS
V <sub>P</sub>	Pinch-off Voltage	-1.5	-0.5	V
BVGS	Breakdown Voltage Gate- Source	-30	-13	V
BVGD	Breakdown Voltage Gate- Drain	-30	-13	V

# TABLE III AUTOPROBE FET PARAMETER MEASUREMENT CONDITONS

FET Parameters	Test Conditions
$G_m$ : Transconductance; $\frac{(I_{DSS} - IDS 1)}{VG1}$	For all material types, $V_{DS}$ is swept between 0.5 V and VDSP in search of the maximum value of $I_{ds}$ . This maximum $I_{DS}$ is recorded as IDS1. For Intermediate and Power material, IDS1 is measured at $V_{GS} = VG1 = -0.5$ V. For Low Noise, HFET and pHEMT material, $V_{GS} = VG1 = -0.25$ V. For LNBECOLC, use $V_{GS} = VG1 = -0.10$ V.
$V_P$ : Pinch-Off Voltage; $V_{GS}$ for $I_{DS} = 0.5$ mA/mm of gate width.	$V_{\rm DS}$ fixed at 2.0 V, $V_{\rm GS}$ is swept to bring $I_{\rm DS}$ to 0.5 mA/mm.
$V_{BVGD}$ : Breakdown Voltage, Gate-to-Drain; gate-to- drain breakdown current ( $I_{BD}$ ) = 1.0 mA/mm of gate width.	Drain fixed at ground, source not connected (floating), 1.0 mA/mm forced into gate, gate-to-drain voltage ( $V_{GD}$ ) measured is $V_{BDGD}$ and recorded as BVGD; this cannot be measured if there are other DC connections between gate-drain, gate-source or drain-source.
$V_{BVGS}$ : Breakdown Voltage, Gate-to-Source; gate-to- source breakdown current ( $I_{BS}$ ) = 1.0 mA/mm of gate width.	Source fixed at ground, drain not connected (floating), 1.0 mA/mm forced into gate, gate-to-source voltage ( $V_{GS}$ ) measured is $V_{BDGS}$ and recorded as BVGS; this cannot be measured if there are other DC connections between gate-drain, gate-source or drain-source.
I <sub>MAX</sub> : Maximum I <sub>DS</sub> .	Positive voltage is applied to the gate to saturate the device. $V_{DS}$ is stepped between 0.5 V up to a maximum of 3.5 V, searching for the maximum value of $I_{DS}$ .

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## TABLE IV RF WAFER CHARACTERIZATION TEST\* $(T_A = 25^{\circ}C \pm 5^{\circ}C)$

 $(Vd = 8V, Id = 1.2A \pm 5\%)$ 

Parameter	Test Condition	Limit		Units	
		Min	Nom	Max	
Small-signal	F = 6  to  17  GHz	20	24	-	dB
Power Gain	F = 18  GHz	18			
Input Return Loss	F = 6  to  18  GHz		6		dB
Output Return Loss	F = 6  to  18  GHz		8		dB
Output Power	F = 6  to  8  GHz	32	34.5	-	dBm
@ 2dB gain compression	F = 9 to 18 GHz	32.5		-	
Power Added Efficiency	F = 6  to  18  GHz	12	25	-	%

Note: RF probe data taken at 1 GHz steps

\* This information is based on the per-channel device.

#### TABLE V THERMAL INFORMATION\*

Parameter	Test Conditions	Т <sub>СН</sub> (°С)	R <sub>θJC</sub> (°C/W)	T <sub>M</sub> (HRS)
$R_{\theta JC}$ Thermal Resistance (channel to backside of carrier)	Vd = 8 V $I_D = 2.4 A$ Pdiss = 19.2 W	144.56	3.88	1.6 E+6

Note: Assumes eutectic attach using 1.5 mil 80/20 AuSn mounted to a 20 mil CuMo Carrier at 70°C baseplate temperature. Worst case condition with no RF applied, 100% of DC power is dissipated.

\* This information is a result of a thermal model analysis based on the entire two-channel device.



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## Data Based on the 50th Percentile On-Wafer RF Probe Test Results, Sample Size = 3370 Devices

Bias Conditions: Vd = 8 V, Id = 1.2 A



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## Data Based on the 50th Percentile On-Wafer RF Probe Test Results, Sample Size = 3370 Devices

**Bias Conditions:** Vd = 8 V, Id = 1.2 A





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Bias Conditions: Vd = 8 V, Id = 1.2 A





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#### Chip Assembly and Bonding Diagram



Note: All Vd's may be connected external to the MMIC.

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

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## **Assembly Process Notes**

Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300°C.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Discrete FET devices with small pad sizes should be bonded with 0.0007-inch wire.
- Maximum stage temperature is 200°C.

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.