Surface Mount Chip Capacitors

Safety Certified Surge Protection Chip

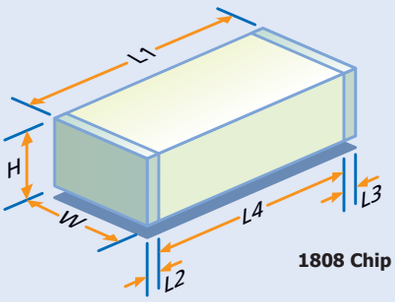
C0G/X7R

Syfer Technology's Surge Protection (SP) range of ceramic chip capacitors are Class Y3/X2 compliant and designed specifically for use in equipment certified to IEC 60950 including modems, faxes, telephones and other electronic equipment where over voltage surges can occur - i.e. a lightning strike.

This range of capacitors is approved and certified by TÜV certificate numbers R2110618 for C0G and R60003323 for X7R.

These multilayer chip capacitors meet the electrical requirements of IEC 60384-14 and EN 132400, and the electrical specification and creepage limitations of IEC 60950.

An application guide is available on request.



1808 Chip Size

Case size	Nominal Cap value	Class	Dielectric	Tolerance	Approvals
1808	4.7pF	Y3/X2	C0G/NP0	±0.25pF, ±0.5pF	UL/TÜV
1808	5.6pF	Y3/X2	C0G/NP0	±0.25pF, ±0.5pF	UL/TÜV
1808	6.8pF	Y3/X2	C0G/NP0	±0.25pF, ±0.5pF	UL/TÜV
1808	8.2pF	Y3/X2	C0G/NP0	±0.25pF, ±0.5pF	UL/TÜV
1808	10pF	Y3/X2	C0G/NP0	±1%, ±2%, ±5%, ±10%, ±20%	UL/TÜV
1808	12pF	Y3/X2	C0G/NP0	±1%, ±2%, ±5%, ±10%, ±20%	UL/TÜV
1808	15pF	Y3/X2	C0G/NP0	±1%, ±2%, ±5%, ±10%, ±20%	UL/TÜV
1808	18pF	Y3/X2	C0G/NP0	±1%, ±2%, ±5%, ±10%, ±20%	UL/TÜV
1808	22pF	Y3/X2	C0G/NP0	±1%, ±2%, ±5%, ±10%, ±20%	UL/TÜV
1808	27pF	Y3/X2	C0G/NP0	±1%, ±2%, ±5%, ±10%, ±20%	UL/TÜV
1808	33pF	Y3/X2	C0G/NP0	±1%, ±2%, ±5%, ±10%, ±20%	UL/TÜV
1808	39pF	Y3/X2	C0G/NP0	±1%, ±2%, ±5%, ±10%, ±20%	UL/TÜV
1808	47pF	Y3/X2	C0G/NP0	±1%, ±2%, ±5%, ±10%, ±20%	UL/TÜV
1808	56pF	Y3/X2	C0G/NP0	±1%, ±2%, ±5%, ±10%, ±20%	UL/TÜV
1808	68pF	Y3/X2	C0G/NP0	±1%, ±2%, ±5%, ±10%, ±20%	UL/TÜV
1808	82pF	Y3/X2	C0G/NP0	±1%, ±2%, ±5%, ±10%, ±20%	UL/TÜV
1808	100pF	Y3/X2	C0G/NP0	±1%, ±2%, ±5%, ±10%, ±20%	UL/TÜV
1808	120pF	Y3/X2	C0G/NP0	±1%, ±2%, ±5%, ±10%, ±20%	UL/TÜV
1808	150pF	Y3/X2	C0G/NP0	±1%, ±2%, ±5%, ±10%, ±20%	UL/TÜV
1808	180pF	Y3/X2	C0G/NP0	±1%, ±2%, ±5%, ±10%, ±20%	UL/TÜV
1808	220pF	Y3/X2	C0G/NP0	±1%, ±2%, ±5%, ±10%, ±20%	UL/TÜV
1808	270pF	Y3/X2	C0G/NP0	±1%, ±2%, ±5%, ±10%, ±20%	UL/TÜV
1808	330pF	Y3/X2	C0G/NP0	±1%, ±2%, ±5%, ±10%, ±20%	UL/TÜV
1808	390pF	Y3/X2	C0G/NP0	±1%, ±2%, ±5%, ±10%, ±20%	UL/TÜV
1808	470pF	Y3/X2	C0G/NP0	±1%, ±2%, ±5%, ±10%, ±20%	UL/TÜV
1808	560pF	Y3/X2	C0G/NP0	±1%, ±2%, ±5%, ±10%, ±20%	UL/TÜV
1808	680pF	Y3/X2	C0G/NP0	±1%, ±2%, ±5%, ±10%, ±20%	UL/TÜV
1808	820pF	Y3/X2	C0G/NP0	±1%, ±2%, ±5%, ±10%, ±20%	UL/TÜV
1808	1nF	Y3/X2	C0G/NP0	±1%, ±2%, ±5%, ±10%, ±20%	UL/TÜV
1808	150pF	Y3/X2	X7R	±5%, ±10%, ±20%	UL/TÜV
1808	180pF	Y3/X2	X7R	±5%, ±10%, ±20%	UL/TÜV
1808	220pF	Y3/X2	X7R	±5%, ±10%, ±20%	UL/TÜV
1808	270pF	Y3/X2	X7R	±5%, ±10%, ±20%	UL/TÜV
1808	330pF	Y3/X2	X7R	±5%, ±10%, ±20%	UL/TÜV
1808	390pF	Y3/X2	X7R	±5%, ±10%, ±20%	UL/TÜV
1808	470pF	Y3/X2	X7R	±5%, ±10%, ±20%	UL/TÜV
1808	560pF	Y3/X2	X7R	±5%, ±10%, ±20%	UL/TÜV
1808	680pF	Y3/X2	X7R	±5%, ±10%, ±20%	UL/TÜV
1808	820pF	Y3/X2	X7R	±5%, ±10%, ±20%	UL/TÜV
1808	1nF	Y3/X2	X7R	±5%, ±10%, ±20%	UL/TÜV
1808	1.2nF	Y3/X2	X7R	±5%, ±10%, ±20%	TÜV
1808	1.5nF	Y3/X2	X7R	±5%, ±10%, ±20%	TÜV
1808	1.8nF	Y3/X2	X7R	±5%, ±10%, ±20%	TÜV
1808	2.2nF	Y3/X2	X7R	±5%, ±10%, ±20%	TÜV

Electrical Specification

Operating Temperature	-55°C to +125°C
Temperature Coefficient	C0G/NP0 = 0 ± 30 ppm/°C, Ultra Stable Class 1 Ceramic (EIA Class 1) X7R = ±15%, Stable Class II Ceramic (EIA Class II)
Insulation resistance at +25°C	>100GΩ
Insulation resistance at +125°C	>10GΩ
Dielectric Strength (DWV)	1500VAC/3000VDC
Rated voltage	250VAC
Climatic Category (IEC)	55/125/56
Ageing rate	C0G/NP0 = zero X7R = 1% per decade of time
Test parameters for capacitance	C0G/NP0 = 1Vrms @ 1MHz @ 20°C X7R = 1Vrms @ 1KHz @ 20°C
Test parameters for DF	C0G/NP0 = 1Vrms @ 1MHz @ 20°C X7R = 1Vrms @ 1KHz @ 20°C

Mechanical Specification

Chip Size	1808
Length (L1)	4.5mm ± 0.35mm (0.18" ± 0.014")
Width (W)	2.0mm ± 0.3mm (0.08" ± 0.012")
Thickness (H)	2.0mm (0.08") Max.
Termination Bands (L2, L3)	0.25 - 0.80mm (0.01" - 0.03")
Creepage Distance (L4)	2.5mm (0.1") Min.
Termination Material	Nickel Barrier (Tin over Nickel)
Solderability	IEC 68-2-20

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Specification	Details
EN 132400: 1994 + A2: 1998 + A3: 1998 + A4: 1999 **IEC 60384-14 second edition 1993 + A1: 1995**	Meets the electrical requirements of these specifications for class Y3 and X2 devices. These capacitors do not meet the creepage distance of these specifications.
EN 61000-4-5 **IEC 1000-4-5** **IEC 801-4-5**	Meets the requirements within these specifications for impulse testing, for 1.2/50µS (2Ω source) and 10/700µS (15Ω source) waveforms. Peak value for both waveforms = 2.5KV.
IEC 60950: 1992	Certified for use in equipment intending to be certified to IEC 60950. Units meet the creepage limitations set out within this specification. Impulse requirements for this specification are met or exceeded by those specified in EN 132400 and EN 61000-4-5.
IEEE 802.3	Meets the 1500Vrms isolation requirements of section 12.10.1 of this specification.
UL 60950 (previously UL 1950)	Meets the 1500Vrms isolation requirements of (previously UL 1950) this specification.

Approvals

Marked parts can be released as certified by TÜV (C0G/NP0 and X7R). Unmarked parts can be supplied tested in accordance with, but not certified by TÜV.

TÜV Rheinland Product Safety — BAUART GEPRÜFT — TYPE APPROVED

TÜV Certificate No. R2110618

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UL 60950
6th Edition
UL Certificate No E235189

Reeled Quantities		
	178mm (7″)	1500
	330mm (13″)	6000

Ordering Information

1808	J	A25	0102	J	C	T	SPU
Chip Size	**Termination** J= Nickel Barrier Y=FlexiCap	**Voltage** A25=250VAC	**Capacitance** Expressed in picofarads (pF). First digit is 0. Second and third digits are significant figures of capacitance code. The fourth digit is number of zeros following. Example: 0102=1000pF. For values below 10pF insert a P for the decimal point. eg: 8P20=8.2pF	**Tolerance** <10pF C=±0.25pF D=±0.5pF ⩾10pF F=±1% G=±2% J=±5% K=±10% M=±20%	**Dielectric** C=C0G/NP0	**Packaging** T=178mm (7″) reel R=330mm (13″) reel B=Bulk	SPU=Unmarked SP=Marked

SYFER TECHNOLOGY LIMITED
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