



User Guide for FEBFOD8316 Evaluation Board

**2.5 A Output Current, IGBT Drive
Optocoupler with Desaturation Detection
and Isolated Fault Sensing**

**Featured Fairchild Product/s:
FOD8316**

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1. Overview

Fairchild Semiconductor's FOD8316 smart gate driver optocoupler, an advanced 2.5 A output current IGBT drive optocoupler, offers the critical protection necessary for preventing fault conditions that lead to destructive thermal runaway of IGBTs. Pin-for-pin compatible with current solutions, the FOD8316 consists of an integrated gate drive optocoupler featuring low $R_{DS(ON)}$ CMOS transistors to drive the IGBT from rail-to-rail and high-speed isolated feedback circuitry for fault sensing. It is ideally suited for driving fast-switching power IGBTs and MOSFETs.

The FOD8316 offers best-in-class noise immunity, resulting from its proprietary Optoplanar® coplanar packaging technology. The optoplanar technology ensures safe insulation thickness of more than 0.4 millimeters in attaining reliable high-voltage isolation, certified by UL1577 and DIN EN/IEC60747-5-5 standards.

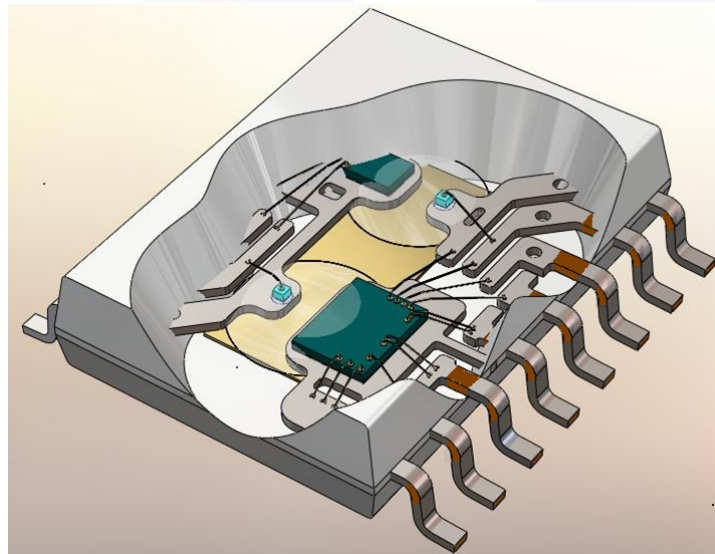


Figure 1. 3-Dimensional Illustration of the Internal Die Set of Fairchild's Optoplanar® Package Construction

1.1. Features and Benefits

- 2.5 A output current driving capability for most 1200 V / 150 A IGBTs
- High noise immunity characterized by CMR: 35 kV/ μ s at $V_{cm} = 1500 V_{peak}$
- 1414 V_{peak} working insulation voltage and 8000 V_{peak} transient isolation voltage rating
- Output voltage swing rail-to-rail: low power dissipation
- Soft IGBT turn-off
- High speed: 500 ns propagation delay
- 3.3 V / 5V, CMOS/TTL-compatible inputs

1.2. Applications

- Motor Drives
- Industrial Inverters
- Solar Power Inverters
- Uninterruptible Power Supplies (UPS)
- Induction Heating
- Isolated IGBT Drive

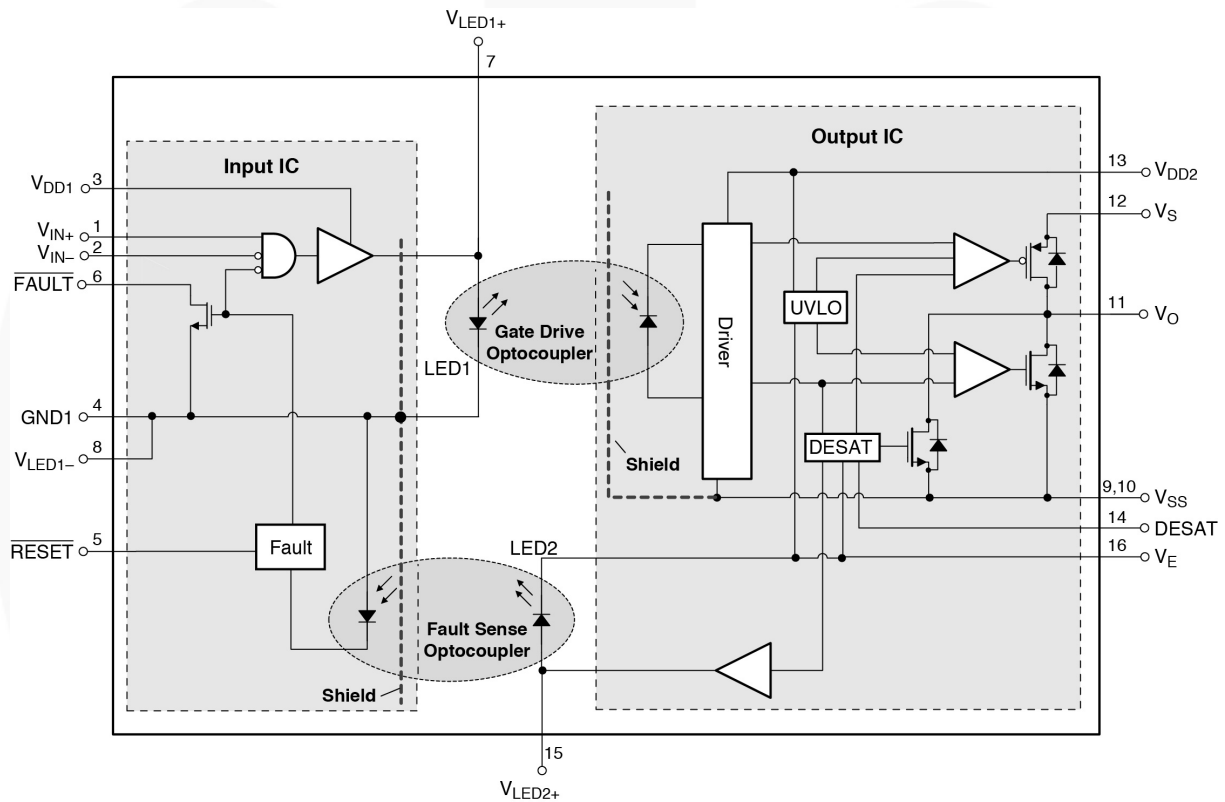


Figure 2. FOD8316 Block Diagram

2. Operations

The application circuit and the timing diagram illustrate the functional use of the FOD8316 between a micro-controller and a three-phase system, as well as the interaction of the internal and external signals.

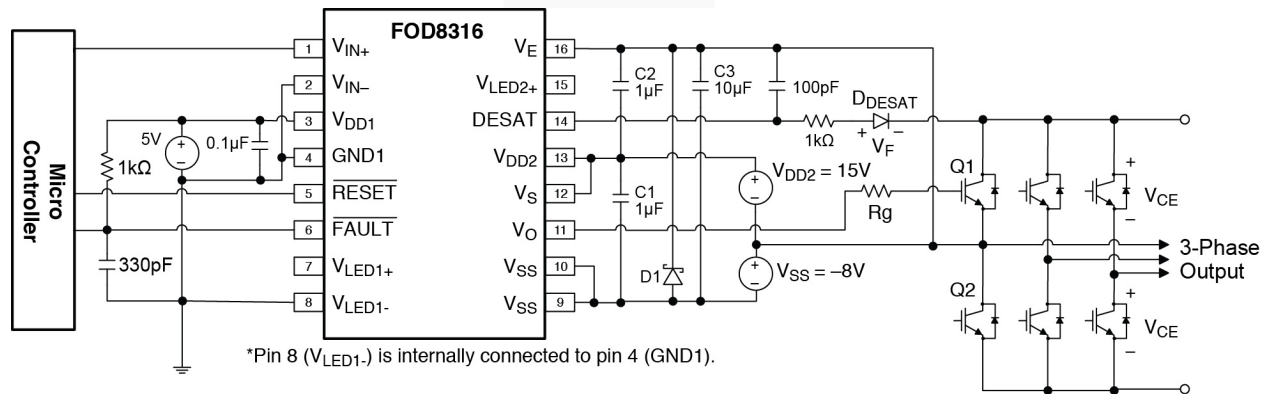


Figure 3. Typical Application Circuit

The internal gate driving circuitry of FOD8316 can be used with either a single positive power supply, V_{DD2} , or a dual positive and negative supply, V_{DD2} and V_{SS} . The output driver stage, V_O , is made up of a pair of PMOS and NMOS transistors, which facilitates close to rail-to-rail output swing. This allows a tight control of gate voltage during on-state and short-circuit condition. Due to the low $R_{DS(ON)}$ of the MOSFETs, the power dissipation is reduced as compared to bipolar-type driver output stages. The absolute maximum rating of the output peak current, $I_{O(PEAK)}$, is 3 A.

FOD8316 provides short-circuit protection by means of desaturation-detection circuits that monitor the collector-emitter voltage of the IGBT. When the DESAT voltage increases above the threshold voltage, a short-circuit condition is detected and the driver output stage executes a “soft” IGBT turn-off and is eventually driven low. The soft turn-off feature ensures the safe turn-off of the IGBT under fault conditions. This reduces the voltage spike on the collector of the IGBT. Without this, the IGBT would see a heavy spike on the collector, resulting in a permanent damage to the device when it is turned off immediately. The FAULT open-drain output is triggered active LOW to report a desaturation error to the micro-controller. The FAULT signal is cleared by activating the RESET pin with an active LOW signal communicated by the external controller. The DESAT fault detector should be disabled for a short period (blanking time) before the IGBT turns on to allow the collector voltage to fall below the DESAT threshold. This blanking period protects against false trigger of the DESAT while the IGBT is turning on.

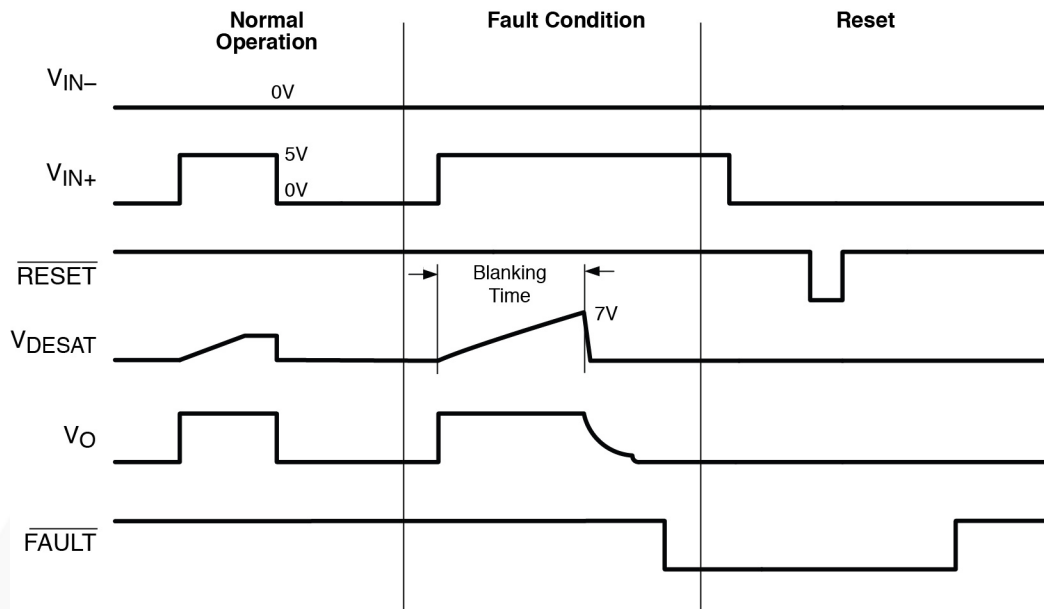


Figure 4. Timing Diagram

The FOD8316 is also designed with an under-voltage detection circuit to prevent the application of insufficient gate voltage to the IGBT. This could be dangerous, as it would drive the IGBT out of saturation and into the linear operation where the losses are very high and the device is quickly overheated.

3. Circuit Schematic

The FEBFOD8316 evaluation board with a booster circuit is designed for the evaluation of FOD8316 timing sequence and AC test performance when driving an IGBT power module. It is recommended to be used in conjunction with the datasheet.

The FOD8316 is designed to perform as a stand-alone, optically coupled, gate driver in most applications. If larger gate drive capability is needed for large IGBT modules or parallel operation, an output booster stage may be added to driver for optimum performance.

One possible implementation is by a discrete NPN/PNP totem-pole configuration. These booster transistors should be fast switching and have sufficient current gain to deliver the desired peak output current.

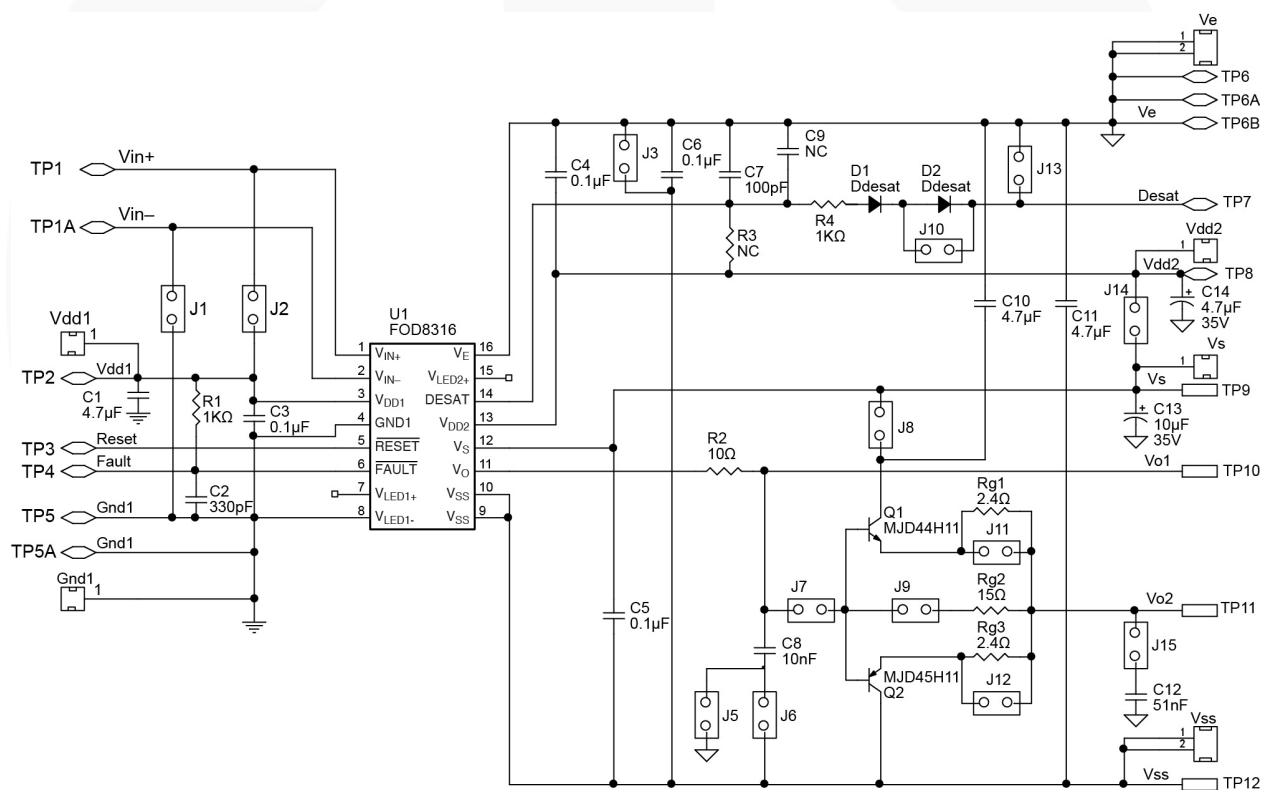


Figure 5. Circuit Schematic

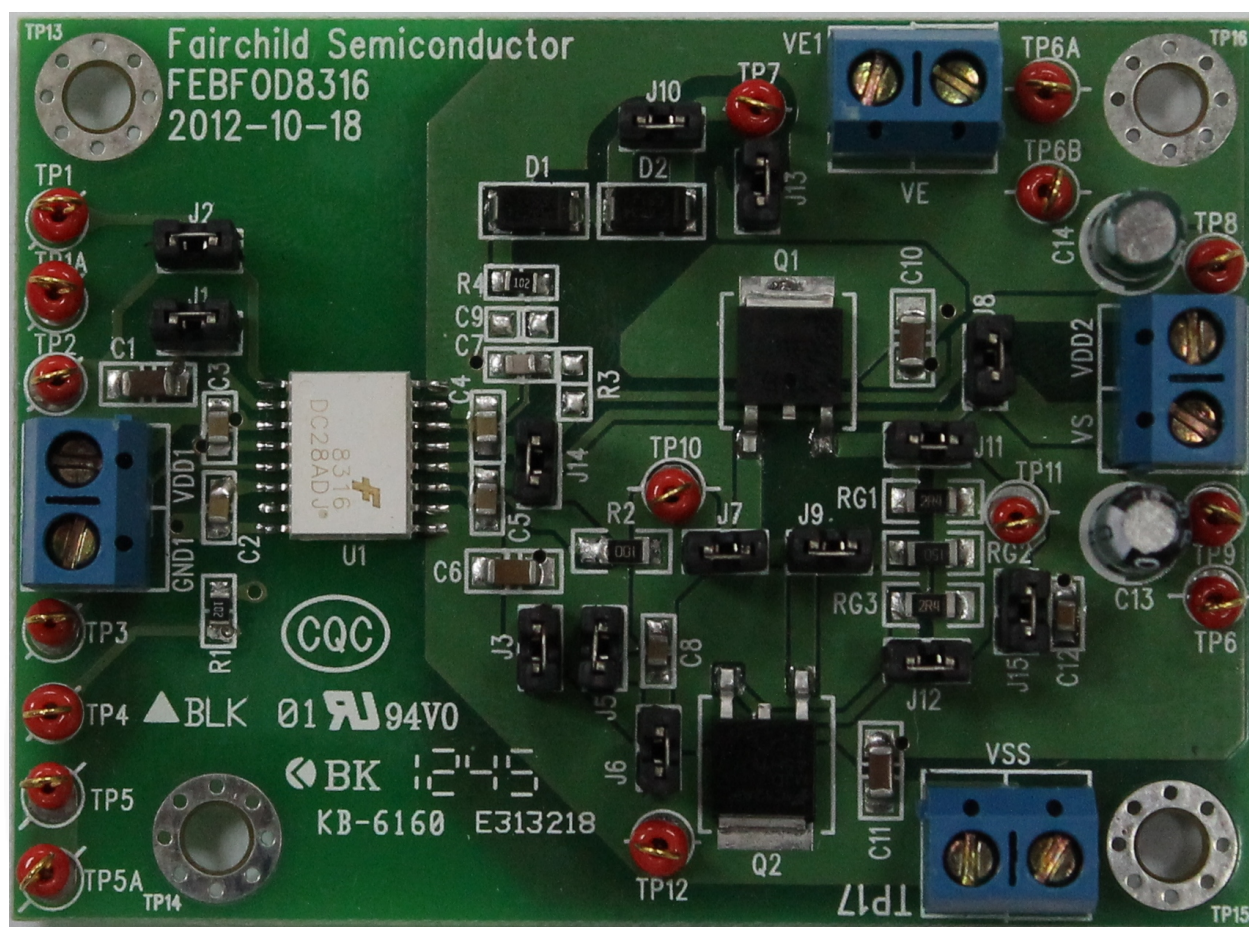


Figure 6. Photograph of the Board

This board consists of a FOD8316 component, a non-inverting bipolar (NPN/PNP) totem-pole current buffer, two capacitor loads (10 nF / 51 nF), as well as connectors and test terminals for power supplies and input signals.

The FOD8316 can be evaluated as a stand-alone gate driver driving a 10 nF capacitor load or FOD8316 with the totem-pole current buffer driving a 51 nF capacitor load.

4. Setup and Operation

The setup requires three power supply sources: V_{DD1} on one side of the isolation barrier, V_{DD2} (positive supply), and V_{SS} (negative supply using two power supplies) on the other side of the isolation barrier.

There are two CMOS/TTL-compatible inputs, V_{IN+} and V_{IN-} , to control the IGBT in non-inverting and inverting configurations, respectively. When V_{IN-} is set LOW, V_{IN+} controls the driver output, V_O in non-inverting configuration. When V_{IN+} is set HIGH, V_{IN-} controls the driver output in inverting configuration.

The subsequent sections describe the set up for non-inverting configuration, where V_{IN-} is connected to GND1.

The input signal is applied at the V_{IN+} and the resulting output is used to drive either a 10 nF capacitor load (C8) or a totem-pole current buffer, which in turn drives a bigger capacitor load (C12). Test points located at selected positions (as indicated in the schematics) allow the technician to probe out the signals and measure the switching characteristics of the device.

5. Test Procedures and Conditions

This section describes the default setup of the FEBFOD8316 evaluation board. Please refer to the schematic in Figure 5.

1. Connect the power supplies across the following connector:
 - Across V_{DD1} and GND1. Set the voltage to 5 V.
 - Across V_{DD2} and V_E (GND of the power supply). Set the voltage to 15 V.
 - Across V_E and V_{SS} (GND of the power supply). Set the voltage to 5 V.

This power supply configuration enables V_O to swing from -5 V to 15 V.
2. Apply the following signal at V_{IN+} : 10 kHz, square wave, 50% duty cycle, amplitude = 5 V.
3. Evaluation can be completed with the FOD8316 as a standalone gate driver or together with the totem-pole current buffer. The jumper configurations are shown in Table 1 on the following page.
4. If soft turn-off evaluation is required, J13 must be left open, with no shorting jumper installed, and TP7 (Desat) has to be pulled above the desat threshold voltage.
5. Scope shots of the signals are shown in the following section using the board in standalone set up and with the totem-pole current buffer.
6. Additional evaluation is accomplished by changing the jumper configuration. For example, the board can be configured to positive gate drive ($V_O > 0$ V), only requiring one power supply source at each side of the isolation barrier. The desat threshold voltage (seen at TP7) and the blanking time, can also be varied using jumper J10 and by soldering additional capacitor on the C9 pads.
7. The test points and their corresponding signals are listed in Table 2 on the next page.

Table 1. EVB Jumper Configurations

Configuration	J1	J2	J3	J4*	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15
Vo swing = 5 V to 15 V; FOD8316 standalone	X				X					X			X	X	
Vo swing = 5 V to 15 V; FOD8316 + totem-pole	X				X		X	X	X	X			X	X	X
Vo swing = 5 V to 15 V; FOD8316 and totem pole (for soft turn-off evaluation)	X				X		X	X	X	X				X	X
Vo swing = 5 V to 15 V; FOD8316 standalone (for soft turn-off evaluation)	X				X					X				X	

X = jumper short, blank = jumper open

*J4 is removed in the latest revision of the evaluation board.

Table 2. Test Points

Test Point	Description
TP1	V_{IN+} , non-inverting gate drive control input
TP1A	V_{IN-} , inverting gate drive control input
TP2	V_{DD1} , positive input supply voltage (3 V to 5.5 V)
TP3	$\overline{RESET}$, FAULT reset input
TP4	$\overline{FAULT}$, fault output
TP5/5A	V_{LED1-} , LED1 cathode (must be connected to ground)
TP6/6A/6B	V_E , output supply voltage/IGBT emitter
TP7	DESAT, desaturation voltage input
TP8	V_{DD2} , positive output supply voltage
TP9	V_S , source of pull-up PMOS transistor
TP10	V_{O1} , gate drive output voltage
TP11	V_{O2} , totem pole current buffer output voltage
TP12	V_{SS} , negative output supply voltage

6. Scope Shots

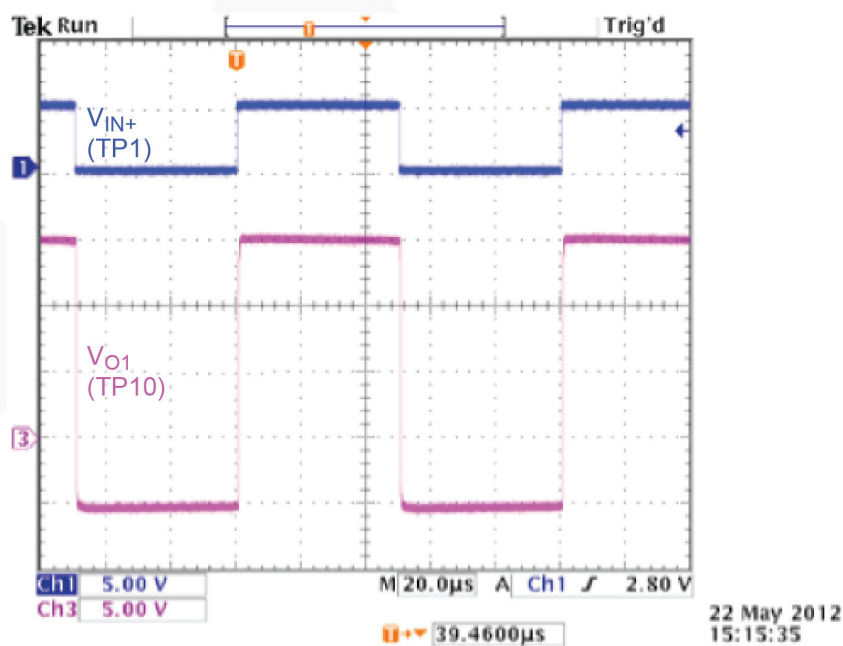


Figure 7. FOD8316 V_{IN+} and V_{O1} Waveform in Standalone Configuration

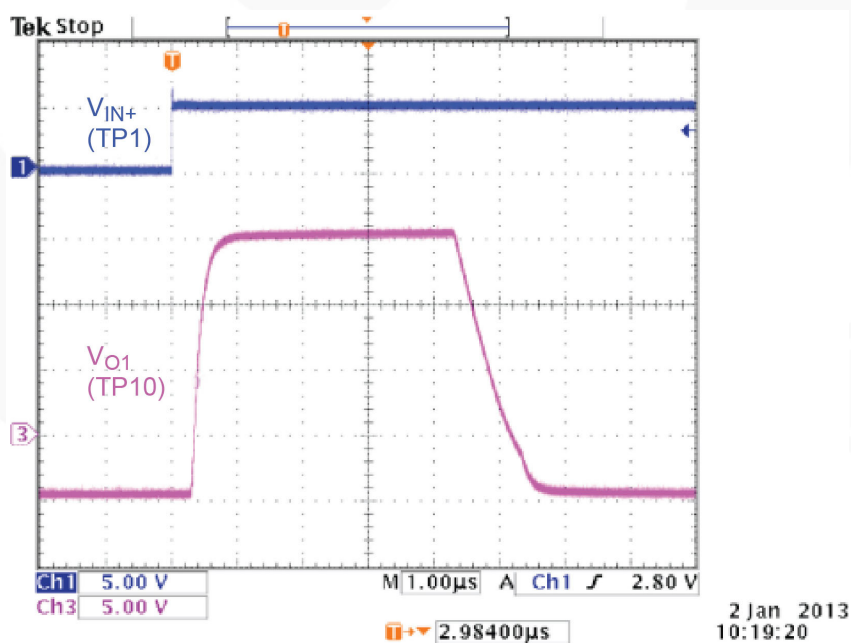


Figure 8. FOD8316 V_{IN+} and V_{O1} Waveform in Standalone Configuration During Soft Turn-Off

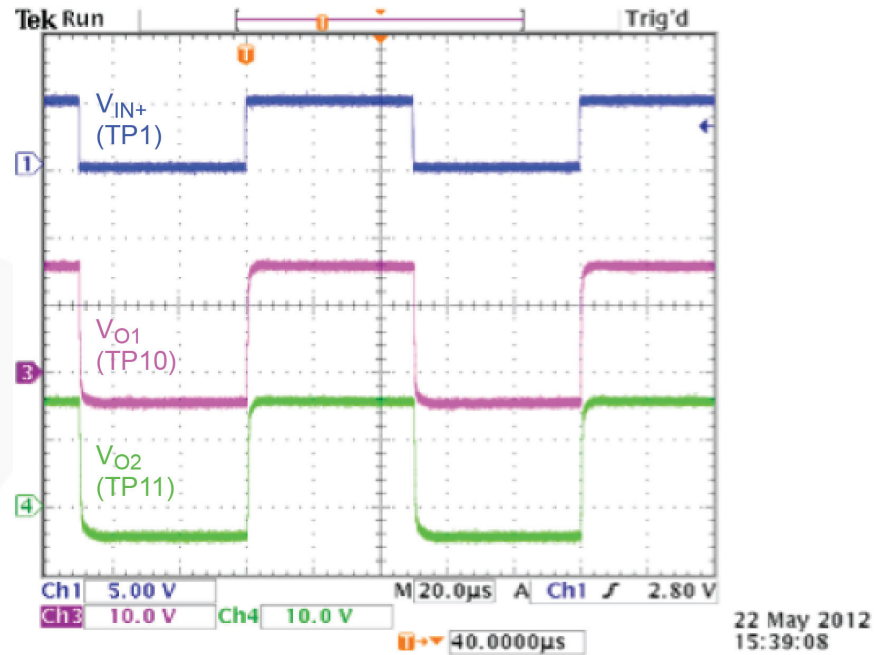


Figure 9. FOD8316 V_{IN+} , V_{O1} and V_{O2} Waveform

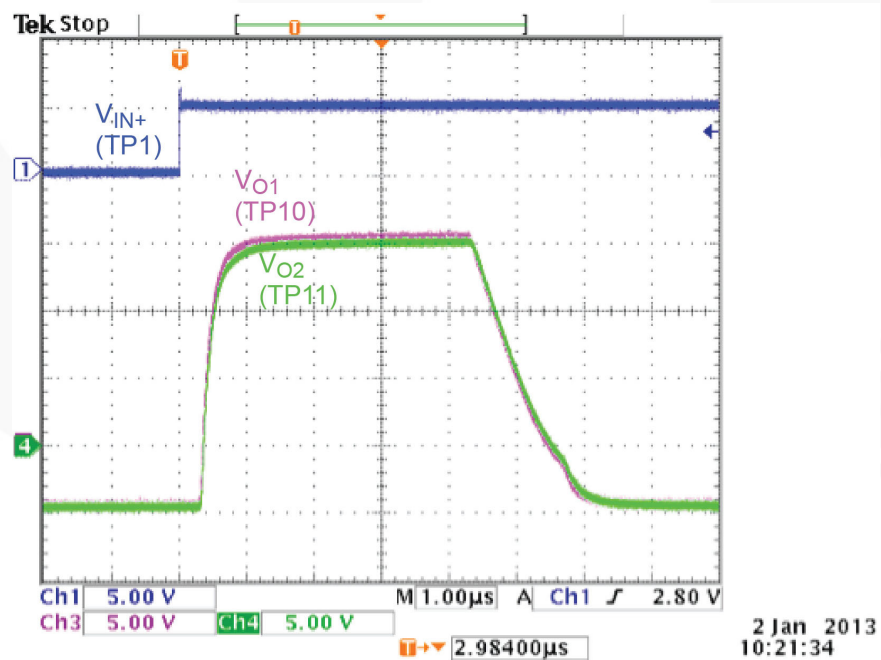


Figure 10. FOD8316 V_{IN+} , V_{O1} and V_{O2} Waveform During Soft Turn-Off



7. Conclusion

The FEDFOD8316 evaluation board allows the user to quickly evaluate the performance of the Fairchild Semiconductor's FOD8316 smart gate driver optocoupler.

Measurement results clearly demonstrate the AC performance and critical protection features of the product that are needed during IGBT fault conditions. With proper booster circuit design, the gate drive capability can be enhanced without affecting key features, such as desaturation detection and soft turn-off timings.

8. Revision History

Rev.	Date	Description
1.0.0	January 2013	Initial Release

WARNING AND DISCLAIMER

Replace components on the Evaluation Board only with those parts shown on the parts list (or Bill of Materials) in the Users' Guide. Contact an authorized Fairchild representative with any questions.

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